A REAL-TIME ENCODING/DECODING SYSTEM (*REDS*) FOR HDTV EDITING

J. H. Jeon*, Y. S. Park*, C. S. Lee, J. Kang,
J. H. Park, D. S. Yoon, and H. W. Park

Dept. of Electrical Engineering
Korea Advanced Institute of Science and Technology (KAIST)
Taejon, Korea

*Also at Samsung Electronics Co., Ltd., Korea

Abstract – A programmable and scalable parallel architecture is proposed for the real-time encoding/decoding of HDTV images and for nonlinear editing of the compressed video data. It only uses the intra-mode compression/decompression so that nonlinear editing can be performed easily and high-quality images can be recovered. Spatially partitioned image data are concurrently processed by multiple parallel processing units (PU's). Each PU consists of a programmable parallel digital signal processor, called multimedia video processor (MVP; TMS320C80), and reconfigurable field programmable logic devices (FPLD's). The performance of the *REDS* is described in terms of the required MVP cycles for transform coding and the FPLD's throughput for entropy coding. Robust RD-optimized quantization matrices for HDTV images are presented.

INTRODUCTION

Multimedia processing is now expected to be the driving force in the evolution of computing, communication, and broadcasting technologies. Digital video and audio processing methods are the most powerful means to extend the capability of television services in both studio and broadcasting systems. As the resolution of digital TV has been increasing, very fast data handling and high computational powers are required. Data compression technology of MPEG-2 standard will be applied to the HDTV broadcasting. However, other aspects should be considered for the purpose of nonlinear HDTV editing in the studio. The data compression technique to store and retrieve vast amount of HDTV data should be computationally efficient, because the amount of data is so vast and the computational requirements are proportional to the amount of data. Also, the image quality at all pictures should be almost perceptually same during the compression and decompression process. Therefore, the JPEG-like encoding/decoding is suitable for the HDTV editing, in which only the intra-mode compression is used. If the motion-compensated compression such as the MPEG-2 MP@HL standard is applied to the HDTV non-linear editing, it results in degradation of the image quality and also the increased computational complexity.

The *REDS* is configured of three functional units as shown in Fig.1; the video unit (VU), the processing unit (PU), and the host unit (HU). It is the multiprocessor architecture based on the spatial partitioning for processing

elements (PE's). In the VU, the digitized HDTV data [1] are first aligned to 64 bit (formatting) according to their color components and divided into multiple strips, each of which includes multiple macroblocks and is the unit of data packet (slicing). Each PU executes the real-time image encoding/ decoding for the assigned strips to those PU's. A PU is composed of a programmable general digital signal processor, called the multimedia video processor (MVP; TMS320C80), and reconfigurable field programmable logic devices (FPLD's). The programmability and scalability of the PU's can provide flexibility and various applications for the future programmable coding, such as traditional video coding or image representation using the description of moving scenes. Various processing algorithms can be implemented in the PU's by only developing the software without changing system hardware [2]. For the nonlinear editing, the intra-mode compression can be implemented in each PU, which mainly consists of two functional modules: One is discrete cosine transform (DCT) to reduce the spatial redundancy. The other is the entropy coding to reduce the statistical redundancy. The MVP performs the DCT, whereas the entropy coding (variable length coding) is implemented in the FPLD's. The compressed strips from all PU's are collected at the HU and stored to the parallel disk system. Decompression process is the reverse process of the compression.

Fig. 1: Block diagram of the REDS.

TRANSFORM CODING

The MVP consists of four fixed-point advanced DSP's (ADSP), one floating-point master processor (MP), and interconnection networks. Four ADSP's perform the DCT in SIMD-like mode. In order to achieve real-time processing for a whole HDTV image, a fast DCT algorithm is proposed by utilizing the characteristics of the ADSP, which can perform one multiplication and two additions simultaneously in one cycle. Some of the fast algorithms [3,4] exploit the properties of the DCT multiplicative constants. We modified the Chen's DCT algorithm so that the numbers of multiplications and additions are balanced for ADSP. The quantization matrix can be also absorbed in this look-up table by scaling each component of these multiplicative constants as shown in Fig 2.

Fig. 2: The signal flow-graph of the proposed fast 1-D DCT.

For the 8×8 input matrix $\mathbf{X}$, the 8×8 1-D DCT output matrix is given as $\mathbf{F} = \mathbf{TX} = \mathbf{CV}$, where $\mathbf{T}$ is 1-D DCT matrix and $\mathbf{F}$ can be expressed by matrix multiplication of the intermediate results $\mathbf{V} = \{v_{i,j}\}$ and diagonal scaling matrix $\mathbf{C}$, whose diagonal components are $\{c_4, c_1, c_2, c_3, c_4, c_5, c_6, c_7\}$. The 2-D DCT output matrix $\mathbf{Y}$ is obtained by applying 1-D DCT on every row of the matrix $\mathbf{F}$. Therefore, $\mathbf{Y} = \mathbf{FT}^T = \mathbf{C}^T \mathbf{HC} = \{m_{i,j} h_{i,j}\}$, where $\mathbf{H} = \{h_{i,j}\}$ is the intermediate results by following the proposed signal flow-graph from input $\mathbf{X}$. The post-multiplication matrix $\mathbf{M} = \{m_{i,j}\}$ can be described as follows; $m_{0,0} = c_4 c_4$, $m_{0,j} = c_4 c_j$, $m_{i,0} = c_i c_4$, and $m_{i,j} = c_i c_j$ for $0 < i, j < 8$. The quantization matrix can be also absorbed in the $\mathbf{M}$ by scaling each component of these multiplicative constants, $\mathbf{M} = \{m_{i,j}/q_{i,j}\}$. Table 1 shows the number of operations required for various 2-D DCT algorithms for a 8×8 block. According to these performances, the required number of MVP's for the real-time implementation of the proposed DCT and the inverse DCT (IDCT) for HDTV image is eight. The IDCT requires more ADSP cycles because multiplications at the first stage of the proposed flow-graph should be computed. Figure 3 shows the PSNR differences with the floating-point 2-D DCT for the proposed and other fixed-point implementations. The proposed algorithm shows better performance.

	Chen's IDCT	Lee's IDCT	Proposed DCT	Proposed IDCT
ADSP's cycle	799	696	394	628

Table 1: The comparison of the number of cycles for fast DCT algorithms.

Fig. 3: The difference values of PSNR between the floating-point 2-D DCT and each fixed-point 2-D DCT algorithm for 256×256 (a) “Lena” image and (b) “Baboon” image with variable Q -scale factors (Q_f) of JPEG default Q matrix.

R-D OPTIMIZED QUANTIZATION

The scaled JPEG or MPEG quantization matrices are normally used to adjust the required quality and the compression rate. The HDTV images represent different characteristics in comparison with conventional JPEG images; different aspect ratio and better spatial correlation with conventional images. Ratnaker and Livny [5] proposed the rate-distortion optimized (RD-OPT) algorithm by considering optimal RD tradeoffs for a given image. The algorithm uses DCT coefficient distribution over a wide range of rates and distortions, and an optimal quantization table is obtained by dynamic programming. The optimal quantization matrix trained for a specific image may not be optimal for the other images. Nearly optimal Q matrices were obtained by statistical averaging the RD-OPT matrices, which were obtained from various HDTV images. The simulation results show that the reconstructed qualities using the proposed Q matrices are better than the JPEG quantization matrix.

7	7	7	7	10	21	14	13
7	7	7	8	14	16	13	9
7	7	7	9	21	14	12	8
8	8	10	16	20	14	11	7
7	8	13	20	14	19	10	7
7	7	8	14	20	12	11	6
8	8	7	13	22	16	11	7
8	10	8	11	18	15	11	8

(a)

8	8	8	7	12	21	13	12
8	8	8	8	15	16	14	8
8	8	8	9	21	14	12	8
8	8	8	10	21	14	11	7
8	8	8	12	20	15	10	6
8	8	8	19	22	15	10	6
8	8	10	20	21	14	9	6
8	10	13	20	21	14	9	6

(b)

Fig. 4: RD-OPT quantization matrices for (a) frame and (b) field of HDTV images.

Fig. 5: PSNR comparison between JPEG quantizer and the proposed quantizer for “HD850” image.

ENTROPY CODING

The input bit-rates to the variable length coder (VLC) were analyzed using the three MPEG-2 test image sequences of “Football”, “Cheer Leaders”, and “Mobile and Calendar”. The “Mobile and Calendar” has the largest average number of non-zero DCT coefficients, 11.66 (coefficients/block). The FPLD for VLC is fully pipelined with five stages. From the run-level coded data, a code symbol and a code length are obtained by the table look-up method. The average throughput for the VLC-FPLD is 20 million codewords/sec. Therefore, eight PU’s are required for the real-time implementation of the VLC for HDTV images.

The variable length of the Huffman code is optimized for coding efficiency, but the variable length limits the decoding throughput because of the recursive data-dependent procedure. The VLC decoding should be performed sequentially. The VLC decoder generally includes a feedback path, which is the critical path for code length-decoding (LD) and symbol-decoding (SD). In the parallel PLA-based architecture proposed by Sun and Lei [6], the feedback path consists of three or four sequential processes. In our FPLD implementation of VLD, two shift processes, input plane barrel shifter (IPBS) for the LD and the SD and output plane barrel shifter (OPBS) for next-input alignment, can be performed concurrently as shown in Fig 6. In addition, the decision whether new data must be read or not can also be performed in parallel with above two shift processes. From a simulation using the sample frames in MPEG-2 video sequences (“Mobile and Calendar”, “Football”, and “Cheer Leaders”), the required processing time of the proposed method for intra-mode pictures was about 70 % of [6].

CONCLUSIONS

A real-time encoding/decoding system, called *REDS*, for nonlinear editing of HDTV image was presented. It is a multiprocessor architecture which uses the MVP as its PE. Equally spatial-partitioned data is transferred to each PE and is

compressed by transform coding and entropy coding to reduce spatial redundancy and statistical redundancy, respectively. The signal flow-graph of the Chen DCT algorithm is modified to adapt the implementation in MVP, so that the required ADSP's cycles are reduced and PSNR performance is better than those of the other methods. By averaging Q matrices that were obtained using RD-OPT algorithm, two scalable Q matrices were obtained. The proposed Q matrices outperform the JPEG Q matrices. The FPLD implementations of VLC and VLD were simulated for the real-time performances.

* CRL: Current Remaining Length

Fig. 6: The hardware block diagram of the proposed VLD-FPLD.

References

- [1] *SMPTE Standard*, "For Television Digital Representation and Bit-Parallel Interface-1125/60 High-Definition Production System", 1995.
- [2] J. H. Jeon, H. S. Kim, G. N. Boo, J. S. Song, E. W. Lee, and H. W. Park, "Real-Time MPEG-2 Video Codec System Using Multiple Digital Signal Processors," *Multimedia Tools and Applications*, to appear.
- [3] B. G. Lee, "A new algorithm to compute the discrete cosine transform," *IEEE Trans. Acoust., Speech, Signal Processing*, vol. 35, no. 6, pp. 1243-1245, Dec. 1984.
- [4] W. H. Chen, C. H. Smith, and S. C. Fralick, "A fast computational algorithm for the discrete cosine transform," *IEEE Trans. Commun.*, vol. 25, pp. 1004-1009, Sep. 1977.
- [5] V. Ratnakar, M. Livny, "RD-OPT: An Efficient Algorithm For Optimizing DCT Quantization Tables," *Proceedings of Data Compression Conference '95*, pp.332-341, 1995.
- [6] S. M. Lei and M. T. Sun, "An entropy coding system for digital HDTV applications," *IEEE Trans. Circuits and Systems for Video Technology*, vol. 1, pp. 147-154, Mar. 1991.