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PAPER

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Large-area, scalable fabrication of conical TiN/GST/TiN nanoarray for low-power phase change memory†

Jong Moon Yoon,[a] Hu Young Jeong,[b] Sung Hoon Hong,[c] You Yin,[d] Hyoung Seok Moon,[a] Seong-Jun Jeong,[e] Jun Hee Han,[a] Yong In Kim,[a] Yong Tae Kim,[f] Heon Lee,[c] Sang Ouk Kim*[a] and Jeong Yong Lee*[a]

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We demonstrate the fabrication and phase change memory performance of a conical TiN/$Ge_2Sb_2Te_5$ (GST)/TiN nanoarray prepared *via* block copolymer lithography and straightforward two-step etching. The created 30 nm scale phase change memory cell (aerial array density: ~207 Gbit inch^{-2}) showed a threshold switching voltage of 1.1 V, a value compatible to conventional phase change memory cells. More significantly, the cell could be amorphized by a reset pulse of 1.8 V height and 100 ns width, where the reset current was 100 μA. Such a low reset current, presumably caused by nanoscale small cell dimension, is greatly beneficial for low power consumption device operation. Reversibly, the set operation was accomplished by crystallization with a set pulse of 1.2 V height, 100 ns width, and 100 ns trailing. This work provides a significant step for low power consumption and ultra-high density storage based on phase change materials.

Introduction

Phase change memory (PCM) is a promising non-volatile memory device demonstrating high operation speed, low power consumption, robust cycling endurance, and so on.[1–4] The data program and erase of a PCM device is accomplished by reversible current-induced phase transitions between the high resistive amorphous state (RESET) and the low resistive polycrystalline state (SET).[2,5] Since the phase change induced by Joule heating is dominantly localized at the interface between the phase change materials and the electrode, it is crucial to maintain an impurity- and void-free interface to achieve high device performance.[6] To address this technological challenge, a trilayer structure consisting of electrode/phase change materials/electrode has been suggested, where the device integration of the PCM involved with cell patterning and encapsulation must be performed, securing the trilayer structure.[7]

Since the electric current required for phase change is generally proportional to the material volume, it is crucial to scale down the cell size to the nanoscale to achieve a low power consumption and high density PCM device.[8–11] Meanwhile, currently available conventional photolithography is close to the resolution limit intrinsically destined by optical diffraction. Block copolymer lithography is a promising alternative or complementary technology, which may generate dense sub-10 nm scale features *via* self-assembly of microphase separated nanodomains.[12–19] In particular, the directed assembly of block copolymers into lateral-ordered nanoscale morphologies in conjunction with conventional photolithography, such as ArF or I-line lithography, ensures low-cost, large-area nanopatterning *via* parallel processing.[20–25] To date, there have been a few reports for the nanopatterning of phase change materials *via* block copolymer lithography.[26–29] Nevertheless, the phase change behavior and the corresponding memory switching of the created nanostructure has not been demonstrated yet.

Here we report on an ultra-high density nanopatterning and corresponding PCM performance of a conical TiN (top electrode)/$Ge_2Sb_2Te_5$ (GST)/TiN (bottom electrode) PCM cell array fabricated *via* block copolymer lithography and straightforward two-step etching (ESI,† Fig. S1). Owing to the nanoscale (~30 nm) cell dimension, the resultant conical cell array exhibited outstanding switching behavior, low power consumption and

[a]*Department of Materials Science and Engineering, KAIST, Daejeon, 305-701, Republic of Korea. E-mail: j.y.lee@kaist.ac.kr; sangouk.kim@kaist.ac.kr; Fax: +82 42 350 3310; Tel: +82 42 350 4216/3339*
[b]*School of Mechanical & Advanced Materials Engineering, Ulsan National Institute of Science and Technology (UNIST), Ulsan, 689-798, Republic of Korea*
[c]*Department of Materials Science and Engineering, Korea University, Seoul, 136-701, Republic of Korea*
[d]*Graduate School of Engineering, Gunma University, 1-5-1 Tenjin, Kiryu, Gunma, 376-8515, Japan*
[e]*Department of Materials Science and Engineering, University of California, Berkeley, California, 94720-1760, USA*
[f]*Semiconductor Materials and Devices Laboratory, Korea Institute of Science and Technology, Seoul, 136-791, Republic of Korea*

† Electronic supplementary information (ESI) available: Schematic illustration of nanoscale conical TiN/GST/TiN PCM cell array fabrication, schematic illustration of two-step etching, masked deposition method, endurance-cycling test of conical trilayer PRAM cell, process for SiO_2 encapsulation of PCM cells, and minimum reset pulse width test. See DOI: 10.1039/c1jm14190b

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high speed operation. In particular, the reset current was as low as 100 μA, which is highly desired for high-density PCM devices.[31]

Experimental

Materials

Polystyrene-*block*-poly(methyl methacrylate) (PS-*b*-PMMA) (PS-*b*-PMMA1: M_n^{PS}: 140 kg mol^{-1}, M_n^{PMMA}: 60 kg mol^{-1} and PS-*b*-PMMA2: M_n^{PS}: 5 kg mol^{-1}, M_n^{PMMA}: 5 kg mol^{-1}) was purchased from Polymer Source. The Cr source for electron-beam evaporation (purity: 99.95%) was purchased from Thifine. Copper grids for TEM analysis and shadow mask were purchased from Electron Microscopy Sciences.

Films deposition

The bottom electrode TiN, amorphous $Ge_2Sb_2Te_5$, and top electrode TiN were sequentially deposited on SiO_2/Si substrate for 51 min, 1 min 35 s, and 21 min 15 s in Ar ambient with the 70 W, 40 W, and 70 W rf power and 5 mTorr working pressure, respectively.

Characterization

The nanoscale morphology of block copolymer films and the created Cr dots arrays images were taken using a Hitachi S-4800 SEM. TEM investigations were carried out using a Jeol 2100F. The samples for TEM were prepared by FIB milling using a gallium ion beam in FEI Helios NanoLab system. The electrical property of the TiN/GST/TiN nanoarray cell device was characterized using a conducting AFM. A 40 nm thick Pt coated AFM tip (NSC-36) was used to measure the electrical characteristics of the TiN/GST/TiN nanoarray cell device. The measurement system consists of a voltage source (Keithely 2612), pulse generator (HP 81150A) and conducting AFM (Park Scientific Instrument, XE-100) system.

Results and discussion

We used binary blends of PS-*b*-PMMA1 (M_n^{PS}: 140 kg mol^{-1}, M_n^{PMMA}: 60 kg mol^{-1}) and PS-*b*-PMMA2 (M_n^{PS}: 5 kg mol^{-1}, M_n^{PMMA}: 5 kg mol^{-1}) with a weight ratio of 7 : 3 as a self-assembling material. The low molecular weight PS-*b*-PMMA2 remarkably enhanced the self-assembly process and promoted the lateral nanodomain ordering in the self-assembled nanotemplate.[32] The detailed procedure for preparing self-assembled block copolymer templates was as described elsewhere.[33] The uniformity of a TiN/GST/TiN trilayer film was a fundamental requirement for the successful fabrication of a large-area nanopatterned PCM cell array. The surface roughness of the trilayer film significantly influenced the lateral nanodomain ordering and uniformity of the self-assembled block copolymer templates and, thus, eventually determined the morphology of the conical cell array. Highly uniform trilayer films with surface roughnesses below 0.8 nm (RMS value) could be deposited by employing RF magnetron sputtering at low deposition rates of 2 nm min^{-1} for the TiN (70 W) layer and 10 nm min^{-1} for the GST (20 W) layer. The successive deposition of trilayers without a vacuum break prevented the oxidation or contamination of the interfaces.[6] The selective deposition of a nanoscale Cr hard mask array *via* self-assembled block copolymer nanotemplates on a uniform trilayer film could be confirmed by SEM, as shown in Fig. 1a and b. As designated in Fig. 1c, the average diameter and the center-to-center distance between neighboring Cr nanodots were ~30 nm and ~60 nm, respectively, which exactly replicated the self-assembled morphology of block copolymer nanotemplates.

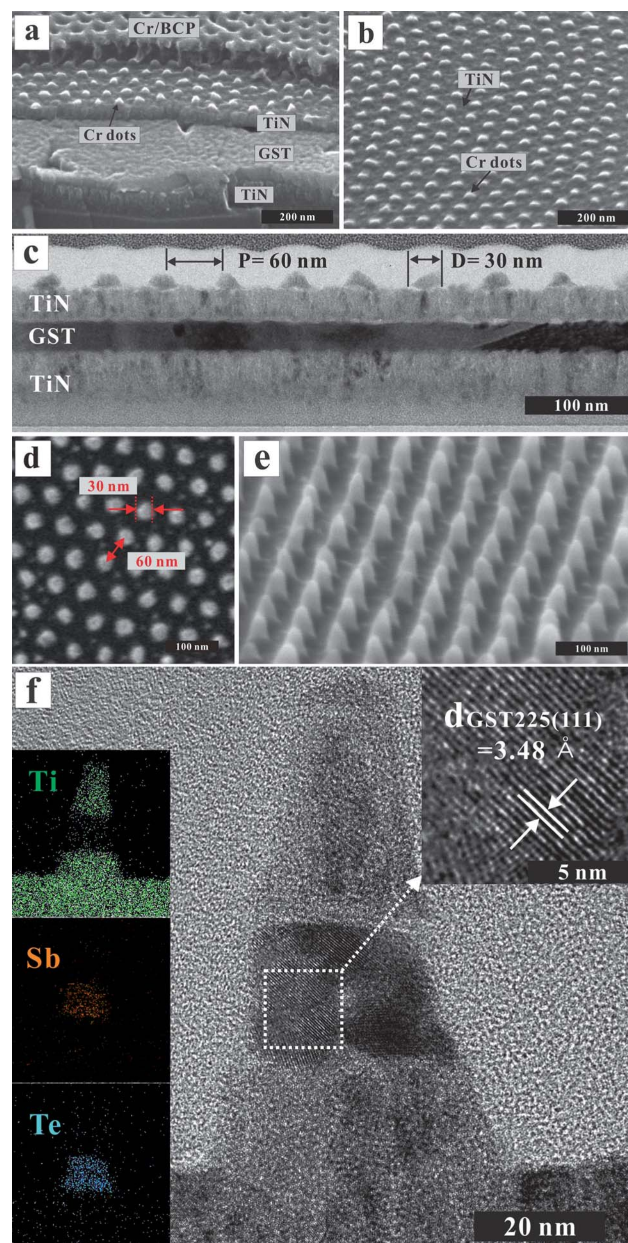

Fig. 1 Cross-sectional (a) SEM images of Cr nanodot arrays deposited *via* block copolymer templates. (b) Tilted-view SEM and (c) cross-sectional TEM images of the generated Cr nanodot arrays. (d) Plane-view and (e) tilted-view SEM images of a nanoscale conical TiN/GST/TiN cell array. (f) Cross-sectional HR-TEM image of a conical TiN/GST/TiN cell. The sample was prepared by FIB (Focused Ion Beam). Inset (top right): magnified HR-TEM image of crystalline $Ge_2Sb_2Te_5$ layer; Inset (left): EDS element mapping of Ti (green), Sb (orange), and Te (sky blue).

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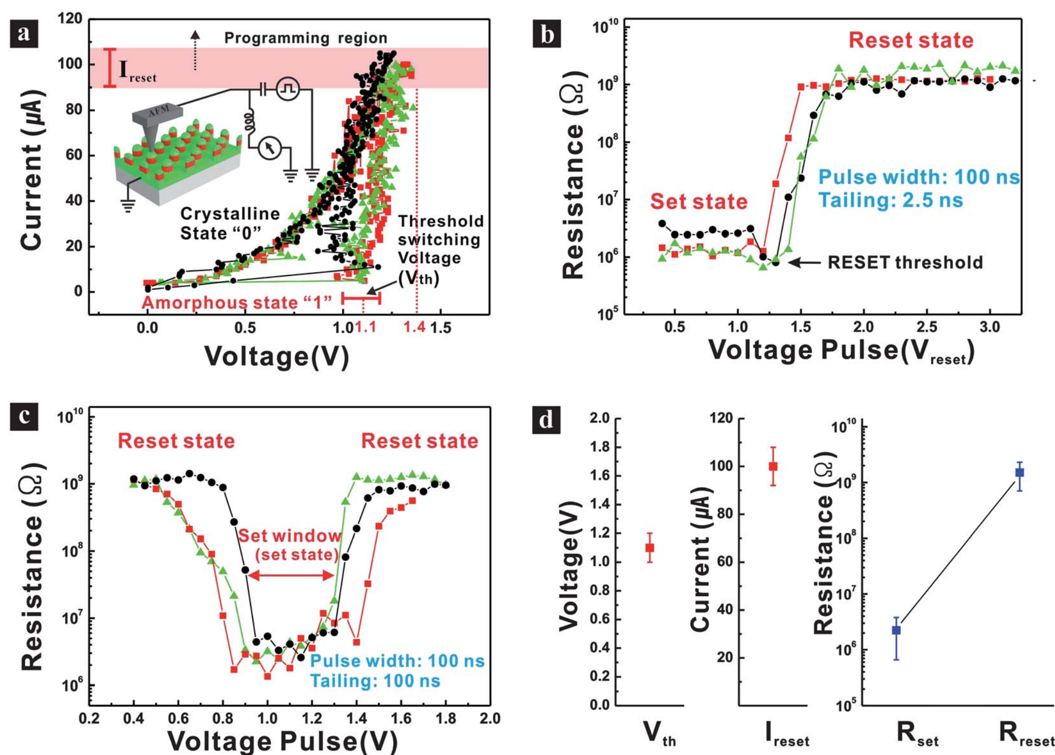

Fig. 2 (a) Current–voltage (I–V) characteristics of a conical TiN/GST/TiN PCM cell in amorphous and crystalline states: Inset: A schematic diagram of the C-AFM measurement system of a single cell. (b) Reset test of a PCM cell with a 100 ns pulse width and 2.5 ns pulse trailing. (c) Set test of a PCM cell with a 100 ns pulse width and 100 ns pulse trailing. (d) Distribution bar graph relating variation of working voltage (V_{th}), reset current (I_{reset}), and set/reset state resistance (R_{set} and R_{reset}).

We employed straightforward two-step ICP-RIE etching with the Ar(45 sccm)/Cl_2(5 sccm) and Ar(45 sccm)/CF_4(5 sccm) gas mixtures (ESI,† Fig. S2) to create PCM cell arrays. In the first etching step, the top electrode TiN was completely etched with the Ar/Cl_2 (30 s etching under 10 mTorr of Ar/Cl_2 and applying power of 400 W (main) and 100 W (bias)) until the GST layer was exposed. In the following step, the exposed GST layer was completely etched with Ar/CF_4 (30 s etching under the aforementioned same chamber pressure and power). The bottom TiN layer was also partly etched to separate the neighboring GST cells. The Cr nanodot array prepared *via* block copolymer lithography was proven to be an appropriate hard mask material, as the etch rate of TiN was approximately two times higher than that of Cr with Ar/Cl_2. We note that although GST had an even higher etching rate than TiN with the Ar/Cl_2 mixture gas, one-step etching with Ar/Cl_2 throughout the trilayer structure was undesired. Due to the high etching rate of GST, it was hard to control the etching depth. Furthermore, ion-assisted chemical etching of GST with Ar/Cl_2 frequently gave rise to undesirable pattern shapes with severe under-cutting.[34] In contrast, the CF_4-based gas mixture employed in this work (Ar/CF_4) could generate highly anisotropic cell shapes without considerable morphological distortions. Fig. 1d and e show the plane-view and the tilt-view SEM images of the fabricated conical TiN/GST/TiN cell, respectively. Owing to the parallel and scalable processing *via* block copolymer lithography and ICP-RIE, the conical cell array could be readily prepared on an arbitrary large-area (ESI,† Fig. S3). It is noteworthy that long-range order and existing defect issues of the block copolymer self-assembled morphology could be addressed by directed self-assembly employing topographic or chemical prepatterns, previously demonstrated by our group and others.[14–17,20–24] The aerial density of the PCM cells was estimated, assuming a perfect hexagonal array formation. According to the aerial density equation of $\rho = [2 \times 6.452/(\sqrt{3}P_{\rm int}^2)] \times 10^{14}$ inch^{-2}, where $P_{\rm int}$ is the center-to-center distance between neighboring PCM cells. The calculated density was ~207 Gb inch^{-2} ($P_{\rm int}$ = 60 nm). As a reference, the currently available commercial CMOS Flash memory is 25 nm NAND technology-based 64 Gb with a die size of 130 mm^2 (318 Gb inch^{-2}).[30] Compared to the previously reported highest-density PCM (1 Gb) demonstrated by Numonyx, our device is approximately 200 times denser. Our device is one of the highest density devices ever demonstrated for PCM devices thus far.[31]

Fig. 1f shows the HR-TEM image of the nanoscale TiN/GST/TiN PCM cells. The ICP-RIE successfully generated a residue-free morphology with an excellent vertical sidewall profile. The inset at the top right shows the magnified HR-TEM image of the GST layer. The observed lattice spacing is consistent with the $Ge_2Sb_2Te_5$ (111) inter-planar distance (3.485 Å) (Cubic, Fm-3m, a = 6.037 Å, PDF #54-0484). Such a high crystallinity confirmed that the $Ge_2Sb_2Te_5$ layer was not damaged during ICP-RIE. The inset at the bottom left shows the superimposed TEM energy dispersive X-ray spectroscopy (EDS) element mapping images for Ti (green), Sb (orange), and Te (sky blue) elements.

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The nonvolatile memory switching performances of the conical PCM cells were investigated by conductive atomic force microscopy (C-AFM) measurements. The inset of Fig. 2a shows the schematic description of C-AFM measurement for a single PCM cell. Fig. 2a presents the measured current–voltage (*I*–*V*) characteristics of trilayer PCM cells. The as-fabricated cell exhibited a linear *I*–*V* characteristic with a low resistance of crystalline GST. The thermal annealing performed at 250 °C during the block copolymer self-assembly caused the crystallization of GST. At reset voltage pulse of 1.8 V (pulse width: 100 ns, pulse trailing: 2.5 ns), the *I*–*V* curve showed a resistance enhancement and subsequent return to its original low value at a threshold voltage of 1.1 V. The reset current of 100 μA was estimated at 1.4 V, which is usually located slightly above the threshold switching voltage.[32] This reset current value was far less than those of the devices fabricated by conventional lithography, whose typical value was ~200 μA for ~0.0108 μm^2 cell size.[31] The fairly low reset current of our device was attributed to the small volume of the nanoscale GST cell. In general, the required reset current is directly proportional to the phase change material volume in a cell.[8,35]

Fig. 2b presents the reset test, where the variation of resistance was monitored as a function of the amorphization voltage pulse (pulse width: 100 ns, pulse trailing: 2.5 ns). An initial low resistance of ~10^6 Ω abruptly increased to a high resistance of ~10^9 Ω at a voltage higher than 1.4 V(resistance ratio: 10^3). The required reset voltage pulse amplitude (reset current) must be higher than 1.4 V (100 μA). Fig. 2c shows the result of the set test. Upon the application of a set pulse with various pulse amplitudes (pulse width: 100 ns, pulse trailing: 100 ns), the resistance gradually decreased from an initial value of ~10^9 Ω down to ~2 × 10^6 Ω at 0.85–0.95 V. Thereafter, the resistance started to increase and restored its original value at a voltage higher than 1.4 V. This indicates that the secure set window range was 0.95 V–1.3 V. 1.2 V was chosen as the set voltage pulse amplitude. Based on the reset and set tests, the conditions for reset (pulse amplitude: 1.8 V, pulse width: 100 ns, pulse trailing: 2.5 ns) and set (pulse amplitude: 1.2 V, pulse width: 100 ns, pulse trailing: 100 ns) were found for reliable program and erase operations, respectively. We note that although electric measurement results for three cells are presented in Fig. 2, the reproducibility of electrical measurement was confirmed by numerous different cell measurements. Owing to the uniform cell size achieved by block copolymer lithography, V_{th}, I_{reset}, R_{set}, and R_{reset} showed narrow distributions as presented by distribution bars in Fig. 2d.

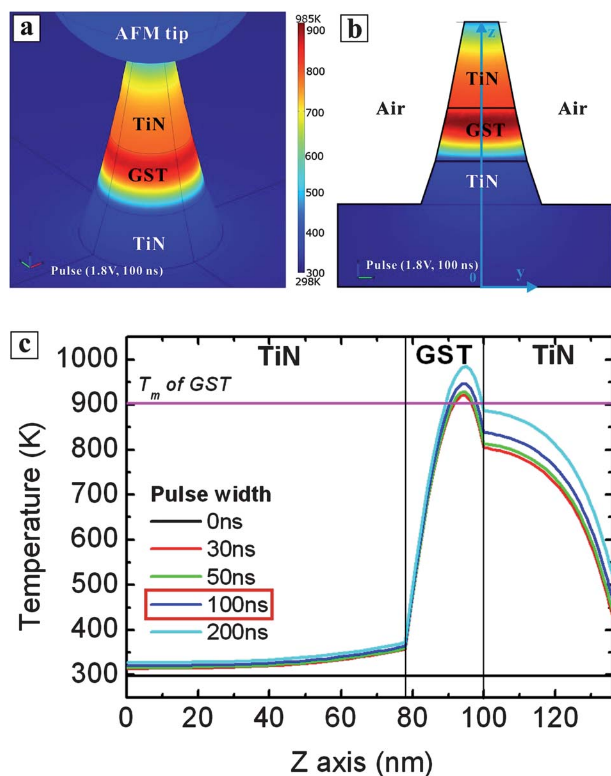

Fig. 3 The finite element analysis (FEA) simulation results of temperature profiles in a conical TiN/GST/TiN PCM cell by applying various reset pulses. (a) 3D temperature distribution with a reset pulse of 1.8 V and 100 ns. (b) The central slice temperature distribution with a reset pulse of 1.8 V and 100 ns. (c) Temperature distribution was monitored as a function of *Z* axis distance with various reset pulse widths.

The endurance-cycling tests under alternating program/read/erase/read pulses were performed (ESI,† Fig. S4). The program/read/erase/read pulse sequences were applied continuously with reset and set pulse. The resistance values were read out at 0.5 V after each pulse. The cycling test successfully demonstrated reliable operation without failure up to dozens of cycles, above which the C-AFM tip underwent spontaneous thermal drift such that further measurement could be hardly performed. Taken together, the measured reliable electrical switching behaviors clearly confirmed that our conical PCM cell can be configured as a low power consumption and rewritable nonvolatile memory device. We note that the void space between neighboring PCM cells could be encapsulated with SiO_2 by PECVD (ESI,† Fig. S5). After encapsulation, the top surface could be mechanically polished to expose the top TiN electrode. This additional SiO_2 passivation is proposed to prevent material loss during Joule heating, which is highly desired for a stable device operation.[7]

The experimentally confirmed phase change behavior of the nanoscale GST cell was simulated by a finite element anlysis (FEA) of cell temperature profile performed with a commercially available software COMSOL 4.1 (Fig. 3). In this analysis, the actual shapes and materials of C-AFM tip as well as conical GST cell could be taken account. When 1.8 V–100 ns reset pulse was applied, the simulated temperature distribution showed that the top part of the GST cell was heated above the melting temperature (T_m) of GST (903 K) (Fig. 3a and b). This molten region would transform into a highly resistive amorphous state after rapid cooling down in a nanosecond time scale. Fig. 3c presents the simulated temperature profiles along the central line of a cell after applying pulses with various widths from 0 to 200 ns. It is obvious that only a small part of the cell was heated above T_m at pulse widths of 30 ns and 50 ns. In contrast, a pulse width longer than 100 ns caused a reliable amorphization, which could bring about a large resistance increase to the reset state. We note that the simulation result was quantitatively well-consistent with the experimentally measured minimum reset pulse width (ESI,† Fig. S6).

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Conclusions

We have demonstrated the successful fabrication of a nanoscale conical TiN/$Ge_2Sb_2Te_5$/TiN trilayer PCM cell array *via* block copolymer lithography and straightforward two-step etching. The robust memory switching behavior of the resultant PCM cell array with an extremely high areal density of ~207 Gbit $inch^{-2}$ could be investigated by C-AFM measurement and FEA simulation. The reset and set states were reversibly switched by employing reset pulse (1.8 V, pulse width: 100 ns, pulse trailing: 2.5 ns) and set pulse (1.2 V, pulse width: 100 ns, pulse trailing: 100 ns), respectively. In particular, the reset current was as low as 100 μA, which is highly advantageous for high-density PCM devices. This conical trilayer PCM device satisfies the requirements of next-generation nonvolatile memory devices, including low power consumption, scalability, robust cyclic stability, and fast switching. Furthermore, further development of this approach in conjunction with directed block copolymer assembly integrated with conventional lithography would accomplish the low-cost, scalable production of fully addressable nanoscale PCM cell arrays.[20–24]

Acknowledgements

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