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Ultralarge capacitance–voltage hysteresis and charge retention characteristics in metal oxide semiconductor structure containing nanocrystals deposited by ion-beam-assisted electron beam deposition

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Amorphous silicon films are deposited by ion-beam-assisted electron beam deposition and subsequently oxidized by a rapid thermal oxidation process. The oxidized film contains a large density of nanocrystals specifically localized at a certain depth from the Si/SiO_x interface, whereas no evidence of nanocrystals is found for oxidized films deposited without ion beam assistance. Such a marked contrast resulted from the enhancement of nucleation rate by ion beam irradiation. The metal-oxide-semiconductor structure utilizing the film shows an ultralarge capacitance–voltage hysteresis whose width is over 20 V. In addition capacitance–time measurement shows a characteristic capacitance transient indicating nondispersive carrier relaxation. The retention time shows a dependence on applied bias and the maximum time of ~70 s is obtained near midgap voltage. The retention time dependence on applied bias and large capacitance–voltage hysteresis are attributed to direct tunneling of trapped charges in the deep traps of nanocrystals to the interface states. © *2001 American Institute of Physics.* [DOI: 10.1063/1.1337618]

Si nanocrystals have recently attracted much attention because of their light-emitting ability.[1–4] Combined with matured Si technology, the light-emitting Si nanocrystals may offer a new class of materials applicable to Si-based monolithic optoelectronic integrated circuit. Besides the attractive light-emitting property, Si nanocrystals in SiO_2 matrix have regained the interest as a possible candidate for memory node in single electron memory device (SEMD). The conditions for SEMD application such as large charging energy for room temperature operation and opaque tunneling barrier for suppressing cotunneling or charge number fluctuation in the charging island are usually met in Si nanocrystal/SiO_2 system. Despite the random distribution and size dispersion problems, innovative single electron devices containing nanocrystals and operating at room temperature have been reported.[5–8]

Nanocrystals have been synthesized by several methods including ion implantation,[2] cosputtering,[3] and silicon-rich-oxide,[4] etc. However, research toward the establishment of stable and reliable methods compatible with the standard CMOS process is still required. In this letter, we investigate a method employing Ar ion beam activation during amorphous Si deposition. In our previous work,[9] we prepared amorphous Si film by e-beam deposition technique with Ar ion beam assistance. After rapid thermal annealing in N_2 ambient, the film deposited by ion-beam-assisted e-beam deposition (IBAED) showed a marked contrast with the film deposited only by e-beam deposition (EBD) in photoluminescence (PL) and transmission electron microscope (TEM) observations. In the PL property of IBAED sample, we observed the PL peak centered at 772 nm and was attributed to the PL from nanocrystals. By contrast, for the EBD sample, we observed only featureless the PL signal widely spreading over visible wavelength region. The PL signal was attributed to some defect-related recombination. For cross-sectional TEM of the annealed EBD sample, we had no evidence of nanocrystals as expected. However, for the annealed IBAED sample, we observed nanocrystals (5–10 nm size) distributed in amorphous Si matrix. Interestingly nanocrystals were distributed laterally at a depth of about 7 nm from the crystalline Si/amorphous Si interface as shown in Fig. 1(a). The present work is motivated by our previous work since the interesting distribution of nanocrystals may result in some interesting charging behavior useful for SEMD application.

Amorphous Si films, 200 nm thick, were deposited either by IBAED or EBD on *p*-Si substrate. Briefly, sample surfaces were presputtered to remove native oxide and other contaminants. Then, for the IBAED sample, the surface was bombarded with an Ar ion beam by utilizing a 2-grid Kaufman ion source (Oxford Applied Research MPD22I) during deposition. Ion acceleration voltage was 500 V. Essentially the samples used in the present work are obtained from the part of the wafer adjacent to the samples used in the previous work. PLs are dispersed by 0.75 m SPEX spectrometer and detected by a photomultiplier with a GaAs detector. As an excitation source, the 364 nm line of Ar ion laser was used.

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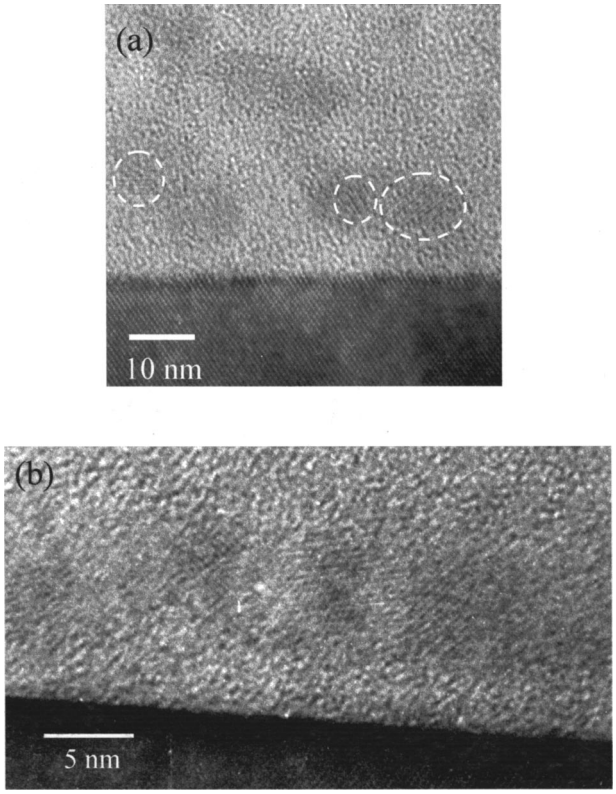

FIG. 1. Cross-sectional TEM images of IBAED samples (a) RTA treated at 1000 °C for 10 min. in N_2 and (b) RTO treated at 1000 °C.

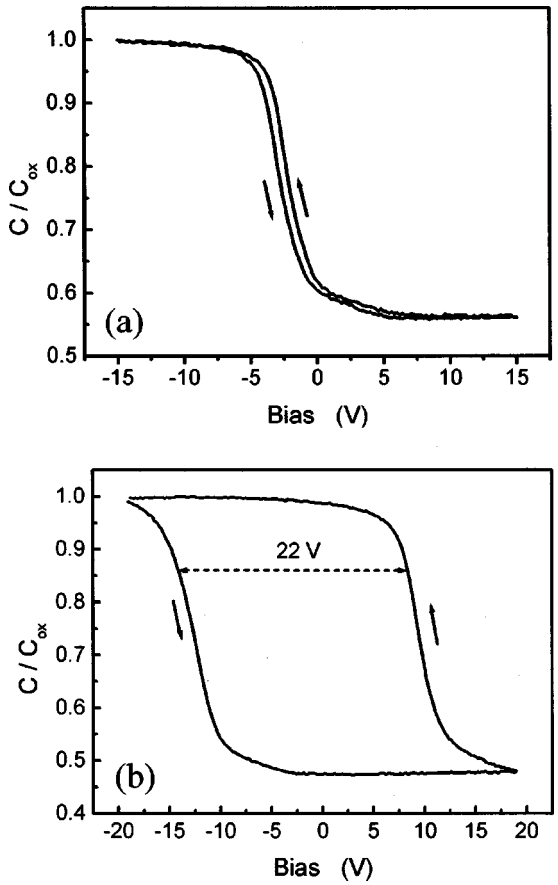

FIG. 2. $C-V$ characteristics of EBD sample (a) and IBAED sample (b). A dual sweeping mode is employed for $C-V$ characteristics. Arrows in the figures are sweeping directions, sweeping rate was 2 V/s.

For capacitance–voltage ($C-V$) and capacitance–time ($C-t$) measurements, a Keithley 590 $C-V$ analyzer was used. All measurements were done at room temperature.

For single electron memory application, metal-oxide-semiconductor (MOS) structure is essential. However, in our previous work, the surrounding matrix of nanocrystals was amorphous Si. Thus we employed rapid thermal oxidation (RTO) technique to oxidize the amorphous Si. A home-built rapid thermal oxidation system with a halogen lamp array was used with the introduction of 5N-grade pure O_2 during the process. The flow rate of O_2 was 500 sccm and oxidation temperature was kept at 1000 °C with the typical ramp rate of 100 °C/s. The oxidation was conducted by using a multiple heating/cooling process to avoid the overheating problem of our system. Each heating time was 150 s and total heating time was 6000 s.

As a control sample, a piece of *p*-Si wafer was placed near IBAED and EBD samples. After the oxidation, Au dots (1 mm diameter) were evaporated using a shadow mask technique. For backside contact, In–Ga eutectic was used after scratching the surface. After the extensive characterizations, the atomic images of nanocrystals were investigated by high resolution TEM using the same sample.

First, we investigate the PL properties of IBAED and EBD samples after RTO. No substantial difference is found as compared to RTA treated samples in the previous work. For control sample, conventional $C-V$ profile of MOS diode without any hysteresis is observed. By contrast, as shown in Fig. 2(a), we observe a hysteresis whose width is about 0.7 V for the EBD sample indicative of a charging behavior during $C-V$ sweeping. The hysteresis loop direction is counterclockwise. $C-V$ characteristics for the IBAED sample is much more striking. For the IBAED sample, we observe an ultralarge hysteresis in $C-V$ profiles as shown in Fig. 2(b). The width of the hysteresis is over 20 V with 2 V/s sweeping rate. With slower sweeping rate, the hysteresis becomes wider. The flat band voltage shift as a function of sweeping rate is almost symmetrical for forward and reverse sweep directions, such a large $C-V$ hysteresis has not been observed yet. The trap and/or nanocrystal density is estimated by using a simple formula of $(C_{ox}/q)\Delta V_{FB}$ where C_{ox}, q, and ΔV_{FB} are oxide capacitance, elementary charge, and flat band voltage shift, respectively.[10] The estimated trap density is about 2×10^{12} cm^{-2}. The $C-V$ hysteresis in the MOS structure has usually been attributed to slow traps or border traps as extensively discussed by Freetwood *et al.*[11] The border traps can communicate with Si substrate by a tunneling process. The hysteresis occurs because the gate bias at which electrons fill the traps is different from the point at which the electrons leave the traps and/or due to the difference between the capture and emission times of the border traps. However, our large $C-V$ hysteresis is not due to border traps. Border traps are usually generated by x-ray irradiation, avalanche injection, and high field stressing. Our sample preparation condition is far from these conditions. In addition, several reports concerning $C-V$ hysteresis were made for MOS structure containing nanocrystals.[4,12–14] Thus nanocrystals or at least nanocrystal-related traps are responsible for such a large $C-V$ hysteresis. Our hypothesis is supported by TEM observation. As observed in Fig. 1(b), nanocystals are con-

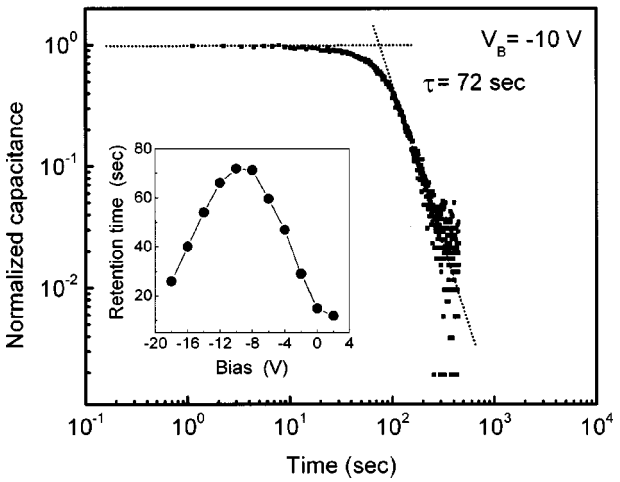

FIG. 3. $C-t$ characteristics of IBAED sample at -10 V after injecting electrons at 20 V for 8 s. The inset shows the retention time variation as a function of bias voltage.

centrated in the localized region close to the Si/SiO_x interface. Due to their high density, nanocrystals appear as a band. The average separation from the interface is about 4 nm.

Ion-beam assistance during deposition should activate adatom migration and thereby enhance nucleation rate (*or* structural relaxation for short range ordering). Then nuclei grow to nanocrystals during subsequent annealing. Spinella *et al.* have reviewed the effect of ion-beam irradiation on the nucleation.[15] The reason why nanocrystals are localized in a narrow region at a certain depth from the Si/SiO_x interface may be a matter of debate. A similar narrow nanocrystal band produced nonintentionally was reported.[16] Such a self-organization of nanocrystals was attributed to collision mixing and near interface oxygen diffusion during ion implantation (75 keV). Those effects create many nucleation sites near the interface. The self-organized band presented in this work may have a different origin since the accelerating voltage in our experiments is much lower.

One plausible explanation may be related to the role of native oxide on the substrate. Such a possibility could be ruled out for several reasons. First, oxide thickness is too thick for native oxide. Second, the separation between nanocrystals and the interface is too regular for the patched nature of native oxide. Another possible reason may be related to the compressive strain present near the interface due to a density mismatch.[17] The strain is relieved by nanocrystal formation at the transition layer. However, the exact reason is not clear at present.

To further elucidate the charging mechanism, $C-t$ measurements were carried out varying biasing condition. After injecting electrons at 20 V for 8 s, gate voltage is suddenly changed to measurement voltage. As observed in Fig. 3, discharging occurs drastically and the distinction between ''charged states'' and ''uncharged states'' is very clear. Such a distinction allows us to evaluate the charge retention time. The evaluated retention time is about 70 s at the measurement voltage of -10 V. Tsybeskov *et al.* reported similar $C-t$ result in their nanocrystal superlattice structure.[13] They discussed their $C-t$ result indicating nondispersive carrier relaxation. A similar discussion was made by Maeda *et al.* in describing tunneling current transient of their MOS diode.[18] However, their structures are well designed for having very narrow nanocrystal size distribution with the aid of sophisticated process steps. Thus the nondispersive carrier relaxation in their reports is not surprising. However, in our IBAED sample, nonintentional design is made in the sense of tunneling barrier thickness and nanocystal size dispersion. Thus our method is attractive by its simplicity. One more interesting observation is about the bias dependence of charge retention behavior (inset in Fig. 3). The longest retention time is obtained at the biasing condition near midgap voltage. Shi *et al.* suggested a model to explain the charge storage characteristics in nanocrystals.[14] According to their model, charges were stored at the deep traps of nanocrystals. The dominant charge-loss process was the direct tunneling of the trapped charges to the interface states. Thus the density of the interface states controls the charge-loss rate. Our result could be explained based on the Shi model. At the midgap voltage, charge tunneling mainly occurs to the interface states near midgap where the density of interface states is lowest. Therefore, the longest retention time will result (i.e., slowest tunneling out of stored charges).

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