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Electron diffraction due to a reflection grating in a conducting wire

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We report on quantum transport in the presence of an electron reflection grating fabricated within a high electron mobility transistor structure. The grating was composed of a periodically corrugated potential wall by which the electron waves are diffracted. The low temperature conductance shows a number of peaks with respect to the gate voltage, which are consistent with the electron diffraction effect and are predicted by the Fraunhofer diffraction condition. © *1997 American Institute of Physics.* [S0003-6951(97)01750-6]

Experimental studies of the conductance properties of semiconductor ring structures evidenced the quantum waveguide effect in the electron propagation.[1,2] Since then, a number of experimental results in the quantum interference transistor structures have been reported; those show the electron interferences associated with the multiple transmissions,[3,4] the multiple reflections,[5] the lateral electron interference,[6] and the electrostatic Aharonov–Bohm effect.[7] On the basis of such results of the phase coherent transports, electron diffraction phenomena as well as the electron interference can appear in a ballistic semiconductor device where the path length of electrons is less than its coherence length.

A single slit quantum diffraction transistor with multiple drains was proposed to have ultrafast extrinsic switching speed and a potential for multi-functionality.[8] However, there were some difficulties in fabrication of sub-micron size multi-drains and in measurements of diffraction currents due to low diffraction efficiency. Recently, electron diffraction by periodic arrays of quantum antidots was investigated by quantum mechanical calculations.[9] It was found that the electron diffraction occurs through multiple channels characterized by the transverse wave vectors that differ from the wave vector of the incident electron by the reciprocal lattice vectors of the periodic arrays as one can expect from the Fraunhofer diffraction of light. So, a reflection type multiple-slit aperture, which is a diffraction grating, is considered to facilitate the device fabrications and to increase the diffraction current for good device performances in the quantum diffraction devices. We have fabricated and characterized a quantum diffraction transistor that has a reflection type grating within a conducting wire structure. In this letter, low temperature conductance properties due to the electron grating in the quantum diffraction transistor are prepared, and the electron diffraction effect is demonstrated.

In our investigation for the electron diffraction, we fabricated a GaAs/AlGaAs-based conducting wire with a grating structure, which has a source, a gate, and two drains as shown in Fig. 1(a). The conducting wire was bent, so that the multiple-slit type reflection grating was planted at the corner of the bent wire. First, the bent conducting path of two-dimensional electron gas (2DEG) has been fabricated by using electron beam lithography and subsequent chemical etching on a modulation-doped $GaAs/Al_xGa_{1-x}As$ ($x=0.3$) heterostructure grown by molecular beam epitaxy. The 2DEG layer is located 650 Å below the top. The width of the conducting path is 1.2 μm, and the distance between the source and drain ohmic contacts is 14 μm in the lithographic length. The heterostructures were wet-etched down to the 2DEG layer to form a well-shaped pathway. Lateral depletion further reduces the conducting width. Second, to form the gate and the grating, electron beam lithography and lift-off technique were employed. The second step defined the Au/Ni gate with the periodically corrugated part for the grating in the sample. The average distance for traveling electrons under the gate is 6.8 μm, and the metal gate covers the whole bent area of the wire. Third, electron beam lithogra-

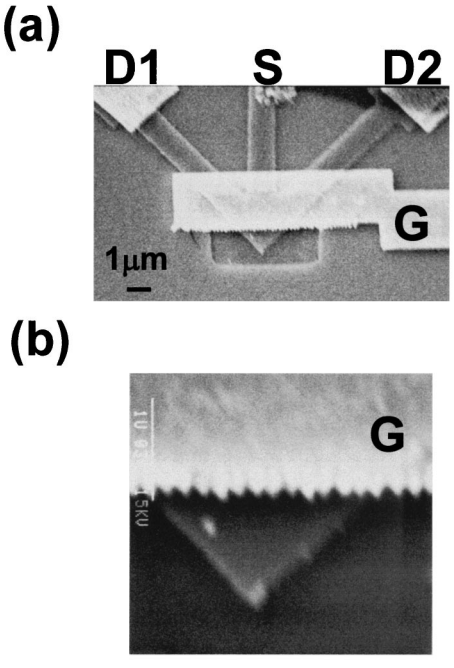

FIG. 1. Scanning electron micrographs of (a) the quantum diffraction transistor and (b) the reflection grating structure.

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phy and the chemically assisted ion beam etching (CAIBE) technique were used to define the etching area and to fabricate the grating structure, respectively. At this moment, we used the corrugated metal gate as an etching mask; the smaller corner area of the 2DEG conducting channel outside of the corrugated gate was etched out. Because CAIBE offers better anisotropic and nonselective etching than other reactive etching techniques, the CAIBE technique is often used in nanostructure fabrication.[10] Finally, a periodically corrugated potential wall, that is a reflection grating, was formed within the bent conducting path. The grating consists of 11 slits in the conducting path, and the slit width and separation are about 70 and 170 nm, respectively [Fig. 1(b)].

The carrier concentration and mobility in the substrate at 1.5 K, as deduced from the Shubnikov–de Haas oscillation measurements in a two-dimensional bar (50×150 μm), were found to be $n_{so}=3.2\times10^{11}$ cm^{-2} and $\mu=5.9\times10^{5}$ cm^2 V^{-1} s^{-1}, respectively. We measured drain current I_{DS}, i.e., conductance σ, versus applied gate voltages V_G at various levels of source-drain voltages V_{DS} by using the lock-in technique at 16 mK. While the drain current was measured at $D1$, the drain $D2$ was grounded and vice versa. The measured values were calibrated under the constant drain-voltage bias mode by considering the effect of conductance change during the gate voltage sweep. We also investigated the temperature dependence of the drain current.

Formation of the sharp potential wall by the grating is very important in the device operation. It is possible that the reactive ion damages at the etched surface create the surface depletion that smooths out the potential modulation of the grating. Even though the diffraction efficiency became small by the smoothing, we could detect the signals for the electron diffraction. Figure 2(a) shows conductance spectra as a function of the gate voltage at $T=16$ mK. The source-drain voltage was fixed at 5 μV to preserve the electron coherence. The pinch-off voltage $V_{\text{pinch-off}}$ of the sample device is -155 mV. It is well known that the conductance in a conventional high electron mobility transistor which has a normal stripe gate is proportional to $V_G-V_{\text{pinch-off}}$. However, we observed oscillatory features which are superposed upon the linear conductance; the oscillations whose intensity is $\sim$25% at $V_G=133$ mV for example are clearly seen. Since these oscillatory behaviors are observed in the grating device and not in the conventional device, we believe that they are manifestations of the electron diffraction effect due to the grating structure. Also, the transconductance versus the gate voltage for $V_{DS}=5$ μV is shown in the inset. Multiple negative transconductance oscillations are clearly seen in the negative slope region of the curve of the source-drain current versus the gate voltage. The pure oscillatory conductances are derived from Fig. 2(a) by subtracting the linear fitting values from the measured conductances. The clear oscillations are exhibited in the gate voltage range, which is shown in Fig. 2(b). Major peaks are represented by bars, which can be attributed to the principal maxima in the diffraction spectra (this attribution of the peaks will be discussed later). Distances between the major peaks increase as the gate voltage increases from the pinch-off voltage, and three minor peaks are shown between the major peaks.

In the conductance measurements by different source-drain voltages from 2.5 μV to 1.2 mV, we have observed a characteristic change in the oscillation intensity. The oscillatory behavior persists up to $V_{DS}=50$ μV, which is shown in Fig. 3. For higher source-drain bias than 50 μV the oscillations start to smear out until they completely disappear at about 1.0 mV. The oscillatory conductances were derived by the same methods used in Fig. 2(b). The characteristic behavior of the oscillatory conductance versus the source-drain voltage is depicted in Fig. 3(b) as $V_G=-133$ mV.

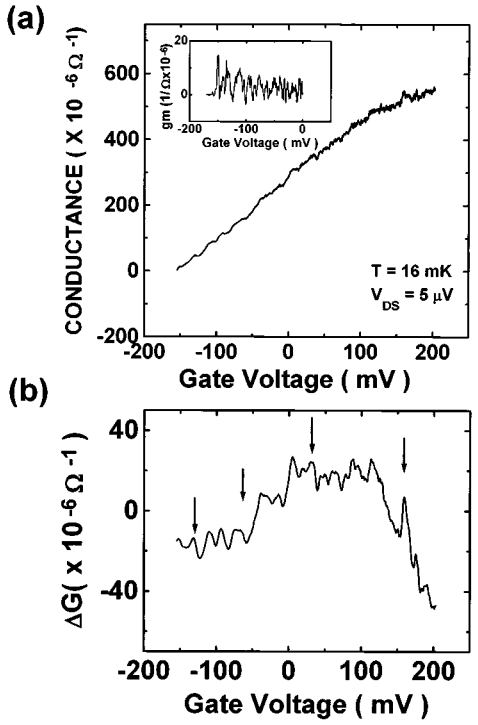

FIG. 2. (a) Conductance spectra vs the applied gate voltages $T=16$ mK. The inset is transconductance $g_m=(\partial I_{DS}/\partial V_G)$ when $V_{DS}=5\mu$V. (b) Changes of the conductance vs the gate voltages. The positions ($\downarrow$) of the major peaks were used in the calculation of the principal diffraction mode index.

It should be noted that the measurements of the temperature dependence of the oscillatory behavior demonstrate how the oscillation intensities vary with the operating temperatures. No oscillation signals with respect to the gate voltage were detected at temperatures above 4.2 K. However, the signals of the clear oscillations appeared below 0.3 K whose intensities were almost constant down to 17 mK. With respect to the correlation energy, both results of 0.3 K in the operating temperature and 50 μV in the source-drain voltage well match. This characteristic behavior of the oscillatory conductance in the operating temperatures as well as in the source-drain voltages agree well with the results of the typical electron interference effect.[11]

The elastic scattering length is deduced to be 6 μm by using the simple approximation; $l_e=h\mu/e\lambda_F$. Because the elastic scattering length is comparable to the gate length, the electron transport under the gate is quasi-ballistic. The incident and diffracted electron waves can be strictly described by plane waves in the ballistic transport regime, so that the Fraunhofer diffraction mechanism is rigorously valid in the sample device. On the other hand, the gate voltage alters the electron density in the device, and the Fermi wavelength is

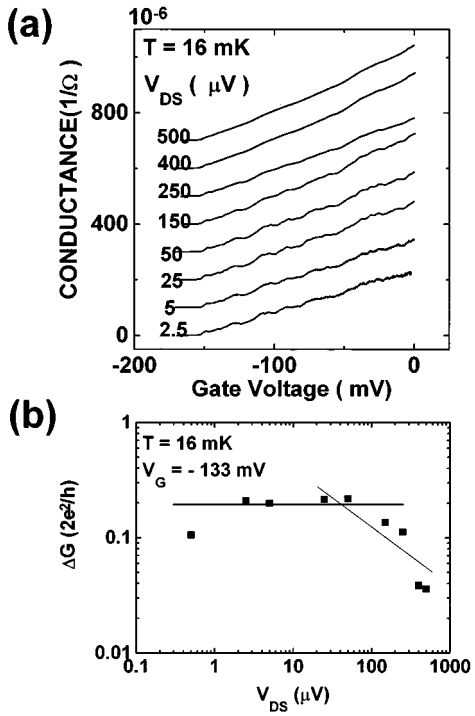

FIG. 3. (a) Plots of the conductances as a function of the gate voltage at the several source-drain voltages $T=16$ mK. The conductances are successively shifted by 100 μmho from the bottom curve. (b) The oscillation intensity of the conductance vs the source-drain voltage when $V_G=-133$ mV.

changed according to $\lambda_F=\sqrt{2\pi/n_s}$ (n_s is the two-dimensional electron density). Therefore, we observe the diffraction pattern with respect to the gate voltage instead of the spatial diffraction pattern in this quantum diffraction transistor. When we assume the slowly varying envelope function in the Fraunhofer diffraction intensity, the diffraction formula yields the principal maximum condition: $m\lambda=b(\sin\theta_I+\sin\theta_D)$, where m is the order of diffraction, λ is the Fermi wavelength, b is the slit separation, θ_I is the incident angle, and θ_D is the diffraction angle. In the sample structures, the incident and diffraction angles are fixed at 0° and 45°, respectively.

In Fig. 2(b), the conductance maxima represented by bars are seen to coincide with the peak positions expected from the diffraction condition. In order to verify that the observed oscillations are due to the electron diffraction effect, the diffraction mode indices, $m=b/\sqrt{2}\lambda(V_G)$, are calculated from the peak positions in the gate voltage; $V_G=-133$, -66, 30, and 161 mV. The results are plotted versus integer numbers in Fig. 4, where the calculated index numbers for the oscillation peaks agree well with the integer numbers. A linear approximation for the two-dimensional electron density depending on the gate voltage, $n_s(V_G)=n_{\rm so}(V_G+0.155)/0.155$, was used in the calculation of the Fermi wavelength.

It should be mentioned that we may consider the multiple transmission effect (that is, the Fabry–Perot type interference) due to the periodically corrugated potential wall in the one-dimensional transport, which leads to the maximum intensity condition; $m\lambda=2b$. However the calculated peak positions from the multiple transmission effect do not agree with the measured values. Moreover, we observed three secondary maxima between the principal maxima which can be explained by the Fraunhofer diffraction effect [see Fig. 2(b)]. We believe that the surface depletion at the side wall of the conducting wire reduces the actual number of the slits in the sample devices to five.

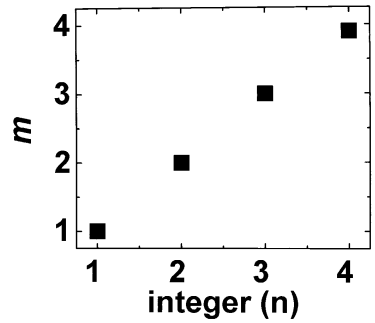

FIG. 4. Calculated principal diffraction mode indices, m, $m=b/\sqrt{2}\lambda(V_G)$, vs integer number n.

In conclusion, we have investigated the electrical transport properties of a GaAs/Al_xGa_{1-x}As-based quantum diffraction transistor which has an electron reflection grating in the conducting wire. The oscillatory behaviors of the source-drain conductance with respect to the gate voltage have been observed. We find that these phenomena are well explained by electron diffraction effect, and the conductance oscillations are predicted by Fraunhofer diffraction condition.

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