Reliability Study of CMOS FinFETs

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Abstract

Hot-carrier and oxide reliability of CMOS FinFETs with 2.1nm-thick gate-SiO_2 were investigated. It was found that hot-carrier immunity improves as the fin width (body thickness) decreases, which facilitates gate-length scaling, while it is degraded at elevated temperature due to the self-heating effect. High values of Q_{BD} are achieved for devices with very small gate area. A post-fin-etch hydrogen anneal is helpful for improving hot-carrier immunity and Q_{BD}.

Introduction

The FinFET offers the superior scalability of the double-gate MOSFET structure with a conventional process flow; hence, it is attractive for scaling CMOS technology to sub-10nm gate lengths. Several groups have recently reported on the fabrication and performance of CMOS FinFET devices [1]-[4]. In this work, the reliability of FD-SOI CMOS FinFETs is investigated. Hot-carrier reliability for various bias stress conditions, device dimensions, and substrate temperature are reported. Gate oxide charge-to-breakdown (Q_{BD}) distributions are also presented.

Experiment

Fabrication process details for the FinFETs used in this work have already been reported elsewhere [1][5]. Two different types of FinFETs were investigated: P+ poly-$Si_{0.6}Ge_{0.4}$ gated FinFETs with gate lengths down to 23nm, fabricated using e-beam lithography (Group I); and N+ poly-Si gated FinFETs of gate length 120nm, fabricated using spacer lithography (Group II). In Group II, one wafer was annealed in hydrogen (5min @ 900°C and 1atm) to smoothen the fin sidewall surfaces prior to gate oxidation [5]. The gate dielectric in all devices was 2.1nm thermally grown SiO_2. For Group I, significant boron penetration through the gate oxide into the channel/fin resulted in a high threshold voltage (V_T=0.8V) and gate-underlapped structure for the n-channel FinFETs. (The p-channel FinFETs have a conventional gate-overlapped structure.) This work is primarily focused on the reliability of sub-100nm L_g FinFETs (Group I). Only the effects of post-fin-etch annealing in H_2 were studied using the longer-channel devices from Group II.

First, the worst-case bias condition for hot-carrier stress was determined, for V_d=1.8V. The V_T shift was found to be larger when the gate voltage was equal to the drain voltage (V_g=V_d), compared to V_g=V_d/2. Degradation in device performance parameters under V_g=V_d=1.8V stress was then tracked over time, for FinFETs of various gate lengths and fin widths (W_{fin}), and several substrate temperatures. Q_{BD} distributions were also obtained for FinFETs of various sizes.

Results

In a double-gate n-channel MOSFET, energetic electrons generated by impact ionization near the drain can become trapped at the gate-oxide interface or in the gate oxide to cause an increase in V_T, while the generated holes flow to the region of lowest potential (*i.e.* the source), as shown in **Fig. 1**. For gate-underlapped n-channel FinFETs, holes can become trapped at the gate-oxide interface in this region, causing a decrease in V_T. Thus, electron trapping and hole trapping have opposite effects on V_T. For fixed V_g-V_T=1V, the dominant V_T-shift mechanism depends on V_d. Hole trapping is dominant for $V_d \leq 1.8$V, so that the magnitude of V_T decreases with increasing stress time, while electron trapping becomes dominant at higher values of V_d, so that V_T eventually increases with increasing stress time (**Fig. 2**). For gate-overlapped p-channel FinFETs, the magnitude of V_T decreases consistently with increasing $|V_d|$ (**Fig. 3**), similar to the behavior of bulk-Si PMOSFETs.

The magnitude of the V_T shift decreases with increasing channel length (**Fig. 4 and Fig. 5**) due to the decreasing lateral electric field; however it increases with increasing fin width, as shown in **Fig. 6 and Fig. 7.** To explain this dependence on W_{fin}, the electron-hole pair generation rate (G) – due to impact ionization – and electron temperature (T_e) profile in an n-channel double-gate MOSFET were studied using the device simulator MEDICI [6]. The gate is assumed to be perfectly aligned (zero overlap) to the abrupt source/drain (S/D) junctions, and its doping concentration is $2\times10^{20}cm^{-3}$. The simulation results (**Figures 8-11**) show that both T_e and G increase with increasing W_{fin}, which is consistent with the reliability measurement data. **Figs. 8** and **9** show that the potential profile becomes increasingly "one-dimensional" as the

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body thickness decreases. In the thicker body case, hot electrons are more strongly driven towards the gate oxide by the 2D curvature of the potential. The paths of generated hot carriers are indicated schematically by the bold arrows in **Figs. 8** and **9.** Thus, hot-carrier immunity is improved by thinning the body of a double-gate MOSFET, which also improves short-channel effects. The simulations show that G is insensitive to channel (fin) doping concentration (**Fig. 11**).

Degradation of the drain saturation current (I_{dsat}) is observed after swapping the source and drain during device measurement after each stress interval, as shown in **Fig. 12**. The degradation is more significant in an n-channel FinFET (n-FinFET) than a p-channel FinFET (p-FinFET) because the n-FinFET has an underlapped-gate structure and p-FinFET has an overlapped-gate structure. More hot carriers are trapped in the underlapped region. The trapped electrons at the drain, which becomes the source after the swapping, suppress the inversion charge. They result in an increase in V_T, hence a decrease in I_{dsat}. In the n-FinFET, I_{dsat} is degraded 4.6% for W_{fin} =18nm and 24% for W_{fin} =42nm. This proves that more carriers are trapped for a thick body as compared with a thin body, consistent with the simulation results shown in **Fig. 8** and **Fig. 9**, and also consistent with the improved hot-carrier immunity observed for a thinner body.

Hot-carrier DC lifetime is plotted in **Fig. 13** and **Fig. 14**. The criteria for failure used for these plots are 10% change of V_T, 10% change of g_m (transconductance), and 10% change of I_{dsat}. Ref. 3 also reports hot-carrier DC lifetime results for FinFETs. However, the results presented here are not directly comparable to the previously reported results because the oxide thicknesses are different and the failure criteria were not noted. The lifetime is improved slightly for devices that received a post-fin-etch anneal in H_2 (**Fig. 14**). These results indicate that FinFETs should be able to meet the 10-yr lifetime requirement for normal operating conditions, if W_{fin} is sufficiently small. The effect of substrate temperature during stress is shown in **Fig. 15** and **Fig. 16.** Ordinarily, G increases when the temperature is decreased, because of increased mean free path [7]. Thus, worse degradation (due to electron trapping) is seen at –50°C compared to 30°C. At elevated temperatures, self-heating effects are significant in SOI MOSFETs and can enhance G [8]. Thus, we also find worse degradation (due to electron trapping) at 120°C *vs.* 30°C.

The gate voltage was linearly ramped for charge-to-breakdown (Q_{BD}) measurements. The area of a single-fin device is $7.11 \times 10^{-3} \mu m^2$ (L_g=79nm and fin height=45nm). The measured Q_{BD} is approximately $10^4 C/cm^2$ for these FinFETs with extremely small gate area (**Fig. 17**). Degraeve *et al.* [9] reported that Q_{BD} becomes a strong function of the channel area as the gate-oxide thickness decreases. A similar trend (increasing Q_{BD} as the channel area decreases) is also observed in this work, as shown in **Fig. 17** and **Fig. 18**. Higher and more uniform Q_{BD} is achieved when a post-fin-etch anneal in H_2 is employed (**Fig. 18**).

Summary

The reliability of CMOS FinFETs has been studied. Hot-carrier immunity is found to improve with decreasing W_{fin}, and is degraded at high substrate temperature (120°C) due to the self-heating effect, as well as at low substrate temperature (-50°C). High values of Q_{BD} (>10^4 C/cm^2) are achieved for 2.1nm gate oxide, for very small gate area. Hydrogen annealing to smoothen the fin sidewalls is effective for improving both hot-carrier lifetime and Q_{BD}.

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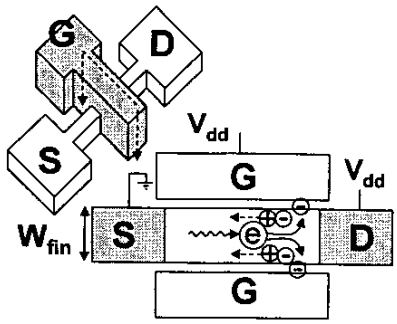

Fig. 1 Schematic of FinFET, and carrier movement in an n-channel double-gate MOSFET under hot-carrier stress bias conditions.

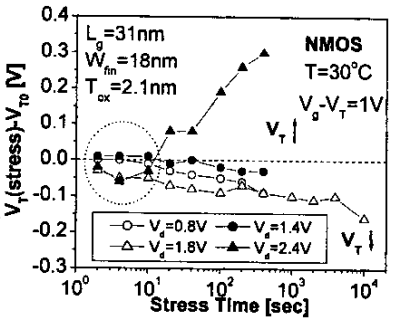

Fig. 2 NMOS FinFET (gate-underlapped structure) V_T shift *vs.* stress time for different drain bias stress voltages. Electron trapping eventually dominates for very high V_d.

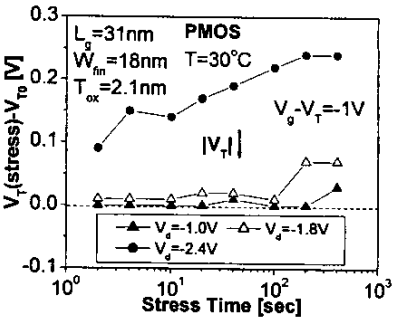

Fig. 3 PMOS FinFET (gate-overlapped structure) V_T shift *vs.* stress time for different drain bias stress voltages.

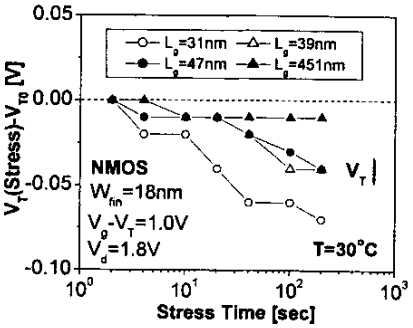

Fig. 4 NMOS V_T shift *vs.* stress time for different gate lengths. Longer-channel devices show better hot-carrier immunity due to the reduced lateral electric field.

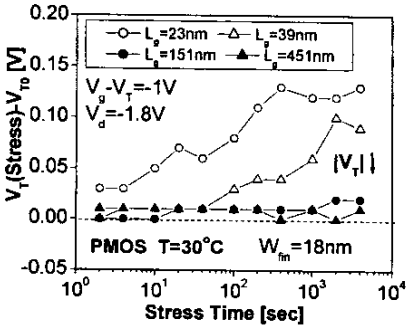

Fig. 5 PMOS V_T shift *vs.* stress time for different gate lengths. Longer-channel devices show better hot-carrier immunity due to the reduced lateral electric field.

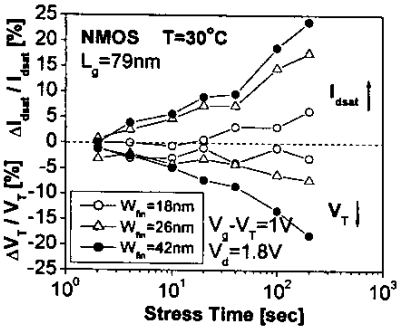

Fig. 6 Relative shifts in V_T and I_{dsat} for NMOS FinFETs (gate-underlapped structure) *vs.* stress time, for different fin widths. Better hot-carrier immunity is achieved with a narrower fin.

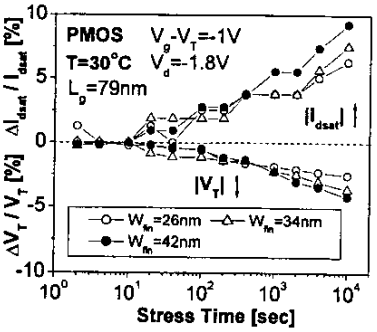

Fig. 7 Relative shifts in V_T and I_{dsat} for PMOS FinFETs (gate-overlapped structure) *vs.* stress time, for different fin widths. Better hot-carrier immunity is achieved with a narrower fin.

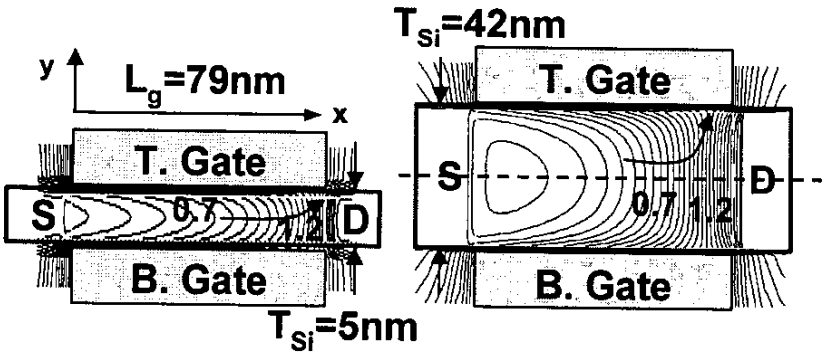

Fig. 8 Simulated 2-D potential profile in a double-gate MOSFET with L_g = 79 and T_{Si} = 5 nm. The gate is perfectly aligned (zero overlap) to the abrupt S/D junctions ($N_{S/D}$=2x10^{20}cm^3). The potential lines are more straight than for the thick-body device at the drain side.

Fig. 9 Simulated 2-D potential profile in a double-gate MOSFET with L_g = 79 and T_{Si} = 42 nm (V_g=V_d=1.2V). The highest potential gradient is located well under the gate, in contrast with the case of the thinner-body structure in Fig. 8.

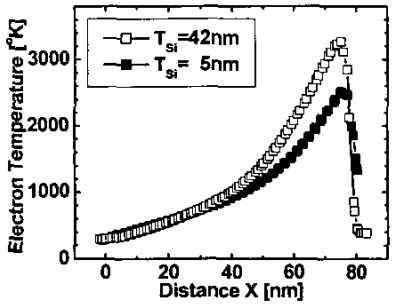

Fig. 10 Comparison of the electron temperature *vs.* distance along the center of the double-gate MOSFET body, for thin *vs.* thick body.

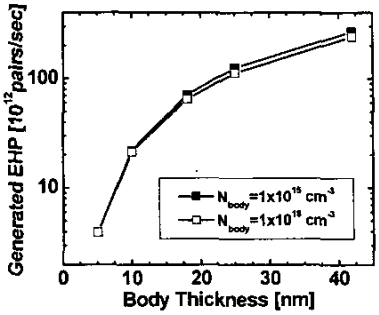

Fig. 11 Simulated impact ionization induced electron-hole-pair generation rate in a double-gate MOSFET (L_g=79nm) *vs.* body thickness. The impact ionization rate is reduced by thinning the body.

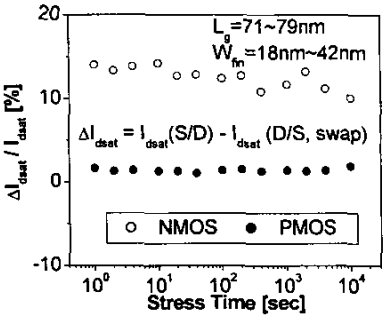

Fig. 12 V_T shift measured after each stress interval. $|I_{dsat}|$ is decreased for measurement with swapped S/D.

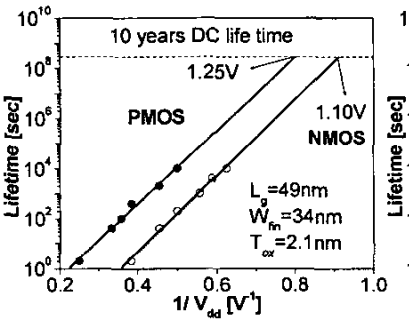

Fig. 13 Hot-carrier DC lifetime for CMOS FinFETs (P+ poly-$Si_{0.6}Ge_{0.4}$ gate, no hydrogen anneal after fin etch).

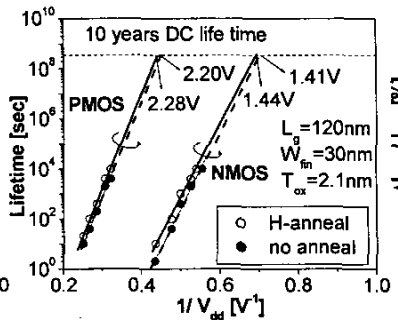

Fig. 14 Hot-carrier DC lifetime for CMOS FinFETs (N+ poly-Si gate), showing the benefit of a hydrogen anneal (5' @ 900°C) after fin etch.

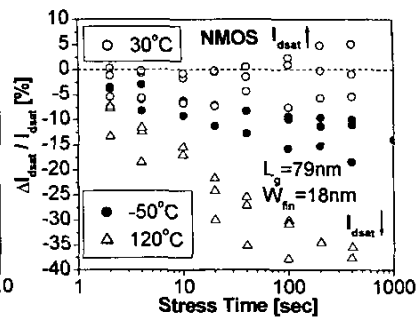

Fig. 15 Fig. 15 Effect of substrate temperature on relative I_{dsat} shift with stress time, for NMOS FinFETs.

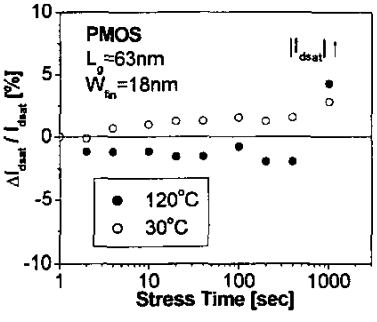

Fig. 16 Effect of substrate temperature on relative I_{dsat} shift with stress time, for PMOS FinFETs.

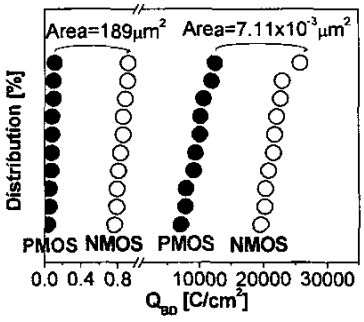

Fig. 17 Q_{BD} distributions for CMOS FinFETs (P+ poly-$Si_{0.6}Ge_{0.4}$ gate, no hydrogen anneal after fin etch). Q_{BD} is extremely high for very small gate areas.

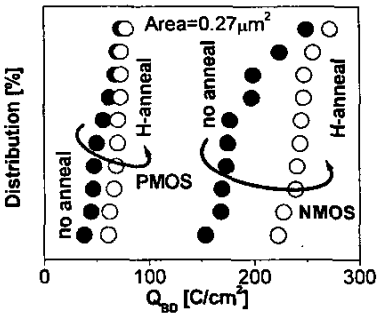

Fig. 18 Q_{BD} distributions for CMOS FinFETs (N+ poly-Si gate). Q_{BD} is higher and more tightly distributed for devices which received a post-fin-etch anneal in hydrogen to smoothen the fin sidewall surfaces.