A High IIP2 Direct-Conversion Receiver Using Even-Harmonic Reduction Technique for Cellular CDMA/PCS/GPS Applications

Myung-Woon Hwang, *Member, IEEE*, Gyu-Hyeong Cho, *Member, IEEE*, Seungyup Yoo, Jeong-Cheol Lee, Sungmin Ock, Sunki Min, Sang-Hoon Lee, Sungho Beck, Kyoohyun Lim, Sangwoo Han, and Joonsuk Lee

***Abstract*—A high IIP2 direct-conversion receiver for cellular CDMA/PCS/GPS has been developed in a 0.35 μm SiGe BiCMOS process. This receiver consists of a RF front-end chip and a base-band chip. The RF front-end chip includes three LNAs, three mixer cores with a common output stage, and LO distribution blocks. The base-band chip includes a channel selection filter, an output buffer, and a dc calibration block. To achieve high IIP2 performance, an even-harmonic reduction technique is proposed based on a simplified analysis of second-order intermodulation. A 40-dB improvement of the IIP2 performance is accomplished by this technique, which reduces sensitivity to operating conditions and to output load mismatches. This receiver also attains high IIP3 and a low-noise figure. Measurement results show 71 dBm IIP2, −1.3 dBm IIP3, and 2.4 dB NF for Cellular CDMA; 68 dBm IIP2, −3.7 dBm IIP3, and 2.9 dB NF for PCS; and 26 dBm IIP2 −30 dBm IIP3, and 2 dB NF for GPS.**

***Index Terms*—BiCMOS analog integrated circuits, filter, harmonic analysis, intermodulation distortion, low-noise amplifier, mixers, receivers.**

I. Introduction

INCREASING demand for smaller and cheaper multiband/multimode mobile handsets has motivated the development of a direct-conversion receivers, which eliminate the need for bulky external IF SAW filters and an IF synthesizer. However, several challenging issues appear in a direct conversion receiver compared to a heterodyne receiver [1], [2]. One of the most important design issues is the second-order intermodulation around the dc, which can be removed by channel selection IF SAW filters in the heterodyne architecture. The most dominant source of second-order intermodulation in a direct-conversion receiver is the downconversion mixer [3]. A conventionally low-noise amplifier (LNA) has a dc-decoupling structure for output matching. Baseband filters and variable gain amplifiers (VGA) both have local feedbacks in order to reduce distortion. Both the dc-decoupling structure and the feedback circuitry reduce the second-order intermodulation.

Generally a double-balanced Gilbert cell type mixer with active transconductance is used for a direct-conversion receiver. In a perfectly balanced case, the even-order distortion caused by device nonlinearity would not appear in the signal path. In a practical situation where a load mismatch and a LO switching pair asymmetry exist, the even-order intermodulation still distorts the signal flow. The second-order intermodulation (IM2) in a balanced mixer signal is composed of two parts; differential-mode and common-mode products. The former is mainly generated by the LO switching pair asymmetry. The latter is mostly generated by the nonlinearity of the active transconductance stages and output load mismatches due to the physical limitations of the asymmetry and the processing tolerances of the fabrication technology [4].

Many techniques utilized to improve IIP2 performance have been investigated. These include using a careful layout, reducing the nonlinearity of the active transconductance by emitter degeneration or harmonic termination, and trimming or intentionally imputing some mismatches to the LO switching pair and the output load [4], [5]. However, the IIP2 of these mixers is sensitive to load mismatch and operating conditions such as supply voltage, temperature, and fabricated location, as well as other conditions, when it comes to performance.

In this paper, a high IIP2 direct-conversion receiver for cellular CDMA/PCS/GPS applications is presented [6]. The developed two-chip solution achieves high IIP2 and IIP3 with a low-noise figure. To enhance IIP2 performance, an even-harmonic reduction technique is introduced based on a simplified analysis of a second-order intermodulation.

This paper is organized as follows: Section II covers the proposed receiver architecture and the simplified block explanation. The receiver requirement analysis is described in Section III; while the IIP2-enhancing technique using an even-harmonic reduction loop is outlined in Section IV. The detail building blocks are described in Section V; the measurement results are presented in Section VI and the paper is summarized in Section VII.

II. System Architecture

Fig. 1 shows the proposed direct-conversion receiver architecture for cellular CDMA, PCS, and GPS applications. This multiband/multimode receiver architecture is composed of two

Manuscript received October 18, 2004; revised October 22, 2005. First published May 28, 2008; current version published October 29, 2008. This paper was recommended by Associate Editor W. A. Serdijn.

M.-W. Hwang is with the Future communications IC (FCI) Inc., Sungnam, 463-020 Korea. He is also with the Circuit and System Lab, Korea Advanced Institute of Science and Technology, Deajon, 305-701 Korea (e-mail: hmw@fci.co.kr).

G.-H. Cho is with the Circuit and System Lab, Korea Advanced Institute of Science and Technology, Deajon, 305-701 Korea.

S. Yoo, J.-C. Lee, S. Ock, S. Min, S.-H. Lee, S. Beck, K. Lim, S. Han and J. Lee are with Future Communications IC (FCI) Inc., Sungnam, 463-020 Korea.

Digital Object Identifier 10.1109/TCSI.2008.925960

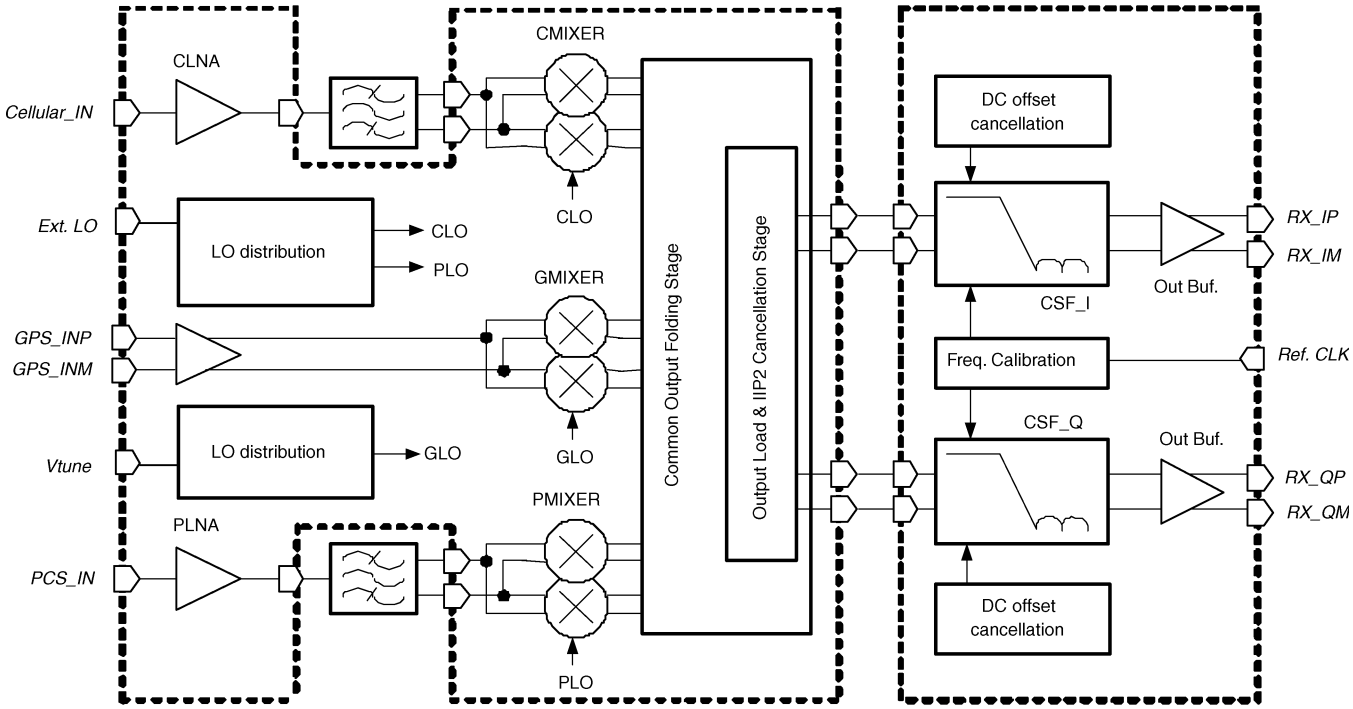

Fig. 1. The proposed cellular CDMA/PCS/GPS direct conversion receiver architecture.

chips; the first being is a RF front-end chip and the second is a baseband chip.

The RF front-end chip consists of three low-noise amplifiers, three mixer cores, a common output folding stage, output loads and IM2 cancellation stage, and LO distribution blocks. There are two on-chip single-ended low-noise amplifiers for the cellular CDMA and PCS bands, which drive the external RF SAW filter. A differential topology is used for the GPS LNA, which is internally connected to a mixer core using internal spiral inductors. The mixer cores for all three bands have a differential input structure for high IIP2 and a low-noise figure. As all three bands do not operate simultaneously, the mixer cores share a common mixer output folding stage as well as the output load and IM2 cancellation stage to reduce the chip area. To obtain high IIP2 and immunity to unwanted output load mismatches, the common output folding stage and the output load and IM2 cancellation stage are used. An IIP2 calibration circuit is included in the output load and IM2 cancellation stage to reject the effect of LO mismatches. The LO distribution block completely integrates a quadrature signal generation block and a frequency translation block.

The base-band chip consists of two fifth-order active-*RC* elliptic channel selection filters, a frequency calibration logic block, a dc offset cancellation block, and an output buffer. These channel selection filters are designed so as not to be saturated by large out-band jammer signals while allowing the desired in-band signal to have a proper gain. The frequency calibration logic block compensates for process variation and mismatches. The dc offset cancellation block causes a small SNR degradation, but is used for the rejection of LO leakage and device mismatch effects. The output buffer drives the external analog-to-digital converter (ADC).

III. System Requirement Analysis

Many published papers describe the block level specification extraction methods from a system standard, such as for IS-98, in a super-heterodyne system. In the direct-conversion system, most of the specifications are similar to those of a super-heterodyne system including the noise figure (NF), power gain, IIP3, and phase noise, among others. The sole difference is the second-order harmonic distortion specification. The NF, IIP3, and IIP2 requirement analysis to satisfy the system standards is described in [7] and [8].

A. Noise Figure (NF)

The receiver noise figure is calculated from the standard's reference sensitivity test. Assuming that E_b/N_t is 6 dB including an additional 1.5 dB margin for a FER of 0.005% and the $loss_{RF}$ is 3 dB, NF is easily calculated from standard

$$\begin{aligned} NF_{\text{chain}} \leq\, & I_{or} + \frac{\text{TrafficE}_\text{c}}{\text{I}_\text{or}} - \left(\frac{E_b}{N_t}\right) + G_p \\ & - 10\log_{10}(k \cdot T_0 \cdot BW) \cdot loss_{RF} \\ \leq\, & 5.4\,\text{dB} \end{aligned}$$

where I_{or} is the reference sensitivity level (-104 dBm), Traffic E_c/I_{or} is the ratio of the desired channel power to the reference signal power, E_b/N_t is signal-to-noise-and-interference ratio, G_p is the processing gain, k is Boltzman's constant, T_0 is the standard noise temperature, BW is the system channel bandwidth, and $loss_{\text{RF}}$ is the loss from the antenna to the RF input.

B. Third-Order Input Intercept Point (IIP3)

The third-order input intercept point (IIP3) is determined by an intermodulation spurious response attenuation test. As-

suming that P_{NI}/P_N is 3 dB and P_{jammer} is -43 dBm, the required IIP3 is as follows:

$$\begin{aligned}\text{IIP3}_{\text{chain}} &\geq \frac{3}{2}\cdot P_{\text{jammer}} - \frac{1}{2}\cdot\frac{P_{NI}}{P_N} - \frac{1}{2} \\ &\quad\cdot\left[I_{or} + \frac{\text{Traffic E}_\text{c}}{I_{or}} - \left(\frac{E_b}{N_t}\right) + G_p\right] \\ &\geq -12.2\,\text{dBm} \end{aligned} \tag{1}$$

where Ior is the intermodulation spurious response test level (-101 dBm), P_{NI}/P_N is the ratio of the power of thermal noise and distortion to the power of thermal noise, and P_{jammer} is the interfering CW power.

C. Second-Order Input Intercept Point (IIP2)

The second-order input intercept point (IIP2) is determined by the jammer test. Assuming that P_{NI}/P_N is 3 dB and P_{jammer} is -18 dBm, which is the strongest power in an intermodulation spurious response attenuation test, IIP2 is calculated as

$$\begin{aligned}\text{IIP2}_{\text{chain}} &\geq 2\cdot P_{\text{jammer}} - \frac{P_{NI}}{P_N} \\ &\quad - \left[I_{or} + \frac{\text{Traffic E}_\text{c}}{I_{or}} - \left(\frac{E_b}{N_t}\right) + G_p\right] \\ &\geq 62.6\,\text{dBm} \end{aligned} \tag{2}$$

where I_{or} is the AM suppression test level (-101 dBm), P_{NI}/P_N is the ratio of the power of thermal noise and distortion to the power of thermal noise, and P_{jammer} is the AM jammer power. Assuming the gain of the LNAs (G_{LNA}) is 15 dB and the loss of the RF SAW filter (L_{saw}) is 2 dB, the required mixer IIP2 is given by

$$\text{IIP2}_{\text{mixer}} = IIP2_{\text{chain}} + G_{\text{LNA}} - L_{\text{saw}} \geq 75.6\,\text{dBm}. \tag{3}$$

This number for an IIP2 value is unachievable in a normal active mixer. A well-biased double-balanced Gilbert cell mixer shows approximately 40∼50 dBm IIP2 in a BiCMOS 0.35 μm process. A IIP2 value can be interpreted as a measure of mismatch between differential paths. Fortunately, any unbalanced factor within the mixer can be improved by adjusting the output loads. Only a high accuracy of the controllable mixer load can give a high enough IIP2, which is not suitable for a realistic implementation. Here even harmonic reduction loop relaxes the load accuracy with minimal hardware addition. As a result, this combined approach makes IIP2 immune to a device mismatch.

IV. Proposed IIP2-Enhancing Technique Using an Even-Harmonic Reduction Loop

In the double-balanced mixer structure, the output second-order intermodulations at each single-ended outputs are derived as follows [6]:

$$\begin{aligned} V_{\text{IM2.out.single+}} &= (I_{\text{IM2.c}} + I_{\text{IM2.d}}/2)\cdot(R + \Delta R/2) \\ V_{\text{IM2.out.single-}} &= (I_{\text{IM2.c}} - I_{\text{IM2.d}}/2)\cdot(R - \Delta R/2) \end{aligned} \tag{4}$$

where $I_{\text{IM2.c}}$ and $I_{\text{IM2.d}}$ are the common and differential output second-order intermodulations, respectively, and R and ΔR are the output load resistor and the mismatch of the output load, respectively. Assuming that $I_{\text{IIM2.c}} \gg I_{\text{IM2.d}}$ and $R \gg \Delta R$, the second-order intermodulations at differential outputs and single-ended outputs are simplified as

$$\begin{aligned} V_{\text{IM2.out.diff}} &= I_{\text{IM2.c}}\cdot\Delta + I_{\text{IM2.d}}\cdot R \\ V_{\text{IM2.out.single}} &\approx I_{\text{IM2.c}}\cdot R. \end{aligned} \tag{5}$$

As shown in (6), the output intermodulations at differential outputs rely on both asymmetries and nonlinearities, while those at a single-ended output rely solely on nonlinearities. Thus, a second-order intermodulation at a single-ended output ($V_{\text{IM2.out.single}}$) can be predicted by calculation and simulation. In order to diminish the common-mode portion in (6), the proposed method is to reduce IIM2.c using an active even-harmonic reduction feedback loop. IIM2.c can be reduced without deteriorating the fundamental output using an even-harmonic reduction loop. The proposed even-harmonic reduction loop makes the opposite current of IIM2.c after sensing it, using an active feedback loop. Using the proposed method, (6) is calculated as

$$\begin{aligned} V_{\text{IM2.out.diff}} &= I_{\text{IM2.c}}/T\cdot\Delta + I_{\text{IM2.d}}\cdot R \\ V_{\text{IM2.out.single}} &= I_{\text{IM2.c}}/T\cdot R + I_{\text{IM2.d}}/2\cdot R \end{aligned} \tag{6}$$

where T is the feedback loop gain of the even harmonics. Assuming the loop gain is very large, the equation is simplified as

$$\begin{aligned} V_{\text{IM2.out.diff}} &\approx I_{\text{IM2.d}}\cdot R \\ V_{\text{IM2.out.single}} &\approx I_{\text{IM2.d}}/2\cdot R. \end{aligned} \tag{7}$$

As shown earlier, the second-order intermodulation products in the mixer with the proposed active even-harmonic reduction loop is estimated to be chiefly determined by the differential mode IM2, which is caused by the asymmetry of the LO switching pair rather than by the nonlinearity of the active transconductance stages and the output load mismatch. However, IIP2 is to some extent affected by the asymmetries in a practical situation because the loop gain cannot be maximized due to the stability problem and the limited gain bandwidth (GBW).

V. Circuit Design

A. Downconversion Mixers

A simplified folded mixer schematic for an I-channel of one band is shown in Fig. 2. The downconversion mixers have three mixer cores, which are designed for each band. They also have a common output folding stage. Each mixer core output is combined at the current mode. The mixer core has a double-balanced structure with an active transconductance stage including inductor degeneration and a LO switching core stage. The active transconductance stage has inductor degeneration for high IIP3 and a low noise, and a tail current source for high IIP2. The LO switching core stage is carefully designed and drawn because the LO switching core mismatch effects the IIP2. To reduce the second-order distortion in the LO switching core, a bipolar transistor is suitable as the nonideal duty cycle error effect of the LO signal is minimized, the device size is suitable for obtaining a matching requirement, and the layout is drawn

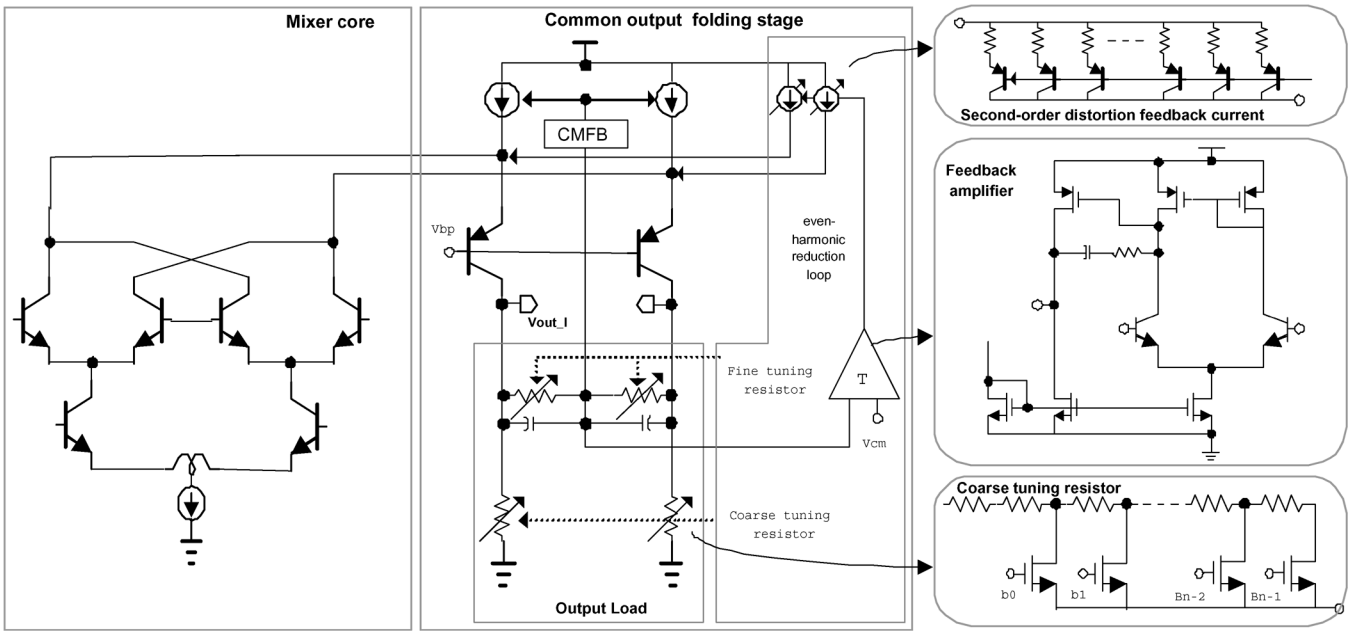

Fig. 2. Simplified folded mixer schematic with an IM2 cancellation stage using an even-harmonic reduction technique for an I-channel of one band.

with a common-centroid structure. Bipolar transistors also provide lower flicker noise; thus, the LO switching core and the folding stage transistor should be a bipolar transistor to achieve low-noise figure.

B. Common Output Folding Stage

The common output stage consists of an output load, an IM2 cancellation stage, and common-mode feedback (CMFB). The common output stage has a current folding structure for guaranteeing a suitable operation at a low supply voltage and a low-noise operation. To reduce the second-order intermodulation, the exact even harmonics should be sensed at the output load. So the output load is composed of digitally controlled resistor arrays, which have the coarse tuning and fine tuning as shown in Fig. 2. The fine-tuning resistor array supports exact even-harmonic sensing by adjusting the fine-tuning resistor that has 0.5%—resolution 4-bit arrays. This adjustment of the fine-tuning resistor array compensates for the systematic errors of the even harmonic sensing because of the nonsymmetry layout effect. The coarse-tuning resistor array supports the mixer gain calibration so that the mixer is not saturated by a large jammer signal, and it has 4%—resolution 4-bit arrays. The IM2 cancellation stage reduces the second-order intermodulation using an even-harmonic reduction loop. The second-order intermodulation at the output load is amplified by the feedback amplifier and the compensation current is generated by the second order distortion feedback current block. This compensation performance is determined by the loop gain and loop bandwidth of this even-harmonic reduction loop. Thus, this even harmonic reduction loop should have a large loop gain and a wide loop bandwidth. To enhance the loop bandwidth and loop gain, the second-order distortion feedback current block uses the high-speed PNP bipolar, and the feedback amplifier has a wide GBW. The CMFB is designed to stabilize the output dc voltage. The CMFB loop should have a low bandwidth.

C. LO Distribution

The LO distribution circuits are designed to make performances insensitive to LO power for cellular CDMA, PCS, and GPS bands, as shown in Fig. 3. The LO distribution of cellular CDMA consists of an external LO buffer that makes a differential LO signal from a single external LO input, and a divided-by-2 circuit for obtaining 4-phase LO signal. The LO distribution of PCS is composed of an external LO buffer, a second-order poly-phase filter (PPF) that receivies a 4-phase LO signal, and a PPF buffer for driving the LO switching cores of the PCS mixer. The LO distribution of GPS has an internal VCO with a 3.2-GHz operating frequency, a VCO buffer for isolating the VCO from the divided-by-2 circuit and achieving a stable oscillation, and a divided-by-2 circuit for supplying the 4-phase LO signals. The GPS VCO utilzes cross-coupled NMOS and PMOS cores for negative trans-conductance to reduce the phase noise and utilzes a large-sized NMOS as tail current source for operating on the current steering mode.

D. Low-Noise Amplifier (LNA)

Fig. 4 is a simplified schematic of the cellular CDMA LNA (CLNA) in which the CLNA supports the three gain modes of high/mid/bypass modes. The principal circuit structure of the CLNA consists of the main amplifying stage, an additional gain stage and a bias circuit. For the optimal performance of the main amplifying stage, the device size and the collector current density of main transistor Q1 initially must be carefully chosen using the contours of gain, NF and IIP3 as a function of the device size and the collector current density [10]. The degeneration inductor L3 in the emitter of Q1, and the external RF choke L1 for the base biasing of Q1 are also used for high IIP3. L3 can tune up the IIP3 of the LNA by tradingoff input impedance, gain and IIP3. L1 enhances the linearity of the LNA with an appropriated biasing circuit because the input source

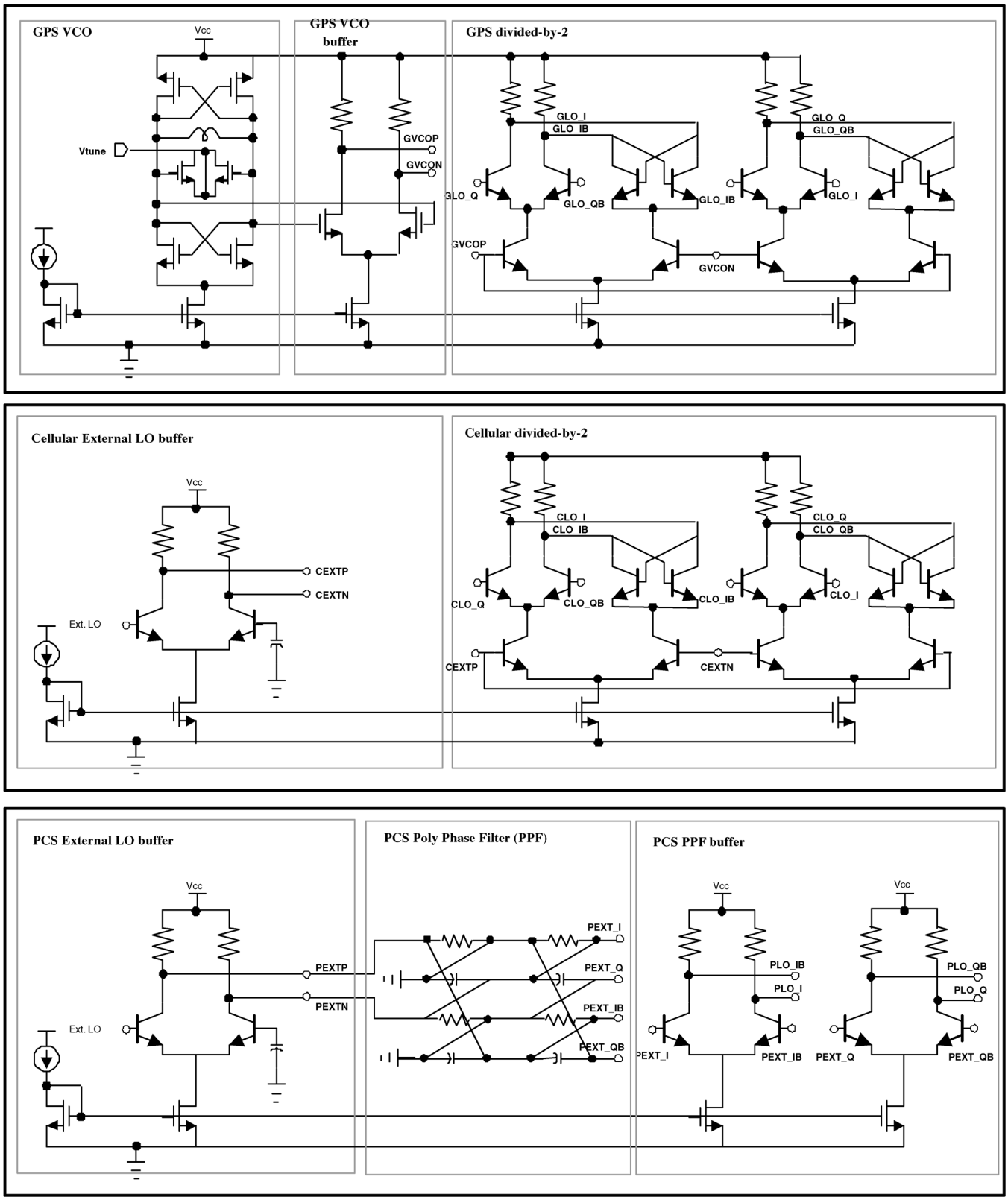

Fig. 3. Simplified circuitry of LO distribution.

impedance at a low frequency range is very low and has no effect on the operating RF frequency range [11]. The bypass devices M1 and C1 are also important because these parts have an effect on the high gain mode while simultaneously affecting their own modes. Generally, the device size of the M1 is large for a bypass gain and high IIP3. The loading effect of additional gain stages can degrade the performance of a high gain mode, whereas additional gain stages using M1 and C1 are off while in a high gain mode. PCS LNA (PLNA) also operates in the three gain modes of high/bypass/loss modes, and the circuit compo-

TABLE I
IIP2 COMPARISON BETWEEN SIMULATION AND MEASUREMENT

	Cellular CDMA	PCS
Simulated $IIP2_{mixer}$ without even-harmonic reduction	43 dBm	43 dBm
Simulated $IIP2_{mixer}$ with even-harmonic reduction	82.1 dBm	79 dBm
Measured $IIP2_{mixer}$ with even-harmonic reduction	81 dBm	79.8 dBm

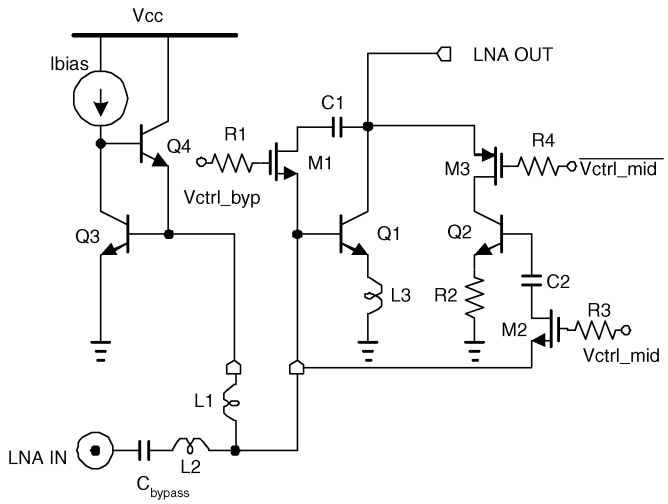

Fig. 4. Simplified schematic of Cellular LNA (CLNA) and PCS LNA (PLNA).

TABLE II
MEASURED PERFORMANCE OF DIRECT CONVERSION RECEIVER

		Cellular CDMA	PCS	GPS
NF_{chain}	High gain	2.4 dB	2.9 dB	2.0 dB
	Mid gain	16 dB	27.8 dB	
	Low gain	29.3 dB	42.6 dB	
$IIP3_{chain}$	High gain	-1.27 dBm	-3.7 dBm	-30 dBm
	Mid gain	4.95 dBm	20.1 dBm	
	Low gain	16.1 dBm	21 dBm	
$IIP2_{chain}$	High gain	70.8 dBm	68 dBm	26 dBm
	Mid gain	84.7 dBm	75.7 dBm	
	Low gain	96.3 dBm	71.67 dBm	
LO-to-RF isolation	mixer input	-97.6 dBm	-87.2 dBm	-107 dBm
Current	High gain	52 mA	56 mA	35 mA
	Mid gain	52 mA	56 mA	
	Low gain	44 mA	48 mA	

sition of PLNA is similar to one for CLNA, despite the fact that the gain specification of PLNA is different from that of CLNA.

Fig. 5 shows a simplified schematic of GPS LNA (GLNA) and of a GPS MIXER core. Unlike CLNA and PLNA, GPS LNA is designed with a differential cascode type amplifier in order to acquire a sufficient gain for fulfilling high sensitivity demands and maintaing a high immunity to substrate and supply noises. As the output of the GLNA and the input of the GPS mixer are connected internally, the internal high-Q differential spiral inductor and capacitors are adequately utilized for the maximum voltage transfer from the GLNA output to the GPS mixer input. The common output folding stage is shared with the cellular CDMA and PCS mixer cores.

E. Channel Selection Filter (CSF)

The baseband filters reject large interferers while performing a channel selection. The performance requirements of the baseband filters are more stringent compared to those of a heterodyne receiver because there are no IF filters before the baseband filters in a direct-conversion receiver. The architecture in a direct-conversion receiver limits the RF-path gain before the baseband filter; thus, any further amplification of the receiver gain must be accomplished during or after the channel filtering and the generated noise at the base-band filter is severely restricted.

The channel select filter is a fifth-order elliptic filter because the filter achieves the out-of-band attenuation requirement in the CDMA system. The filter has a -3 dB bandwidth of 630 kHz. The block diagram of the base-band channel selection filter is shown in Fig. 5. The filter architecture was based on the leapfrog ladder prototype for its low sensitivity and its immunity to a device mismatch. It was implemented in an active-*RC* filter for its inherent linearity characteristics. For a low-noise performance, the resistor value of the filter's first stage is minimized and the input differential pair of the opamp is designed with bipolar transistors. A two-stage opamp topology is chosen to drive the resistive load. The rail-to-rail output swing of the opamp is suitable for dealing with larger interferers. The filter is optimized for noise and linearity performance by scaling the gain of each stage. The signals of the filter are fully balanced for high IIP2 and CMRR.

The frequency response of the filter is auto-calibrated with fine accuracy by the 5-bit capacitor arrays as well as the 2-bits resistor arrays. The calibration circuit uses the time-based integrator's characteristic and requires a reference clock. The calibration is activated by the receiver's power coming on, and is disabled during normal operation. The required calibration time is below 40 μs and assures a 2.5% frequency tuning accuracy. The filter has a dc offset cancellation block for solving the dc-offset problem. The dc offset cancellation block uses the dc feedback loop with a servo amplifier. The dc-cutoff frequency is approximately 5 kHz.

VI. MEASUREMENT RESULTS

The microphotographs of the direct-conversion receiver chip set for the cellular CDMA, PCS, and GPS applications are shown in Fig. 7. Fig. 7(a) shows the RF front-end chip and Fig. 7(b) is the base-band chip. The front-end chip and the base-band chip These were both fabricated in a 0.35 um BiCMOS process and occupy a 2.3 mm $\times$ 1.9 mm and 2.3 mm $\times$ 1.5 mm die area, respectively. These chips are packaged in a 6 mm $\times$ 6 mm MLF 36-pin chip-scale package.

For even-harmonic reduction the feedback loop gain has approximately 40 dB, which is limited by the stability problem. The comparison between the simulated $\mathrm{IIP2_{mixer}}$ and the measured $\mathrm{IIP2_{mixer}}$ is given in Table I. It shows that the proposed technique improves the $\mathrm{IIP2_{mixer}}$ performance by an amount of loop gain compared to the a simple analysis without an even-harmonic reduction technique. And the measured $\mathrm{IIP2_{mixer}}$ with the proposed technique matches well enough to simulated one.

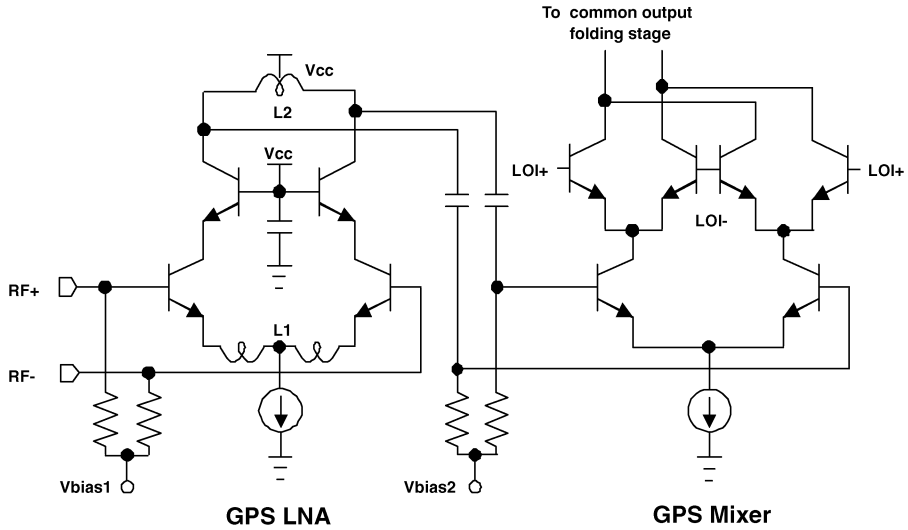

Fig. 5. Simplified schematic of GPS LNA (GLNA) and GPS MIXER.

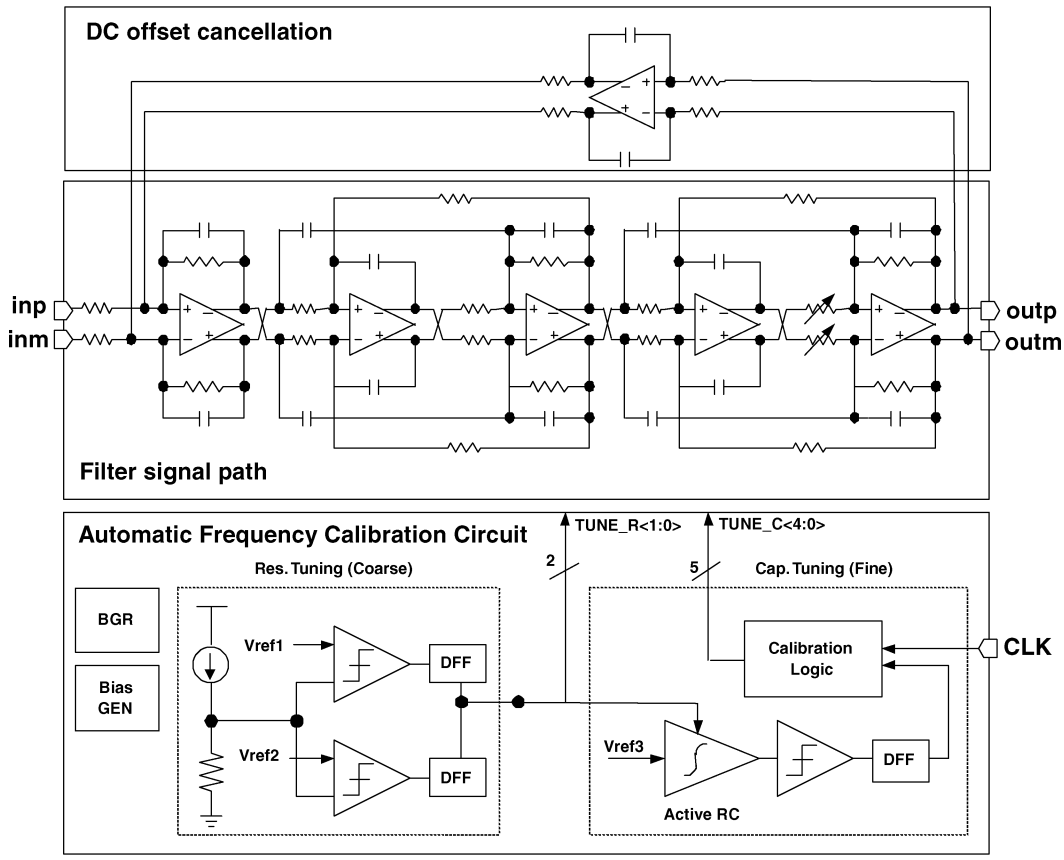

Fig. 6. Simplified block diagram of a channel selection filter.

Fig. 8 shows the variation in the $\mathrm{IIP2_{mixer}}$ along the downconversion channel once the mixer has been trimmed. It shows that the $\mathrm{IIP2_{mixer}}$ decreases as the downconversion channel rises to 5 MHz, but is almost flat within the downconversion channel bandwidth of 630 kHz. Fig. 9 shows the measured sensitivity of the improved $\mathrm{IIP2_{mixer}}$ as a function of the controlled imbalance in the mixer output load resistor. It shows that the IIP2 of the cellular CDMA band is approximately 80 dBm and that the variation is small. It also shows that the IIP2 variation of the PCS band is larger than that of the cellular CDMA band, as the LO distribution of the PCS band is more complex. The measured sensitivities of the IIP2mixer in Figs. 8 and 9 show that is the $\mathrm{IIP2_{mixer}}$ is insensitive to the operating condition and the mismatch due to the proposed IIP2-enhancing technique.

The measured performance of proposed the cellular CDMA/PCS/GPS receiver is summarized in Table II. The proposed receiver has three gain modes to achieve the CDMA standard requirements. These measured results satisfy the calculated system requirements of the (1), (2), and (3) in Section III. The cellular LNA has a measured performance of 1.52 dB NF/8 dBm IIP3/15.5 dB gain/8 mA of current consumption at the high-gain mode, 3.95 dB NF/12.5 dBm

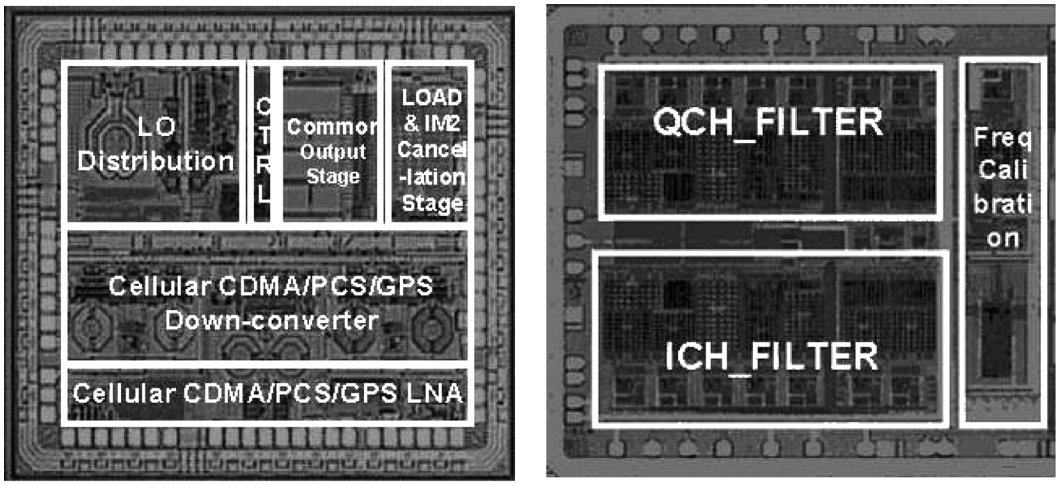

Fig. 7. Micrograph of a direct conversion receiver. (a) RF front-end chip. (b) Baseband chip.

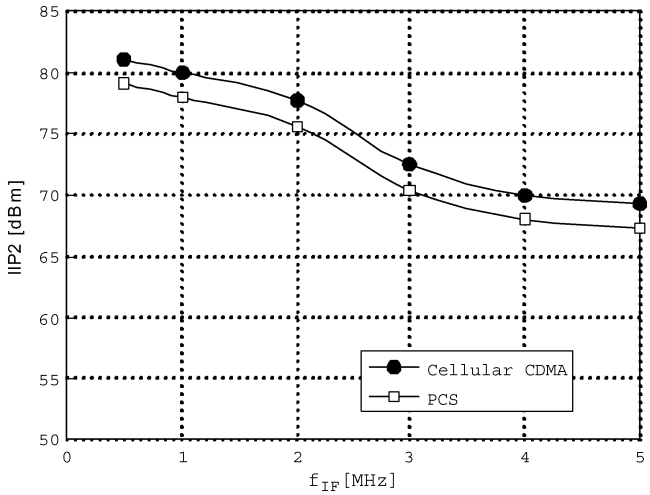

Fig. 8. Measured sensitivity of $\mathrm{IIP2}_{\mathrm{mixer}}$ performance as a function of output frequency.

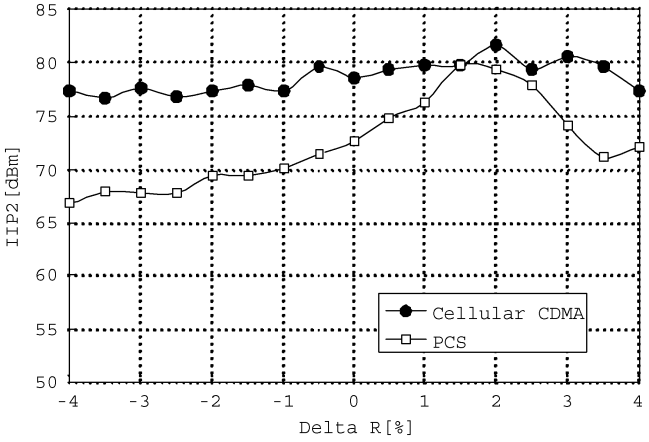

Fig. 9. Measured sensitivity of $\mathrm{IIP2}_{\mathrm{mixer}}$ performance as a function of output load mismatch.

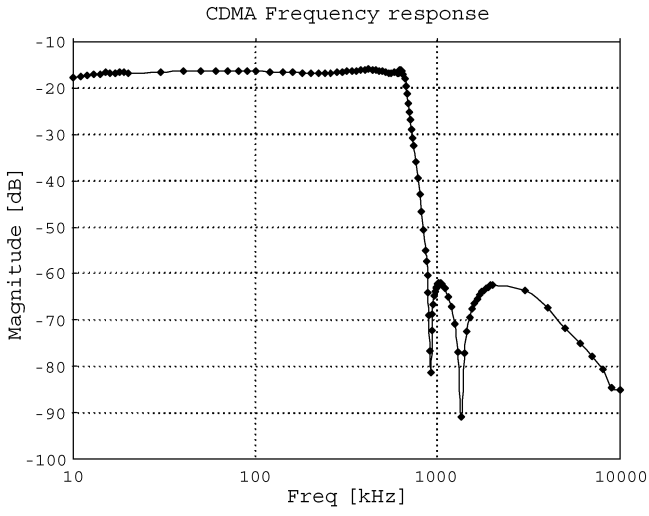

Fig. 10. CDMA filter frequency response.

IIP3/6.3 dB gain/8 mA of current consumption at the midgain mode, and 7.3 dB NF/19 dBm IIP3/−6.3 dB gain/0.2 mA of current consumption at the low-gain mode. The PCS LNA has a measured performance of 2.0 dB NF/3.8 dBm IIP3/15.2 dB gain/8 mA of current consumption at the high-gain mode, 11.5-dB NF/25.5 dBm IIP3/−11.5 dB gain/8 mA of current consumption at the midgain mode, and 27-dB NF/20 dBm IIP3/−25.5 dB gain/0.2 mA of current consumption at the low-gain mode.

Fig. 10 shows the CDMA output frequency response of the proposed receiver. The measured results shows that the CDMA receiver has a 3-dB bandwidth of 630 kHz and over 40-dB attenuation of over 900 kHz, which is similar to the simulation result. Fig. 11 shows the CDMA receiver output spectrum when a −101 dBm in-band signal and −43 dBm out-band jammer signal are applied to the LNA, which shows that the −43 dBm adjacent channel jammer is rejected by 51.47 dB $(-43\ \mathrm{dBm} + 101\ \mathrm{dBm} - 6.53\ \mathrm{dB})$. The measured IQ mismatch is smaller than 0.5 dB. The measured dc-offset at the baseband output was maintained to within 3 mV.

VII. Conclusion

This paper presents direct-conversion cellular CDMA/PCS/GPS direct-conversion receiver chips using an even-harmonic reduction technique to enhance IIP2 performance. This receiver has been designed and fabricated in a 0.35 um SiGe

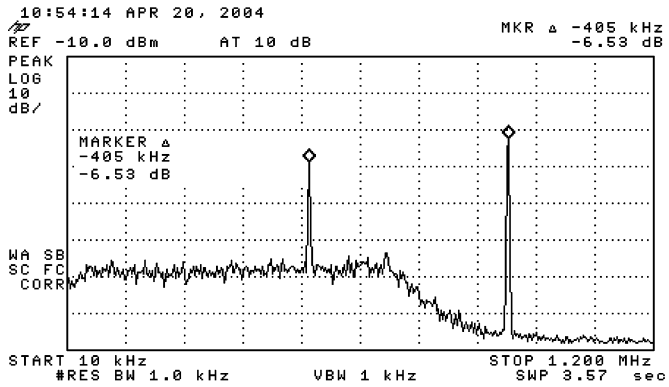

Fig. 11. CDMA filter output spectrum when a −101 dBm inband signal and a −43 dBm outband jammer (@ 900 kHz) signal are applied to the LNA.

BiCMOS process. Measurement results of the receiver chain show 71 dBm IIP2, −1.3 dBm IIP3, and 2.4 dB NF for Cellular CDMA; 68 dBm IIP2, −3.7 dBm IIP3, and 2.9 dB NF for PCS; and 26 dBm IIP2 −30 dBm IIP3 and 2 dB NF for GPS, as shown in Table II. The proposed IIP2 enhancement technique is described by a simplified analysis of the second-order intermodulation. Due to this technique, the IIP2 performance can be improved by reducing sensitivity to operating condition and to an output load mismatch. The experimental results show a 40 dB improvement and a reduced sensitivity of IIP2, which is in good agreement with the simulation results.

ACKNOWLEDGMENT

The authors wish to acknowledge the FCI Quality and Product Engineering team for their measurement support, and T. H. Lee and K. Kim for their software assistance.

REFERENCES

[1] A. Abidi, "Direct-conversion radio transceivers for digital communications," *IEEE J. Solid-State Circuits*, vol. 30, pp. 1399–1410, Dec. 1995.
[2] B. Razabi, "Design considerations for direct-conversion receivers," *IEEE Trans. Circuits Syst. II*, vol. 44, pp. 428–435, June 1997.
[3] K. Kivekas *et al.*, "Characterization of IIP2 and dc-offsets in transconductance mixer," *IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process.*, vol. 48, pp. 1028–1038, Nov. 2001.
[4] D. Manstretta, "Analysis and optimization of IIP2 in CMOS direct down-converters," in *Proc. IEEE 2002 Custom Integr. Circuits Conf.*, May 2002, pp. 243–246.
[5] K. Kivekas *et al.*, "Calibration techniques of active BiCMOS mixer," *IEEE J. Solid-State Circuits*, vol. 37, pp. 766–769, Jun. 2002.
[6] M. W. Hwang, S. Y. Yoo, J. C. Lee, J. Lee, and G. H. Cho, "A high IIP2 direct-conversion mixer using an even-harmonic reduction technique for cellular CDMA/PCS/GPS applications," in *Proc. IEEE RFIC Symp. Dig.*, 2004, pp. 39–42.
[7] O. K. Jensen, "RF receiver requirements for 3G W-CDMA mobile equipment," *IEEE Microw.*, Feb. 2002.
[8] Recommended Minimum Performance Standards for Dual-Mode Wideband Spread Spectrum Cellular Mobile Stations TIA/EIA-98, Nov. 1997.
[9] M. W. Hwang, J. T. Hwang, and G. H. Cho, "Design of high speed CMOS prescaler," in *Proc. Second IEEE Asia Pacific Conf. ASICs. AP-ASIC 2000*, 2000, pp. 87–90.
[10] Q. Liang, "Geometry and bias current optimization for SiGe HBT cascode low-noise amplifiers," in *Proc. IEEE RFIC Symp. Dig.*, 2002, pp. 407–410.
[11] V. Aparin, "Highly linear SiGe BiCMOS LNA and mixer for cellular CDMA/AMPS applications," in *Proc. IEEE RFIC Symp. Dig.*, 2002, pp. 129–132.

Myung-Woon Hwang was born in Seoul, Korea, in 1974. He received the B.S., M.S., and Ph.D. degrees in electronics engineering from Korea Advanced Institute of Science and Technology (KAIST), Deajon, in 1996, 1998, and 2005, respectively.

In 2003, he joined Future Communications IC (FCI) Inc., Sungnam, Korea. He is currently a design manager with the development team as an Associate Director. He is involved with the development of SiGe BiCMOS RF wireless transceivers. His other research interests include the CMOS RF transceiver, frequency synthesizer, and high-speed communication interfaces.

Dr. Hwang won a Bronze Medal in the Human-Tech Thesis Prize hosted by Samsung Electronics, Inc., in 1996.

Gyu-Hyeong Cho received the Ph.D. degree in electrical engineering from the Korea Advanced Institute of Science and Technology (KAIST), Taejon, in 1981.

He was with the Westinghouse R&D Center until 1983. Since 1984, he has been with KAIST, where he was appointed Professor in 1991. During 1989, he was a Visiting Professor with the University of Wisconsin, Madison. He is interested in power electronics, but since 1993, has also been interested in the area of CMOS/BiCMOS analog integrated circuits including A/D converters, smart power IC's, RF IC's for wireless communications, at panel displays, etc.

Dr. Cho is a member of the Institute of Electrical/Electronics Engineers of Korea.

Seungyup Yoo was born on December 24, 1969, in Seoul, Korea. He received the B.S. and M.S. degrees in electrical engineering from Hanyang University, Seoul, in 1992 and 1994, respectively, and the Ph.D. degree in electrical and computer engineering from the Georgia Institute of Technology, Atlanta, in 2000.

From 2000 to 2003, he was with RF Solutions, Atlanta, where he was a staff engineer and worked on GaAs MESFET and SiGe BiCMOS RFIC designs for wireless data applications. He is currently with Future Communications IC (FCI) Inc., Sungnam, Korea, working as an Associate Director since 2003. His main research interest includes various SiGe BiCMOS analog integrated circuits for wireless communication systems.

Jeong-Cheol Lee was born in Sangju, Korea, in 1976. He received the B.S. degree in electronic engineering from Kyungbuk National University, Taequ, Korea, in 1999 and the M.S. degree from the Department of Electrical Engineering, Pohang University of Science and Technology (POSTECH), Kyungbuk, Korea, in 2001.

In 2001, he joined Future Communications IC (FCI) Inc., Sungnam, Korea, where he is currently a senior engineer. He is involved with the development of SiGe BiCMOS RF wireless transceivers. His other research interests include the VCO, frequency synthesizer, high-speed communication interfaces, signal integrity, and interconnect modeling.

Sungmin Ock received the B.S. and M.S. degrees from the Pohang University of Science and Technology, Pohang, Korea, in 1997 and 2000, respectively.

Since 2000, he has been with Future Communications IC (FCI) Inc., Sungnam, Korea, where he designed various RF circuits applying for wireless communications. Currently, he is interested in the nonlinearity of device and amplifier.

Sunki Min was born in Seoul, Korea, in 1975. He received the B.S. and M.S. degrees in electrical engineering from University of Seoul, in 2001 and 2003, respectively.

He is currently working with Future Communications IC (FCI) Inc., Sungnam, Korea. He is an Associate Engineer with the WTG/ZR team and involved with the development of SiGe BiCMOS RF wireless transceivers. His other research interests include the Baseband analog integrated circuit design for wireless communications systems.

Sang-Hoon Lee was born in Seoul, Korea, in 1972. He received the B.S. and M.S. degrees in electronics engineering from Incheon University, Incheon, Korea, in 1998 and 2001, respectively.

In 2001, he joined Future Communications IC (FCI) Inc., Sungnam, Korea. He is currently a Senior Engineer with the WTG/ZR team. He is involved with the development of SiGe BiCMOS RF wireless transceivers. His other research interests analog-to-digital data converter.

Sungho Beck received the B.S. degree and the M.S. degree in electrical engineering from Korea Advanced Institute of Science and Technique (KAIST), Daejon, in 1999 and 2001, respectively.

He is currently a Senior Design Engineer with Future Communications IC (FCI) Inc., Sungnam, Korea. His current research interest includes the design of transceiver ICs for wireless communication applications.

Mr. Beck won a Bronze Medal in the Human-Tech Thesis Prize hosted by Samsung Electronics, Inc., in 1998.

Kyoohyun Lim was born in Taejon, Korea, in 1971. He received the B.S. and M.S. degrees in electrical engineering and the Ph.D. degree in electrical engineering from the Korea Advanced Institute of Science and Technology (KAIST), Taejon, Korea, in 1995, 1997, and 2002, respectively.

From 2001 to 2003, he was with Berkana Wireless, Inc., San Jose, CA, as a Member of Technical Staff, where he worked on the design of CMOS RF transceivers for CDMA, W-CDMA, and GSM/GPRS applications. He is currently with Future Communication IC (FCI), Inc., Sungnam, Korea. He is involved with the development of SiGe BiCMOS RF wireless transceivers. His current research interests include CMOS high-speed analog IC, mixed-mode signal processing IC, and integrated RF circuits for wireless communication systems.

Sangwoo Han was born in Seoul, Korea, in 1968. He received the B.S. degree in electrical engineering from Carnegie-Mellon University, Pittsburgh, PA, in May 1992, the M.S. degree in electrical engineering from the University of Pennsylvania, Philadelphia, in December 1993, and the Ph.D. degree in electrical engineering from the Georgia Institute of Technology, Atlanta, in May 2000.

In 1997, he cofounded RF Solutions Inc., Atlanta, which is now Anadigics WLAN center of excellence, where he was a principal engineer and developed 2.4-GHz, 3.5-GHz, and UNII band power amplifiers products for fixed wireless and WLAN applications. He joined Future Communication IC (FCI), Inc., Sungnam, Korea, in 2003. He is currently a Director of the WTG and in charge of transceiver developments for various wireless communication applications.

Dr. Han has written and contributed to several IEEE TRANSACATIONS ON MICROWAVE THEORY AND TECHNIQUES (MTT) publications and presented at many conferences on RF/optical communications and RF transceiver design.

Joonsuk Lee (S'97–M'03) received the B.S., M.S., and Ph. D degrees in electrical engineering and computer sciences from Korea Advanced Institute of Science and Technology (KAIST), Daejon, in 1995, 1997, and 2002, respectively.

From 1999 to 2000, he was with IBM Microelectronics, Boston, MA, where he conducted research on a high performance sigma-delta ADC/DAC. From 2002, he joined Future Communications IC (FCI) Inc., Sungnam-City, Korea, as an Associate Director involved with a direct-conversion RF system. His research interests include PLL/DLL, timing recovery algorithm, high-speed SDRAM interface, LAN, and multimode RF/IF trancesiver IC's.

Dr. Lee is the Gold Medal winner of the 4th Human-Tech Thesis Prize from Samsung Electronics Co. Ltd., in 1997, the Gold Medal winner of the 4th Chip Design Contest from LG Semicon Co. Ltd., in 1998, and the Gold Medal winner of the 2nd Integrated Design Center (IDEC) Award in 1998.