A CMOS 10Bit 37MS/s Pipelined A/D Converter with Code Regeneration and Averaging

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Abstract

A 10bit pipelined analog to digital converter(ADC) having 1bit per stage architecture with code regeneration is proposed. Code regeneration is performed by digital averaging of two analog shifted codes obtained from one sample of analog input to ADC. Analysis shows allowable gain and offset errors are tolerable up to 8bit resolution to achieve 10bit ADC. This allows ADC free from calibration or trimming against gain errors to implement 10bit resolution. Test results show that the maximum DNL of 0.51LSB and 37MHz conversion rate with the process of 0.8um CMOS.

1. Introduction

Analog to digital converters(ADC) are developed in wide varieties. One of the main issues of resent papers is calibration[3~6]. Main purpose of calibration is to compensate gain errors in residue because the conventional digital error correction cannot correct gain error of residue amplifier. Thus if we want a 10 bit ADC with digital error correction circuit, we must design circuits reducing or canceling gain error down to 0.1% rather than offset error. Calibration may be a method to increase resolution above 10bit, but complex logic and memories are needed requiring extra calibration cycle. Continuously calibrated ADC seems to solve the problem of extra cycle[7], however, large area and power as well as complexity are the price to be paid. Error drift due to aging and temperature requires more often calibration, it is very inconvenient to user.

The simulation of yield of a ADC can be done by inserting random error. Offset and gain errors degrade the yield but due to conventional digital error correction technique[1,2], offset errors have no effect on the linearity of a ADC. But the error of residue gain still remains critical factor degrading the yield. Proposed 10bit pipelined ADC uses 1bit per stage architecture with code regeneration. Code regeneration is performed by digital averaging of two analog shifted codes obtained from one sample of analog input to ADC. Most striking merit of proposed 10bit ADC is that allowable gain error of the residue amplifier is four times larger than conventional technique of digital error correction. Analysis shows allowable gain errors and offset errors correspond to 8bit resolution to get 10bit ADC. And simulation shows that the proposed ADC gives higher yield. This technique makes ADC less sensitive to gain errors existing in residue amplifiers, which allows ADC free from calibration or trimming. Considering the allowable errors of 8bit resolution, the proposed ADC provides less sensitivity to aging or temperature than conventional method of digital error correction.

2. Proposed ADC with 1bit per stage

Fig. 1 is the block diagram of proposed ADC with 1bit per stage pipelined architecture. Conventional digital error correction is not used here. For 10bit ADC, one sample and hold amplifier(S/H), and nine stages of residue amplifier are needed. Every stage must have one comparator at its output. First five residue amplifiers perform the following calculation at their output:

$$Vres = Gres \times Vin - Gdac \times Vda \qquad (1)$$

where Vda is the quantization level of Vin. The value of Gres is larger than 2 and that of Gdac is larger than 1. Last four residue amplifiers perform conventional operation with Gres=2 and Gdac=1 as in (1).

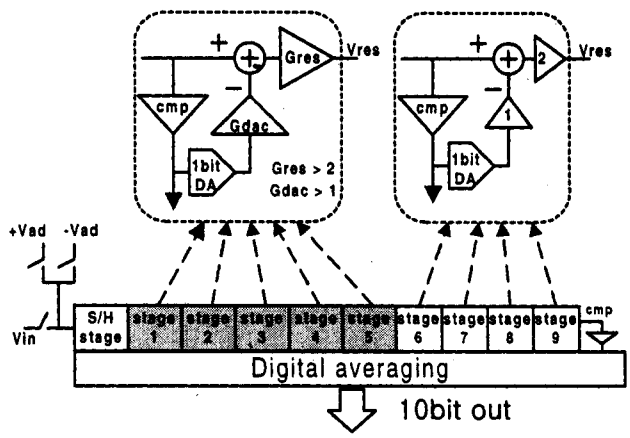

Fig. 1. Proposed pipelined ADC of 1bit per stage

There are two inputs in Fig. 1, one is analog signal 'Vin', the other is small dc voltage 'Vad'. The operation is that ADC block quantizes 'Vin+Vad' and produces code1 first and, quantizes 'Vin-Vad' and produces code2 next. Fully differential architecture is easy to apply +Vad and -Vad sequentially by crossing switches. The ADC generates two codes of 20bits corresponding to one sample of Vin. Then digital logic gets two codes and generates smooth code of final 10bit output. Since two codes are obtained from one sample of analog input, conversion speed becomes half compared to conventional architecture. This is one disadvantage of the proposed ADC.

Fig. 2 is the plot of three codes with respect to Vin. Each code has 10bit length with 1024 digital values and final code is the result of digital averaging. For the convenience of explanation, Fig. 2 is the case that the first two residue amplifiers have adjusted gain such that Gres > 2 and Gdac > 1, and the other stages have Gres = 2 and Gdac = 1. In the prototype ADC, the first five residue amplifiers have adjusted gain. The curves of code1 and code2 are just the same except the analog shift of 2Vad as in Fig. 2. P is the width of wide code. Vad is a known DC voltage with 2Vad ≡ P. Vfs is the full scale voltage of ADC. Prototype ADC uses the digital averaging of unity weight which is simply composed of adders with one bit truncation, however, truncation does not make DNL error.

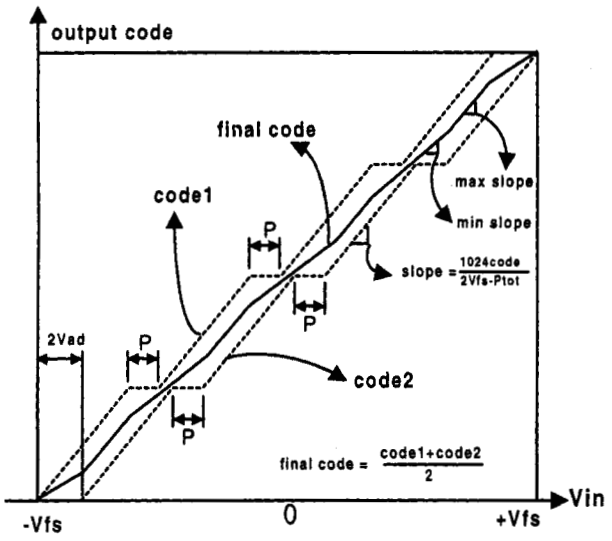

Fig. 2. Code regeneration and averaging method.

3. Errors in the proposed ADC

Analysis of error limit starts from the assumption that if first K stages of residue have the adjusted gain, the other stages have negligible errors. This is reasonable assumption considering the gain of first K residue amplifiers. One more condition is needed, that is, code1 and code2 have no wide codes at the same time, i.e., no overlapped 'P' region as in Fig. 2. This guarantees that the final code has no wide code. Now the final code in Fig. 2 has a range of slope due to averaging operation with the slope of code1 and code2. To get the maximum 0.5LSB DNL, the slope of final code must satisfy the following conditions:

$$\text{max slope} \cong \frac{1024\text{code}}{2\text{Vfs} - \text{Ptot}} < \frac{1\text{code}}{0.5\text{LSB}}$$

$$\text{min slope} \cong \frac{512\text{code}}{2\text{Vfs} - \text{Ptot}} > \frac{1\text{code}}{1.5\text{LSB}}$$

$$\therefore \frac{0.5\text{Vfs}}{2^K} < P < \frac{\text{Vfs}}{2^K}$$

$$\therefore \Delta P = 0.5\text{Vfs}/2^K \quad (2)$$

where 1LSB is 2Vfs/1024 and each wide codes in Fig. 2 have the same width of P. Ptot is the total width of wide code such that Ptot = $P(2^K-1)+2\text{Vad} \cong P\times 2^K$. K is the number of residue amplifiers having adjusted gain. Fig. 2 is the case of K=2. Max slope of final code appears when code1 and code2 are in the same slope region. Min slope of final code appears when one of code1 and code2 is in the zero slope region, in other words, 'P' region. (2) gives allowable error-limit of ADC since P is directly related to offset error of first K stages and ΔP is related to gain error. Now let the adjusted gains in residue of i th stage be follows:

$$\text{Gres}(i) = \frac{1.5}{3/4 - 0.5\text{Pc}(i)/\text{Vfs}} \quad (3)$$

$$\text{Gdac}(i) = \frac{3\text{Gres}(i) - 2}{4} \quad (4)$$

where Pc(i) is related to P such that:

$$P = 2\text{Pc}(1)+\text{Pc}(2)/3+\text{Pc}(3)/6+\ldots+\text{Pc}(K)/(3\times 2^{K-2})$$
$$\therefore \Delta P = 2\Delta\text{Pc}(1)+\Delta\text{Pc}(2)/3+ \ldots +\Delta\text{Pc}(K)/(3\times 2^{K-2})$$

Now if every ΔPc(i) is the same as ΔPc then:

$$\therefore \Delta\text{Pc} = \frac{\Delta P}{(2+\frac{1}{3}\times\frac{1-0.5^{K-1}}{0.5})} = \frac{\Delta P}{(2+\frac{2}{3}\times(1-0.5^{K-1}))} \quad (5)$$

The combination of (2), (3), (4), (5) produces ΔGres and ΔGdac:

$$\Delta\text{Gres} = \frac{2}{(6+2\times(1-0.5^{K-1}))(2^K)} \quad (6)$$

$$\Delta\text{Gdac} = \frac{6}{4(6+2\times(1-0.5^{K-1}))(2^K)} \quad (7)$$

ΔGres/Gres is about 0.4% for K=5 and 0.8% for K=4 and 0.2% for K=6. Intuitively INL becomes smaller for larger value of K. So the optimum value of K is 5 if achievable gain error is 0.4%. And if achievable gain

error is 0.2% then the optimum value is 6. In the prototype ADC, 0.4% matching is reasonable so the value of K is 5. And P is about 40mV. This limit is 4 times larger than conventional ADC of digital error correction. For conventional digital error correction method, gain error of +0.4% gives code overlap and that of -0.4% gives code missing.

The input offset of total ADC is affected by the offset of residue amplifier. This is because the decision levels of first five MSB's are inside 'P' region if the error of offset is less than P/2.

Except the analog shift of 2Vad, the difference between code1 and code2 can appear due to random transient noise such as settling time difference and switching noise difference. This can be larger than 1LSB, but if there is no overlap interval of 'P' region in which both of code1 and code2 simultaneously generates wide code, final output code can maintain the maximum DNL of 0.5LSB. But slight change in INL can be expected.

The yield simulation is shown in Fig. 3. The amount of yield is % of the number of ADC's satisfying DNL of less than 0.5LSB. Random gaussian errors are inserted in residue gain and offset. Settling time error is also considered. All four cases are above 80% near 0.1% gain error. But as the gain error increases up to 0.5%, conventional ADC has less than 10% yield, on the other hand, the proposed ADC maintains 60% for 0.13% settling error and, 80% for 0.1% settling error.

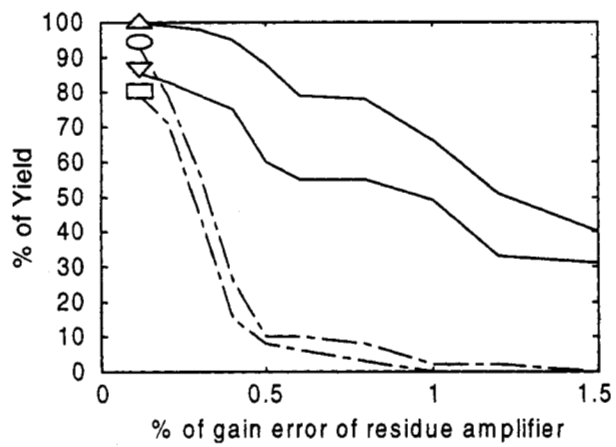

Fig. 3. Simulations of yield of the proposed ADC

4. S/H and residue amplifier

Fig. 4 is the circuit of S/H. Vin is sampled at shck1 and +Vad is applied to S/H input at shck21, and -Vad is applied at shck22. And next residue amplifier samples the output of S/H at ck2. In this way 'Vin+Vad' and 'Vin-Vad' are processed through following stages making two codes per one sample of Vin. Residue amplifier in Fig. 5 gives Gres = {C1+C2}/C2 and Gdac = C3/C2 as in (1). This architecture can give Gres and Gdac any value. Main offset error comes from switches of unity feedback not from OP-amp. Mismatches of switch feedthrough make offset errors. To make mismatches of switch feedthrough small, small size switch is needed if minimum size L is used. This is because large W makes large effects of mismatches in L. But small size switch causes large settling time. Proposed S/H and residue amplifier uses smallest size of unity feedback switches with the output compensation capacitor satisfying the time constant of 0.5ns. NMOS gate acts as a compensation capacitor and two stages of ADC share one pair of gate capacitor to reduce overall area.

Architecture of OP-amp is similar one as presented in [8], but with different design guide and CMFB structure. High DC gain of 90dB in OP-amp makes less sensitive to parasitic capacitance and reduces the effects of gain drift by temperature.

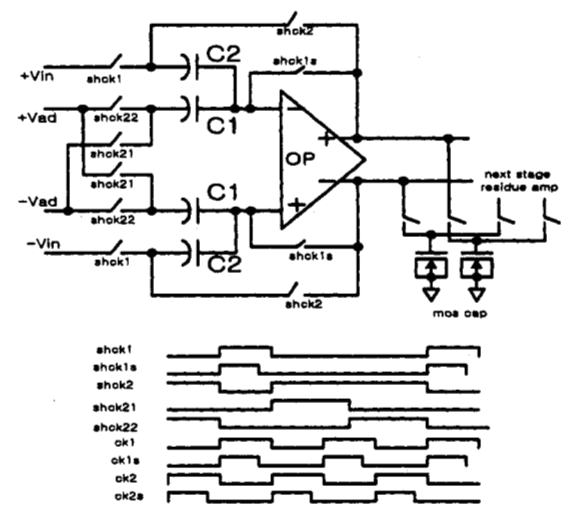

Fig. 4. S/H circuit and clock timing

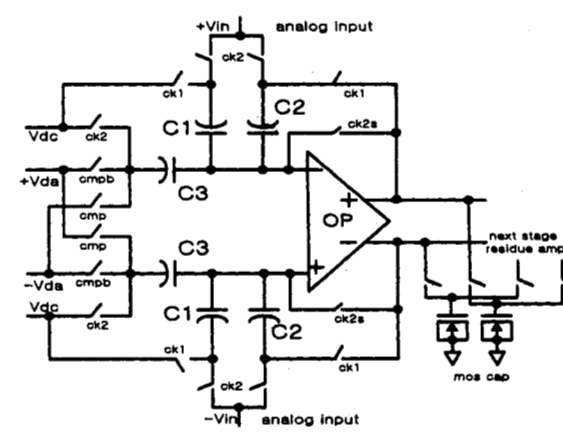

Fig. 5. Residue amplifier circuit

5. Measured results

Prototype ADC is fabricated in 0.8um double metal CMOS process. Two poly capacitor is used. The Die photo is shown in Fig. 7. Total size is 1.7mm x 2.4mm.

Table 1 summarizes the measured results. Typical plot of differential non-linearity(DNL) and integral non-linearity (INL) is shown in Fig. 6. Maximum DNL is 0.51LSB and maximum INL is 1.8LSB.

6. Conclusion

Proposed 10bit pipelined ADC uses 1bit per stage architecture with code regeneration. Code regeneration is the averaging of two codes obtained from one ADC block and this technique gives at least 4 times larger limit of allowable gain error than conventional digital error correction method. This allows ADC free from calibration or trimming against gain errors to achieve 10bit or more resolution. And thus higher yield and less sensitivity to aging or temperature is expected. Test results show the maximum DNL of 0.51LSB without any calibration or trimming.

Table 1. Measured properties of ADC

Supply voltage	3.3V, 5V
Resolution	10Bit
Conversion speed	37MHz
Avg Power at 37MHz	82mW
Full Scale	1.4Vp differential
Chip Area	1.7mm x 2.4mm
Process	0.8um two poly CMOS
Max DNL	+0.51LSB, -0.4LSB
Max INL	+0.9LSB, -1.8LSB

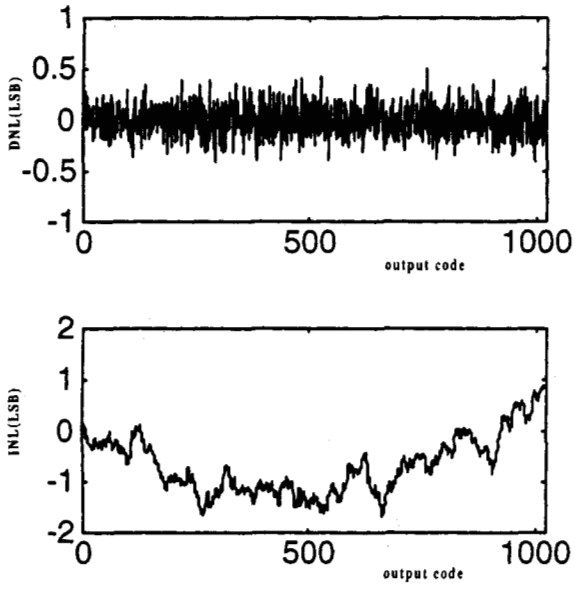

Fig. 6. Typical plot of DNL and INL

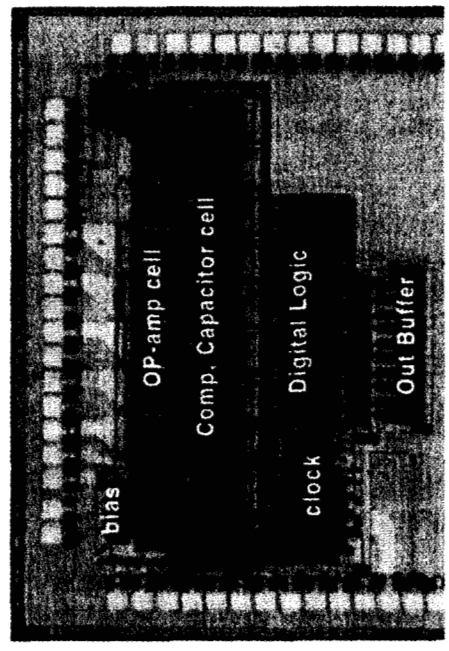

Fig. 7. Die photo of ADC

7. References

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