New Current Source Inverters with dc-Side Commutation and Load-Side Energy Recovery Circuit

Yong-Ho Chung and Gyu-Hyeong Cho

Abstract—**Two all-thyristor-type current source inverters (CSI's) with dc-side commutation and load-side energy recovery are proposed with analyses and explanations of the circuit operations. The inverters overcome most of the drawbacks of conventional CSI's—high device voltage stress, low operating frequency range, large commutation capacitance, etc.—by employing a simultaneous recovery and commutation concept. The new CSI's employ only one commutation capacitor and can be built with considerably low cost. The commutation energies are temporarily stored in a large dc capacitor and recovered to the load side, which makes the device voltage stress low and the efficiency high.**

Computer simulation results are given in brief comparison with the auto-sequentially commutated inverter. Finally, experimental results are shown for 5-hp induction motor drive.

I. Introduction

THE MOST widely used current source inverter (CSI) is the auto-sequentially commutated inverter (ASCI) because of its simplicity and reliability [1]. However, the ASCI has some drawbacks that are caused by the commutation circuit. There have been several attempts to eliminate or to reduce the drawbacks of the ASCI [2], [4], [6], [7].

One method is to add a delayed thyristor ring-up circuit [6], [7] to the basic power circuit to widen the operating frequency range while maintaining the same voltage stress as the basic circuit. However, this approach increases the device and the commutation capacitor current stresses because the commutation capacitance and the ring-up reactance should be increased and decreased, respectively, in order to reduce the voltage stress while maintaining the maximum operating frequency constant.

Another method is to add an energy recovery or voltage clamping circuit to reduce the voltage stress while maintaining the wide operating frequency range [4], [5]. The recovered energy is returned to the dc link side or the utility ac lines. If the recovered energy is fed to the dc link side, undesired current ripple occurs in the load side. On the other hand, if the energy is to be returned to the utility, the required hardware cost becomes expensive. In order to overcome such problems, the simultaneous recovery and commutation (SRC) concept is introduced, where the recovered energy is fed to the motor side during the commutation interval [2]. In the SRC concept inverter (SRCI), the energy of recovery capacitor is discharged to the oncoming phase of the motor during the commutation interval until the offgoing phase current of the motor becomes about one half of the dc link current. After that, the remaining energy in the leakage reactance of the motor is recovered to the recovery capacitor for the next commutation, whereby the device voltage stress is greatly reduced. In addition, the device voltage stress level can be controlled by varying the discharging interval length as a function of load current.

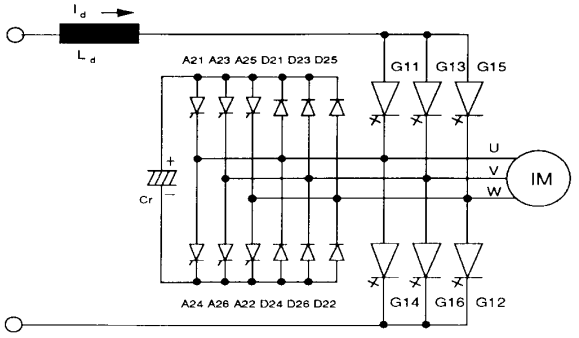

Fig. 1. Power circuit of GTO-type SRCI.

Fig. 1 shows the power circuit of the SRCI, whose main switching devices are composed of GTO's. One drawback of such a basic circuit shown in Fig. 1 is that the commutation failure of the auxiliary thyristors could occur when the oncoming phase current exceeds the dc link current during the discharging interval. This phenomenon can happen when the load current is abruptly changed. Besides, the system cost becomes high because it employs GTO's as main switches. If thyristors are used as main switches, the inverter cost can be low, and its power rating can also be easily increased, even though the additional commutation circuit that turns off the main thyristors is required. However, if the hard commutation circuit such as the ASCI is used to turn off the main thyristors, the voltage stress of the devices is increased about twice that of the commutation capacitor. This is because the summed voltage of the commutation capacitor and the energy recovery capacitor is applied to the devices during commutation. In addition, the possibility of commutation failure still exists if the SRC concept is applied to the ASCI-type CSI's.

In this paper, two all-thyristor type CSI's operating with the SRC concept are proposed to reduce the device voltage stress and to eliminate the commutation failure problems. Two proposed inverter circuits are analyzed approximately to give a guideline of the commutation circuit design, and their characteristics are compared with the ASCI. Finally, the operation of the proposed inverters is verified through computer simulation and the experiment.

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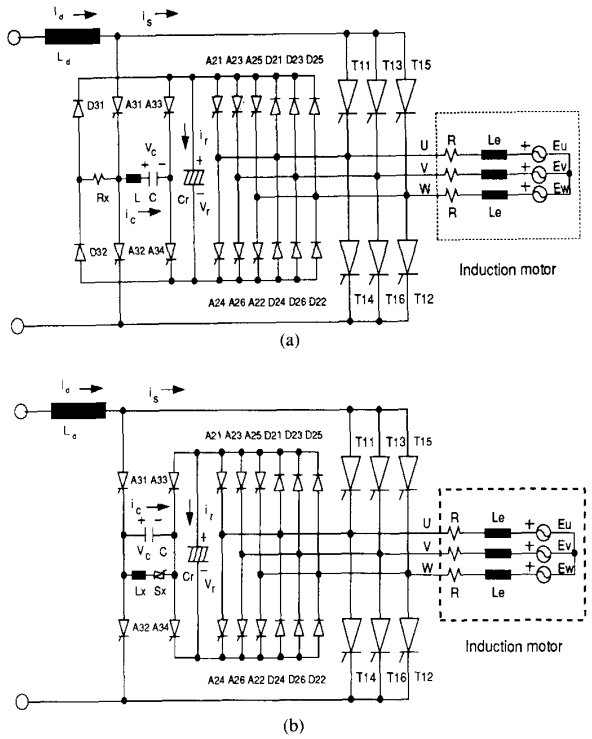

Fig. 2. Power circuits of the proposed two inverters: (a) Type-1 circuit; (b) type-2 circuit.

II. Description of the Proposed Inverter Circuits

Fig. 2 shows the power circuits of the two proposed inverters. Compared with Fig. 1, the dc-side commutation circuit is only added while replacing GTO's with thyristors. Six auxiliary thyristors ($A21$–$A26$), six diodes ($D21$–$D26$), and one dc capacitor C_r play the role of energy recoverer as in Fig. 1. The upper side (the lower side) main thyristors are commutated by turning on $A31$ and $A34$ ($A32$ and $A33$) simultaneously in both types of inverters.

In a type-1 circuit, four thyristors ($A31$–$A34$), two diodes ($D31$–$D32$), and three passive elements (R_x, C, L) operate as a soft commutation circuit with the help of six diodes ($D21$–$D26$). Since the offgoing thyristor of a type-1 inverter is turned off by the voltage drop across R_x, two diodes ($D31$ and $D32$) provide a short path to the L, C resonant circuit through a very small resistor R_x, whereby the main thyristor voltage stress is near the same as that of the recovery capacitor C_r.

In a type-2 circuit, four thyristors ($A31$–$A34$), one antiparallel thyristor S_x, one capacitor C, and one fast polarity conversion reactor L_x operate as a hard commutation circuit with the help of six diodes ($D21$–$D26$). S_x and L_x in type-2 inverters are used to delay thyristor ring-up operation [6]. Since the problem of device voltage stress cannot be solved if this circuit operates as the basic SRC inverter does, the operation of the basic SRCI is modified to limit the device voltage stress to the value of the capacitor C_r voltage. In this circuit, the offgoing thyristor is turned off before the discharging current of the capacitor C_r begins to flow through the oncoming phase. When the commutation capacitor voltage reaches zero, the auxiliary thyristor connected to the oncoming phase is turned on to start the discharging current, whereby the problem of device voltage stress is solved. Since this method shortens the length of the discharging time compared with the GTO-type SRCI, the resultant capacitor voltage stress is somewhat higher than that of the GTO-type SRCI but not significant up to 1.5 p.u. load condition.

III. Operations of Proposed Inverters

A. Type-1 Inverter

The initial state with $T11$ and $T12$ conducting is defined as mode 0. Mode 1 (Fig. 3(b)) begins by turning on thyristors $A23$ and $A24$, whereby the part of the stored energy of the capacitor C_r is discharged through the oncoming phase. After a certain period T_1, which is dependent on the operating condition, mode 2 (Fig. 3(c)) begins by firing thyristors $A31$ and $A34$ in order to turn off the main thyristor $T11$. During this interval, the commutation capacitor begins to discharge through L, $D32$, and R_x. Once the diode $D32$ is conducted, the offgoing thyristor $T11$ is turned off and reverse biased by the voltage drop across R_x. In this process, the thyristor $A24$ is also turned off by the conduction of diode $D24$ to provide the current path to the offgoing phase of the induction motor. This operation eliminates possible commutation failure problems. Since the interval length of mode 2 is dependent on several factors (such as the turn-off time T_{off} of the main thyristors, the di/dt limiting reactance L_{sn}, the dc link current, and the voltage drop across R_x), all of these effects should be considered in designing the commutation circuit for safe commutation, especially in the case of high-power application by using the exact thyristor turn-off model [3]. However, the thyristor's turn-off process is idealized in this paper since the length of mode 2 is very short compared with the total commutation time.

When thyristor $T11$ is turned off, mode 3 (Fig. 3(d)) begins and continues until the commutation capacitor current $i_c(t)$ reaches the dc link current value I_d. Fig. 3(d) shows that the oncoming phase thyristor is reverse biased by the voltage drop across R_x plus the capacitor C_r voltage. The voltage stress of the main thyristor $T13$ is determined by the capacitor C_r voltage stress if the voltage drop over R_x is small. This operation eliminates the device voltage stress problem. The operation of the commutation circuit can be understood easily if R_x is set to zero and the diode $D32$ is replaced by a diode string. When $i_c(t)$ reaches I_d, mode 4 (Fig. 3(e)) begins, and the commutation capacitor C is charged linearly by the dc link current. The main thyristor $T11$ is in the forward blocking state during this mode.

Mode 4 ends when $v_c(t)$ equals $v_r(t)$, and mode 5 begins by turning on $T13$ (Fig. 3(f)). Although the capacitor C_r is discharged through the interval from mode 1 to mode 4, it is charged through the next two modes by the remaining energy of the leakage reactance of the induction motor. In mode 5, thyristor $A23$ is turned off by the conduction of diode $D23$, and the current through $T13$ begins to increase. Since the capacitance C_r is much larger than that of C, C_r may be replaced with a voltage source during this interval. In this case, $i_c(t)$ decreases rapidly and reaches zero. The next state is mode 6 (Fig. 3(g)), where the remaining energy exchange between the capacitor C_r and offgoing phase occurs. When the offgoing phase current reaches zero, the overall commutation ends, which is shown in Fig. 3(h).

Fig. 4 shows the gating signals of the main and auxiliary thyristors of the type-1 inverter, and Fig. 5 shows the various waveforms of the type-1 inverter during one commutation interval. The commutation capacitor voltage and the current are

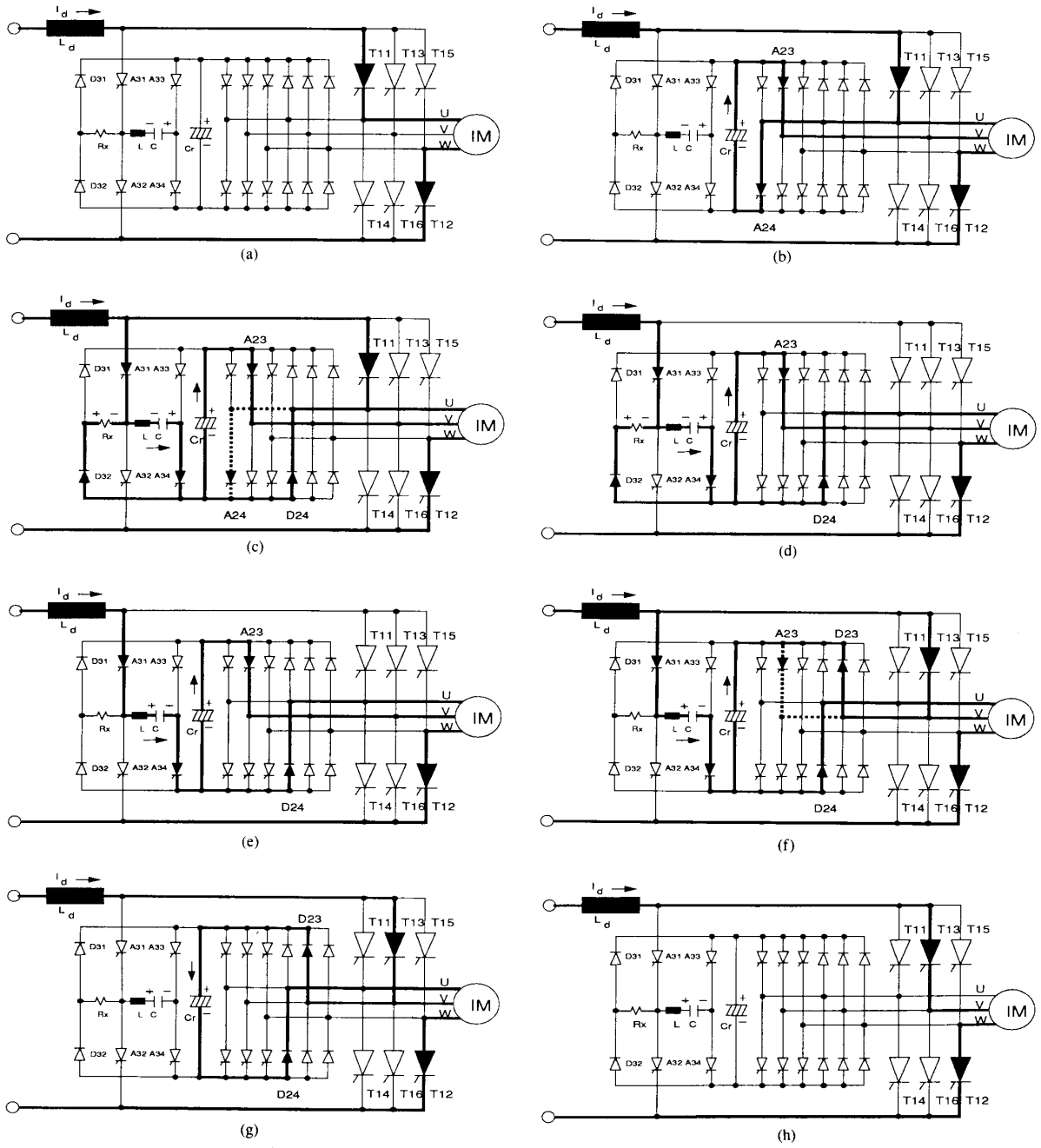

Fig. 3. Commutation mode diagrams of type-1 inverter: (a) Mode 0; (b) mode 1; (c) mode 2; (d) mode 3; (e) mode 4; (f) mode 5; (g) mode 6; (h) mode 7.

scaled down for easy comparison with line currents. It can be seen in Fig. 5 that the discharging time T_d is composed of the intervals from mode 1 to mode 4, and the recovery time T_r is determined mainly by the length of mode 6. Transition from the discharging mode to the recovery mode occurs during mode 5.

B. Type-2 Inverter

The initial state with $T11$ and $T12$ conducting is defined as mode 0. Mode 1 (Fig. 6(b)) begins by turning on thyristors $A31$ and $A34$ in order to turn off the offgoing thyristor $T13$. After a certain delay time T_1, mode 2 begins by turning on the thyristor S_x in order to shorten the linear discharging time by increasing the capacitor discharging rate (Fig. 6(c)). Mode 3 begins when the commutation capacitor voltage reaches zero by turning on the auxiliary thyristor $A23$ in order to discharge the part of the stored energy of the capacitor C_r through the oncoming phase (Fig. 6(d)). This approach eliminates the problem of the device voltage stress for the hard commutated inverter since the summed

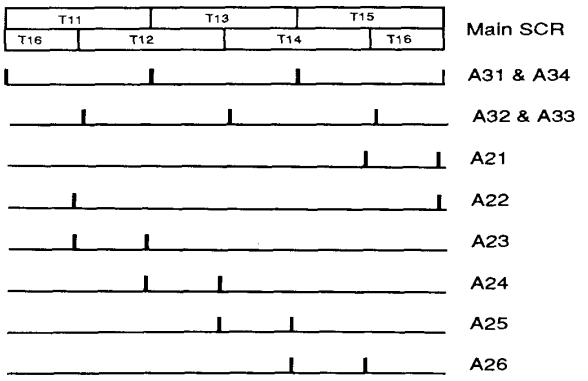

Fig. 4. Gating signals of type-1 inverter.

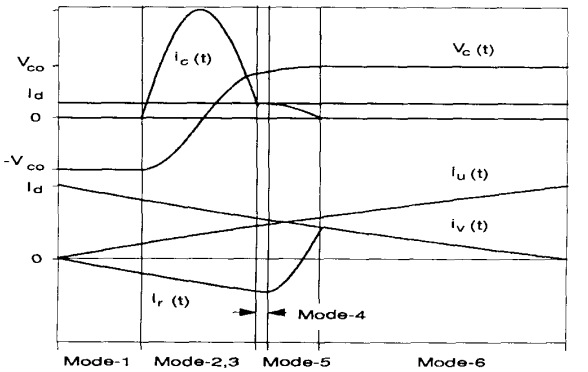

Fig. 5. Various waveforms of type-1 inverter during commutation interval.

voltage of the commutation capacitor and the energy recovery capacitor equals that of the energy recovery capacitor. The next state can be mode 4 (Fig. 6(e)) or mode 5 (Fig. 6(f)); however, mode 5 does not occur in most cases, except for the transient case.

When the reactor current $i_x(t)$ becomes zero, mode 4 begins. During this interval, the commutation capacitor is charged linearly by the dc link current until the oncoming phase thyristor $T13$ is forwardly biased. Since the length of mode 4 is dependent on the three factors (the dc link current, the commutation circuit parameters L, C, and the length of mode-1), it is possible to control the length of this interval (discharging interval) to some extent by varying T_1. When $T13$ is turned on, mode 6 begins, and the auxiliary thyristor $A23$ is turned off by the conduction of $D23$ (Fig. 6(g)). In this mode, the remaining energy of the leakage reactance of the induction motor is transferred to the paralleled capacitors C and C_r. Mode 6 ends when the offgoing phase current reaches zero and the overall commutation ends, which is shown in Fig. 6(h).

Fig. 7 shows the gating signals of the main and the auxiliary thyristors of the type-2 inverter, from which it is shown that the operations of the two inverters are somewhat different from each other. Fig. 8 shows the various waveforms of the type-2 inverter during one commutation interval. The commutation capacitor voltage and the current are also scaled down for easy comparison with line currents. It can be seen from Fig. 8 that the discharging time T_d is composed of the intervals mode 3 and mode 4, and the recovery time T_r is determined by the length of mode 6.

IV. Commutation Mode Analyses of Two Types of Inverters

The series equivalent circuit is used for a 5-hp induction motor [1], and the parameters and relationships used for the simulations and analyses of the inverter operations are given in Table I and Table II, respectively. In addition, the equivalent circuits corresponding to the respective modes of type-1 and type-2 inverters can be obtained from Figs. 3 and 6, respectively. All of the equations related to the commutation modes are given in Table III (and the corresponding equation numbers to respective modes are given in Table IV). Detailed analyses of the proposed inverters can be obtained using those equations; however, simplified analyses are given in this section through appropriate approximations under the following assumptions:

1) Back EMF variation during commutation interval is negligible.
2) Effects of bypassing currents are negligible.
3) Effects of R_x and R are negligible.
4) DC link current is constant during the commutation interval.
5) At the start of each mode, $t = 0$.
6) The respective mode length is T_i (i is the mode number)
7) Motor operates on a constant flux mode up to the base frequency.

A. Type-1 Inverter

1) Mode-1: From (A12), (A15), (A23) and, (A25) in Table III, the line current $i_v(t)$ and the capacitor voltage $v_r(t)$ across C_r become

$$i_v(t) = \frac{V_{ro} - E_m \sin\phi}{Z_r} \sin \omega_r t \tag{1}$$

$$v_r(t) = E_m \sin\phi + (V_{ro} - E_m \sin\phi) \cos \omega_r t \tag{2}$$

where $Z_r = \sqrt{2L_e/C_r}$ and $\omega_r = 1/\sqrt{2L_eC_r}$.

Equations (1) and (2) are good up to mode 4.

2) Mode-2 and Mode-3: If the reverse recovery characteristic of the main thyristor is neglected, the commutation capacitor voltage $v_c(t)$ and current $i_c(t)$ can be obtained from (A5), (A10), (A17), and (A26) as

$$v_c(t) = -Z_x I_\alpha \cos(\omega_x t + \phi_\alpha) \tag{3}$$

$$i_c(t) = I_\alpha \sin(\omega_x t + \phi_\alpha) \tag{4}$$

where $Z_x = \sqrt{L/C}$, $\omega_x = 1/\sqrt{LC}$

$$I_\alpha = \sqrt{I_d^2 + (V_{co}/Z_x)^2} \tag{5}$$

$$\phi_\alpha = \tan^{-1}(Z_x I_d / V_{co}). \tag{6}$$

If the peak current of the commutation capacitor shown in Fig. 5 is sufficiently greater than the dc link current I_d, the interval of mode 2 and mode 3 can be approximated as

$$T_{23} \approx \sqrt{LC}(\pi - Z_x I_d / V_{co}). \tag{7}$$

The second term of (7) becomes negligible, compared with the first term if the commutation circuit is well designed, whereby the interval of mode 2 and mode 3 become constant, irrespective of the load current.

3) Mode-4: From (A9) and (A20), the voltage and the cur-

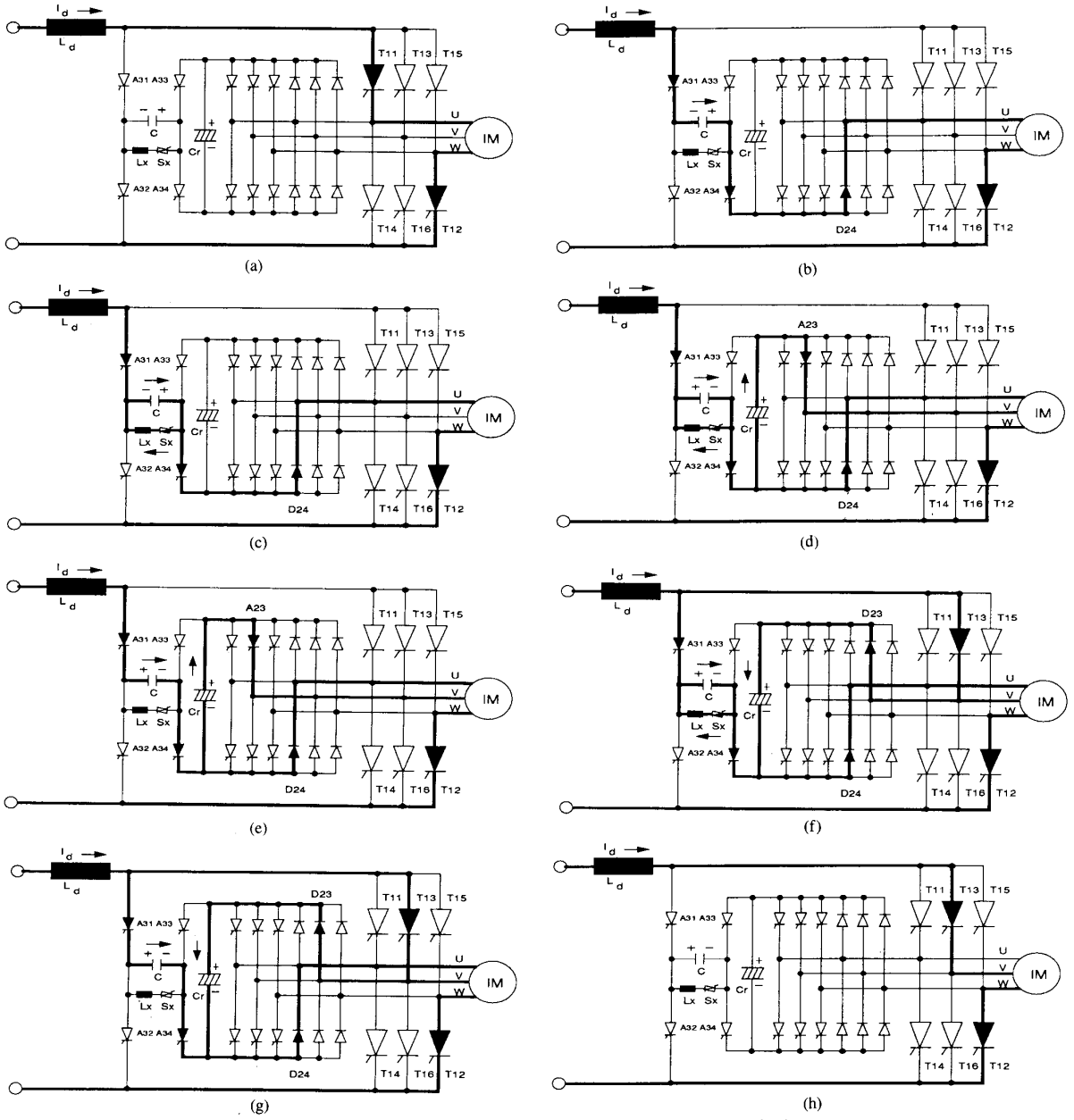

Fig. 6. Commutation mode diagrams of type-2 inverter: (a) Mode 0; (b) mode 1; (c) mode 2; (d) mode 3; (e) mode 4; (f) mode 5; (g) mode 6; (h) mode 7.

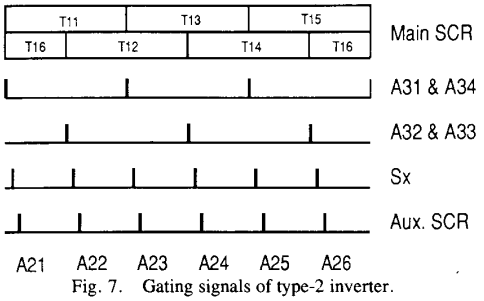

Fig. 7. Gating signals of type-2 inverter.

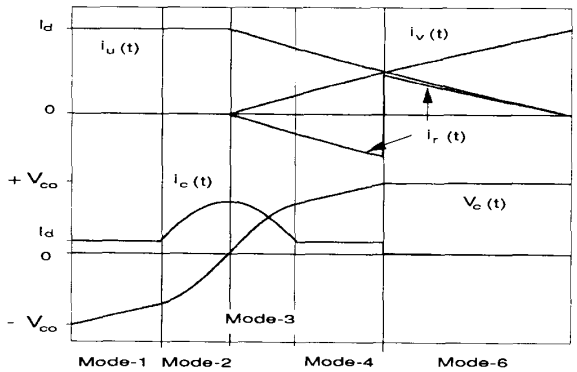

Fig. 8. Various waveforms of type-2 inverter during commutation interval.

TABLE I
PARAMETERS USED FOR THE SIMULATION OF THE INVERTER

$R_s = 0.45\ \Omega$	$R_r = 0.47\ \Omega$	$L_s = 1.26$ mH	$L_r = 2.94$ mH
$L_m = 76$ mH	$I_{sm} = 14$ A [rms]	$V_{sm} = 220$ V [rms]	$f_b = 60$ Hz
$L = 0.5$ mH	$C = 5{,}10\ \mu$F	$R_x = 0.1$–$0.4\ \Omega$	$f_s = 60$ Hz
$C_r = 50\ \mu$F	$L_x = 1$ mH	$W_{slm} = 13.6$ rad/s	$T_{off} = 100\ \mu$s

TABLE II
BACK EMF OF THE INDUCTION MOTOR AND I_d FOR CONSTANT FLUX OPERATION

$E_u(t) = V_m \sin(2\pi f_S t + \phi + 5\pi/6)$
$E_v(t) = V_m \sin(2\pi f_S t + \phi + \pi/6)$
$E_w(t) = V_m \sin(2\pi f_S t + \phi - \pi/2)$
$E_{uv}(t) = -E_m \sin(2\pi f_S t + \phi)$
$E_{uw}(t) = E_m \cos(2\pi f_S t + \phi + \pi/6)$
$\phi = \tan^{-1}(R_r/L_m\omega_{Sl})$

$$V_m = \frac{2\pi f_S L_m I_S}{\sqrt{1 + (\omega_{Sl} L_m / R_r)^2}}$$

$$I_d = \frac{E_g}{2\sqrt{6} f_b L_m} \sqrt{\frac{R_r^2 + \omega_{Sl}^2 (L_r + L_m)^2}{R_r^2 + (L_r \omega_{Sl})^2}}$$

$E_m = \sqrt{3}\, V_m$
I_s = Stator current [rms] of the induction motor
E_g = Airgap voltage [rms] at base frequency f_b

TABLE III
DESCRIBING EQUATIONS OF COMMUTATION MODES FOR TWO TYPES OF INVERTERS

$i_u(t) = 0$	(A1)	$i_u(t) + i_v(t) = I_d$	(A13)
$i_u(t) = I_d$	(A2)	$i_r(t) + i_v(t) = I_d$	(A14)
$i_v(t) = 0$	(A3)	$i_r(t) + i_v(t) = 0$	(A15)
$i_v(t) = I_d$	(A4)	$i_r(t) + i_v(t) + i_c(t) = I_d$	(A16)
$i_S(t) = 0$	(A5)	$i_S(t) + i_c(t) - i_x(t) = I_d$	(A17)
$i_S(t) = I_d$	(A6)	$i_r(t) + i_v(t) + i_c(t) + i_x(t) = I_d$	(A18)
$i_x(t) = 0$	(A7)	$v_c(t) = -V_{co} + I_d t/C$	(A19)
$i_c(t) = 0$	(A8)	$v_c(t) = V_{C3} I_d t/C$	(A20)
$i_c(t) = I_d$	(A9)	$L_{Sn}\dfrac{di_S(t)}{dt} = -R_x i_x(t)$	(A21)
$v_c(t) = -V_{co}$	(A10)	$L_{Sn}\dfrac{di_S(t)}{dt} = v_c(t) - v_r(t)$	(A22)
$v_c(t) = +V_{co}$	(A11)	$C_r\dfrac{dv_r(t)}{dt} = -i_r(t)$	(A23)
$v_r(t) = +V_{ro}$	(A12)	$C\dfrac{dv_c(t)}{dt} = i_c(t)$	(A24)

$$2L_e\frac{di_v(t)}{dt} = -2Ri_v(t) - RI_d + v_r(t) - E_{vu}(t) \quad \text{(A25)}$$

$$L\frac{di_c(t)}{dt} = -R_x i_x(t) - v_c(t) \quad \text{(A26)}$$

$$L\frac{di_x(t)}{dt} = -R_x i_x(t) + v_c(t) = 0 \quad \text{(A27)}$$

$$L\frac{di_c(t)}{dt} = -R_x i_x(t) - v_c(t) + v_r(t) \quad \text{(A28)}$$

TABLE IV
CORRESPONDING EQUATION NUMBERS FOR EACH COMMUTATION MODE

	Type No.	Mode 0	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5	Mode 6	Mode 7
$i_u(t)$	1	A2	A13	A13	A13	A13	A13	A13	A1
$i_u(t)$	2	A2	A2	A2	A13	A13	A13	A13	A1
$i_v(t)$	1	A3	A25	A25	A25	A25	A25	A25	A4
$i_v(t)$	2	A3	A3	A3	A25	A25	A25	A25	A4
$i_s(t)$	1	A6	A6	A21	A5	A5	A21	A6	A6
$i_s(t)$	2	A6	A5	A5	A5	A5	A22	A22	A6
$i_x(t)$	1	A7	A7	A17	A17	A7	A17	A7	A7
$i_x(t)$	2	A7	A7	A27	A27	A7	A27	A7	A7
$i_c(t)$	1	A8	A8	A26	A26	A9	A28	A8	A8
$i_c(t)$	2	A8	A9	A17	A17	A9	A17	A17	A8
$i_r(t)$	1	A15	A15	A15	A15	A15	A16	A14	A15
$i_r(t)$	2	A15	A15	A15	A15	A15	A18	A16	A15
$v_c(t)$	1	A10	A10	A24	A24	A20	A24	A11	A11
$v_c(t)$	2	A10	A19	A24	A24	A20	A24	A24	A11
$v_r(t)$	1	A12	A23	A23	A23	A23	A23	A23	A12
$v_r(t)$	2	A12	A12	A23	A23	A23	A23	A23	A12

rent of the commutation capacitor become

$$V_c(t) = V_{c3} + I_d t/C \tag{8}$$

$$i_c(t) = I_d. \tag{9}$$

This mode ends when $v_c(t) = v_r(t)$ but may be skipped over, depending on the load conditions. Using (1) and (2), the final conditions of mode 4 are given as

$$I_{V4} = \frac{V_{ro} - E_m \sin\phi}{Z_r} \sin \omega_r T_d \tag{10}$$

$$V_{r4} = E_m \sin\phi + (V_{ro} - E_m \sin\phi) \cos \omega_r T_d \tag{11}$$

$$V_{c4} = V_{r4}. \tag{12}$$

4) Mode-5 and Mode-6: During mode 5, the polarity of $i_r(t)$ is changed from a negative to a positive value, whereby $A23$ is turned off and $D23$ conducts. Since the voltage buildup on C_r is negligible during this interval, the voltage and current of the commutation capacitor become, from (A17), (A24), and (A28) to be

$$v_c(t) \approx V_{c4} + Z_x I_a \sin \omega_x t \tag{13}$$

$$i_c(t) \approx I_d \cos \omega_x t. \tag{14}$$

Equation (14) shows that the length of mode 5 is determined only by the commutation circuit parameters (L and C). Since mode 5 ends when the commutation current reaches zero, the interval length of mode 5 can be written as

$$T_5 = 0.5\pi\sqrt{LC}. \tag{15}$$

On the other hand, by using (A14), (A23), and (A25), the oncoming phase current and the capacitor C_r voltage during mode 5 and mode 6 can be written as

$$v_r(t) = E_m \sin(\phi + \omega_s T_d) + Z_r I_\beta \cos(\omega_r t + \phi_\beta) \tag{16}$$

$$i_v(t) = I_d + I_\beta \sin(\omega_r t + \phi_\beta) \tag{17}$$

where

$$I_\beta = \sqrt{\left[(V_{r4} - E_m \sin(\phi + \omega_s T_d))/Z_r\right]^2 + (I_{V4} - I_d)^2} \tag{18}$$

$$\phi_\beta = \tan^{-1} \frac{Z_r(I_d - I_{V4})}{V_{r4} - E_m \sin(\phi + \omega_s T_d)}. \tag{19}$$

Since mode 6 ends when the oncoming phase current reaches the dc link current value, the final conditions are given from (16) and (17) as

$$v_r(t)\,|_{\,t=T_r} = V_{ro} \tag{20}$$

$$i_v(t)\,|_{\,t=T_r} = I_d. \tag{21}$$

5) Capacitor Voltage and Commutation Time in the Steady State: In steady-state operation, the charge balancing across C_r should be satisfied, that is, the discharged energy of C_r must be equal to the recovered energy of C_r. If (16) and (17) are combined by using the initial conditions (10), (11) and the final conditions (20) and (21), the following relationship can be obtained:

$$\begin{aligned}(V_{ro} - E_m \sin(\phi + \omega_s T_d)) \cos \omega_r T_r &= E_m \sin\phi - E_m \sin(\phi + \omega_s T_d) \\ &\quad + (V_{ro} - E_m \sin\phi) \cos \omega_r T_d.\end{aligned} \tag{22}$$

If the variation of back EMF voltage during commutation interval is small enough, (22) can be approximated as

$$\cos \omega_r T_r \approx \cos \omega_r T_d. \tag{23}$$

Equation (23) means the discharging time T_d is very close to the recovery time T_r independent of load condition, which is a very interesting result. From (17), (21), and (23), the discharging time T_d and the final capacitor voltage V_{ro} can also be approximated as

$$T_d \approx \sqrt{2L_eC_r} \sin^{-1} \frac{Z_r I_d}{2(V_{ro} - E_m \sin\phi)} \tag{24}$$

$$V_{ro} \approx E_m \sin\phi + \frac{1}{2} \frac{Z_r I_d}{\sin \omega_r T_d}. \tag{25}$$

Equations (24) and (25) show that the commutation time T_c ($= T_d + T_r$) is closely related to the capacitor voltage V_{ro} for a fixed Z_r. Therefore, once one parameter between T_c and V_{ro} is set, then another parameter is accordingly determined by (24) and (25). If C_r is sufficiently large, (25) can be approximated as

$$V_{ro} \approx E_m \sin\phi + L_e(I_d/T_d). \tag{26}$$

Equation (26) says that V_{ro} is controllable by varying T_d as a function of I_d, and it is independent of C_r. Alternately, V_{ro} can be set to a constant value irrespective of load condition by controlling T_d proportional to I_d. In this case, it is noticeable that the maximum commutation time occurs at maximum load condition. If (24) and (25) are combined with (10), we known that I_{V4} approaches $I_d/2$. This means that the discharging current at the end of discharging interval is about one half of the dc link current.

Fig. 9 shows the various waveforms of the type-1 inverter in the steady state. Since $v_r(t)$ remains almost constant and its ripple component is very low, C_r acts like a voltage source and clamps the spike voltage during commutation interval, whereby the peak voltage stresses of the devices and the motor terminals are all limited to $v_r(t)$. In addition, Fig. 9 shows that the

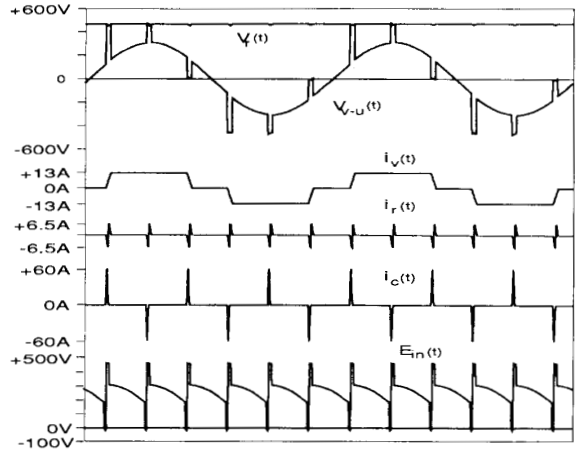

Fig. 9. Various waveforms of type-1 inverter in the steady state (L = 0.5 mH, C = 10 μF, load = 1.0 p.u.)

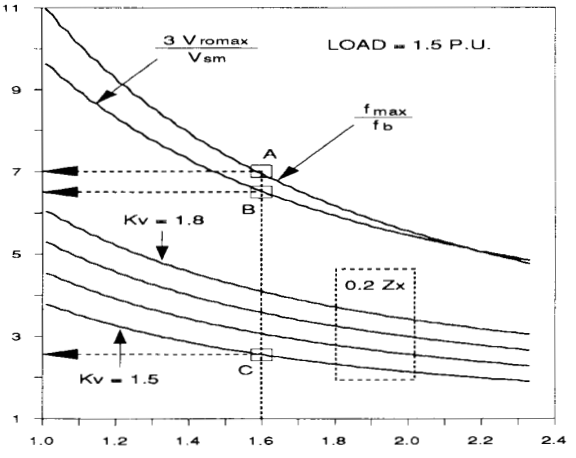

Fig. 10. Design curve for determining the commutation $\pi/\omega_x T_{off}$ circuit elements of type-1 inverter.

inverter input voltage $E_{in}(t)$ swings from near zero to the positive peak value during the commutation interval, and the transient duration is negligible compared with the output period. However, in conventional CSI's, it swings from the negative peak to the positive peak value, and its duration is significant as the operating frequency increases. Thus, there is a noticeable reduction in the ripple of the inverter bus voltage, which correspondingly reduces the dc link current ripple—this property is obtained by employing the SRC concept and the soft commutation circuit.

6) Commutation Circuit Design Procedure and Control Algorithm: Using the results of the commutation mode analyses, the commutation circuit elements (L, C, R_x) can be easily determined on the bases of the safe commutation of main thyristor and the minimization of V_{co}. By using (12), (13), and (15), the final commutation capacitor voltage V_{co} can be approximately written as

$$V_{co} \approx V_{r4} + Z_x I_d \approx V_{ro} + Z_x I_d. \tag{27}$$

Equation (27) says that the commutation capacitor voltage V_{co} depends on V_{ro} and Z_x. Since the controllable interval of T_d is only T_1, the worst condition occurs when $T_1 = 0$. If the maximum value of V_{co} is set to k_v times V_{romax} when $T_1 = 0$ and $I_d = I_{dmax}$, the following two relationships should be satisfied:

$$V_{comax} \approx V_{romax} + Z_x I_{dmax} \le k_v V_{romax} \tag{28}$$

$$T_d \approx T_{23} + 0.5T_5 \approx 1.25\pi\sqrt{LC} \tag{29}$$

where it is assumed that a half of period T_5 belongs to the discharging interval, and $T_4 = 0$, which is true under heavy load condition.

By using (25), (28), and (29), we can obtain Fig. 10, which shows the normalized quantities ($3V_{romax}/V_{sm}$, f_{max}/f_b and $Z_x/5$) as a function of T_d (normalized value by the main thyristor turn-off time T_{off}) for several k_v, where V_{sm}, f_b, and f_{max} denote the nameplate line-to-line rms voltage, the base frequency of the motor, and the maximum operating frequency of the inverter, respectively. The lower and the upper limits of T_d are set 1.25 times T_{off} and T_{dmax}, respectively, where T_{dmax} is given by the allowable minimum value of V_{ro}, e.g., 1.2 times E_m.

If T_d is set, the resultant V_{romax}, f_{max}, and Z_x are determined by points A, B, and C of Fig. 10, respectively. In addition, if the voltage drop allowable across R_x is k_R times V_{comax}, R_x is given by the following relationship:

$$R_x I_\alpha = R_x \sqrt{I_{dmax}^2 + (V_{comax}/Z_x)^2} \le k_R V_{comax}. \tag{30}$$

Therefore, the three passive elements (L, C, R_x) can be determined by using (25), (28)–(30) or Fig. 10 and (30). Fig. 10 shows that it is not necessary to control T_1 or effectively T_d as a function of I_d because it is sufficient to set $T_1 = 0$ in most applications. However, it would be necessary to control T_1 when a heavy load is applied abruptly. In such a case, the relationships between T_1 and I_d for maintaining V_{romax} as a desired value can be written as

$$T_1 \approx T_d - T_{23} - 0.5T_5 \approx k_d I_d - 1.25\pi\sqrt{LC} \tag{31}$$

$$k_d = L_e/(V_{ro} - E_m \sin\phi) \approx L_e/V_{romax}. \tag{32}$$

Determination of T_1 can be easily implemented by comparing the right terms of (31) with a sawtooth waveform synchronized to the inverter gating signals.

B. Type-2 Inverter

1) Mode-1: From (A9) and (A19) in Table III, $v_c(t)$ and $i_c(t)$ across C become

$$v_c(t) = -V_{co} + I_d t/C = -V_{ro} + I_d t/C \tag{33}$$

$$i_c(t) = I_d. \tag{34}$$

This mode determines the length of the discharging interval and V_{ro}.

2) Mode-2: From (A24) and (A27) in Table III, $v_c(t)$ and $i_c(t)$ can be written as

$$v_c(t) = -\hat{Z}_x \hat{I}_\alpha \cos(\hat{\omega}_x t + \hat{\phi}_\alpha) \tag{35}$$

$$i_c(t) = \hat{I}_\alpha \sin(\hat{\omega}_x t + \hat{\phi}_\alpha) \tag{36}$$

where $\hat{I}_\alpha = I_\alpha|_{V_{co}=-V_{C1}}$, $\hat{\phi}_\alpha = \phi_\alpha|_{V_{co}=-V_{C1}}$, $\hat{Z}_x = \sqrt{L_x/C}$, $\hat{\omega}_x = 1/\sqrt{L_x C}$.

Equations (35) and (36) are good through mode 3, and the

interval of mode 2 can be approximated as

$$T_2 = \sqrt{L_x C}\,\tan^{-1}\left(-V_{C1}/\hat{Z}_x I_d\right). \tag{37}$$

Equation (37) says that the interval length of mode 2 is negligible under heavy load condition. In addition, it is shown in Fig. 8 that the interval of mode 3 approximately equals to that of mode 2.

3) Mode-3 and Mode-4: From (A12), (A15), (A23), and (A25) in Table III, $i_v(t)$ and $v_r(t)$ during mode 3 become

$$i_v(t) = \frac{V_{ro} - E_m \sin\hat{\phi}}{Z_r} \sin\omega_r t \tag{38}$$

$$v_r(t) = E_m \sin\hat{\phi} + \left(V_{ro} - E_m \sin\hat{\phi}\right)\cos\omega_r t \tag{39}$$

where $\hat{\phi} = \phi + \omega_s T_1 + \omega_s T_2$.

Using (A9) and (A20) in the Appendix, $v_c(t)$ and $i_c(t)$ during mode 4 can be written as (8) and (9), respectively. Equations (38) and (39) are good through mode 4, and Fig. 8 shows that the interval of mode 4 approximately equals that of mode 1 in the steady state.

4) Mode-5 and Mode-6: If C_r is much larger than C, from (A14) and (A25) in Table III, $i_v(t)$ and $v_r(t)$ across C_r become

$$v_r(t) = E_m \sin\left(\hat{\phi} + \omega_S T_d\right) + Z_r \hat{I}_\beta \cos\left(\omega_r t + \hat{\phi}_\beta\right) \tag{40}$$

$$i_v(t) = I_d + \hat{I}_\beta \sin\left(\omega_r t + \hat{\phi}_\beta\right) \tag{41}$$

where $\hat{I}_\beta = I_\beta|_{\phi=\hat{\phi}}$, $\hat{\phi}_\beta = \phi_\beta|_{\phi=\hat{\phi}}$.

5) Capacitor Voltage and Commutation Time in the Steady State: In steady-state operation, the charge balancing across C_r should be satisfied, as in the case of the type-1 inverter. Therefore, if the discharging time and the recovery time are denoted to T_d ($= T_3 + T_4$) and T_r ($= T_6$), respectively, the relationships of (23) to (26) are also satisfied in the type-2 inverter. From the commutation mode analysis, the total commutation time T_c can be written as

$$T_c \approx T_1 + T_2 + 2T_d \approx 3T_d. \tag{42}$$

Equation (42) says that the discharging time is controllable by T_1, and from (25), V_{ro} is also controllable. On the other hand, compared with the type-1 inverter, the commutation time T_c of the type-2 inverter is increased by T_d for the same voltage stress V_{ro}.

Fig. 11 shows various waveforms of the type-2 inverter in the steady state. Compared with Fig. 9, there is no major difference between them, except for the inverter input voltage waveform. Since the type-2 inverter employs a hard commutation circuit, $E_{in}(t)$ swings from a negative peak to a positive peak value. However, its effects are negligible owing to the reduced capacitor peak voltage and the short commutation interval length.

6) Commutation Circuit Design Procedure and Control Algorithm: Using the results of the commutation mode analysis, the commutation circuit elements (L_x, C) can be easily determined on the basis of the stable commutation under the minimum and the maximum load conditions. Since the discharging time corresponds to $T_1 + T_2$, it is necessary to control T_1 such that the resultant T_d should satisfy (26) for a given V_{romax}. If T_2 is set to be zero when $I_d = I_{dmax}$, the discharging time and the maximum value of commutation capacitance C_{max} can be written as

$$T_d = \sqrt{L_e C_{max}} \tag{43}$$

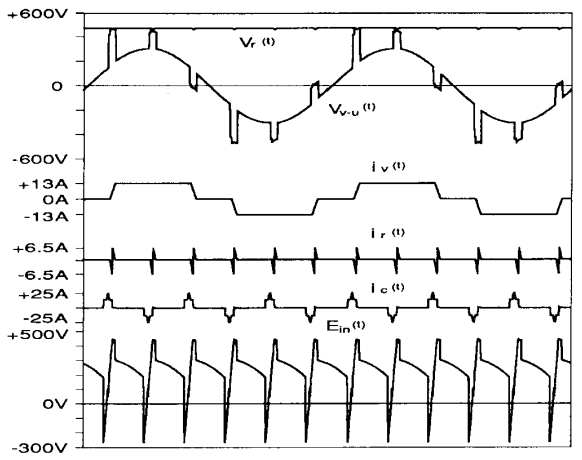

Fig. 11. Various waveforms of type-2 inverter in the steady state (L_x = 1 mH, C = 10 μF, load = 1.0 p.u.).

$$C_{max} = \frac{I_{dmax}}{18 f_{max} V_{romax}}. \tag{44}$$

On the other hand, for the purpose of stable commutation under the light load condition and the maximum operating frequency, the following relationship should be met:

$$2T_{off} \le \pi\sqrt{L_x C_{max}} \le 2\sqrt{L_e C_{max}} \tag{45}$$

where $T_1 = 0$ is regarding the worst condition. Since (45) determines only the maximum and the minimum values of L_x, it is necessary to assign another constraint on L_x. If the current stress on the commutation capacitor at no load is no greater than that of the maximum load condition, the following relationship should be met:

$$\sqrt{L_x} = \frac{\pi C_{max}}{4\sqrt{L_e}}\left(\frac{V_{C1}}{I_{dmax}}\right)^2 \tag{46}$$

where V_{C1} denotes the commutation capacitor voltage at the end of mode 1 and depends on the control scheme on T_1.

By using (43)-(45), we can obtain Fig. 12, which shows the normalized quantities (V_{romax}/V_{sm} and f_{max}/f_b, and L_x in millihenrys and C_{max} in microfarads) as a function of T_d (normalized by T_{off}). The lower and the upper limits of T_d are set to T_{off} and T_{dmax}, respectively. If T_d is set, then the resultant f_{max}, V_{romax}, C_{max}, and L_x are determined by points P, Q, R, and S respectively, of Fig. 12.

Since the control scheme of T_d is similar to the case of the type-1 inverter, the relationship between T_1 and I_d can be written as

$$T_1 \approx T_d - T_2. \tag{47}$$

However, from (37) and (47), we know that it is not simple to determine T_1 as a function of I_d. Considering (43), it is reasonable to use a constant delay time, in which case T_1 can be written as

$$T_1 \approx \sqrt{L_e C}. \tag{48}$$

V. Simulation and Experimental Results

Fig. 13 shows the capacitor voltage stresses of the two inverter types. The discharging time is controlled by (31) and

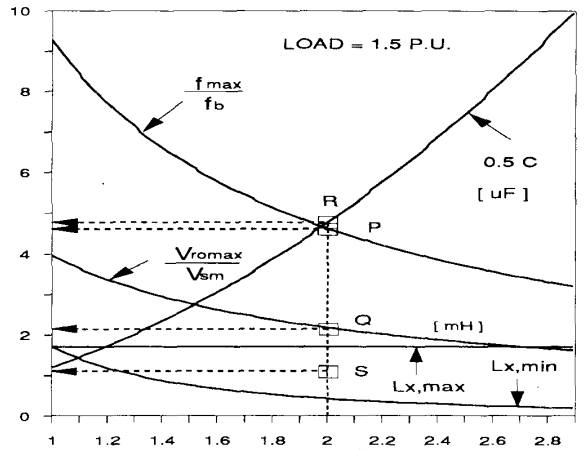

Fig. 12. Design curve for determining the commutation $\sqrt{L_eC}/T_{off}$ circuit elements of type-2 inverter.

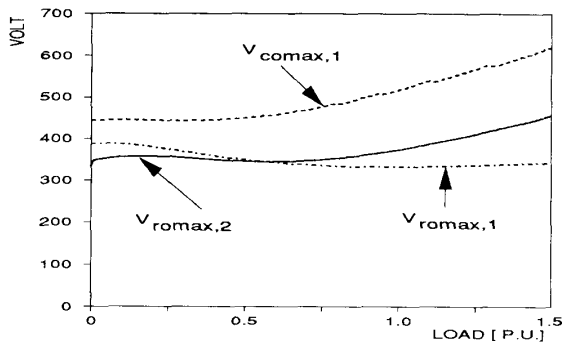

Fig. 13. Commutation and recovery capacitor voltages of the two types of inverters versus load.

(48) for respective inverters. Fig. 13 shows that the V_{romax} are similar to each ohter; however, the commutation capacitor voltage V_{comax} of the type-1 inverter is somewhat higher than V_{romax}, as is expected. Fig. 14 shows that the commutation time of the type-1 inverter increases as the load increases, whereas the commutation time of the type-2 inverter decreases as the load increases. Since these results are obtained when T_1 is very simply controlled, the better results can be obtained by employing a more accurate control scheme.

In Fig. 15, the maximum voltage stresses of the two inverter types are compared with the ASCI as a function of the maximum operating frequency. In addition, the required maximum commutation capacitance of the type-2 inverter and the minimum capacitance of the ASCI are compared. From Fig. 15, we know that the proposed two inverters overcome most of the drawbacks of the ASCI—high device voltage stress, low operating frequency range, large commutation capacitance, etc.

Figs. 16 and 17 show the oscillograms of the commutation capacitor voltage and current for the type-1 and type-2 inverters, respectively. Compared with the waveforms of Figs. 5 and 8, it is shown that the experimental results are in agreement with the simulated waveforms. However, there are some differences between them owing to the neglected effects such as the thyristor recovery characteristics, snubbers, etc. Figs. 18 and 19 show the oscillograms of the line-to-line voltage, the line current, and the recovery capacitor current for the type-1 and type-2 inverters,

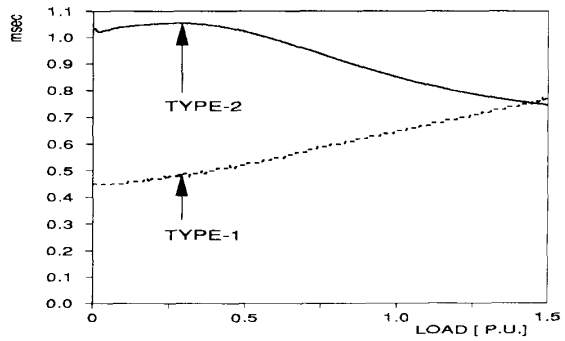

Fig. 14. Commutation times of the two types of inverters versus load.

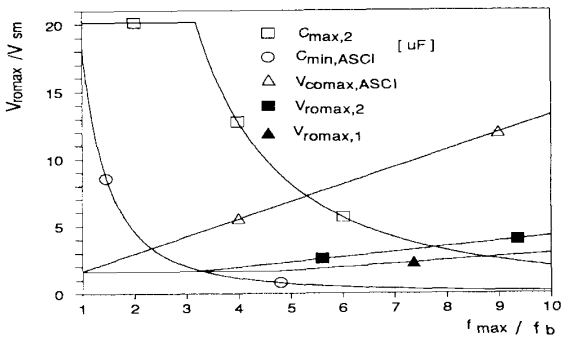

Fig. 15. Comparison between ASCI and the two types of inverters regarding the voltage stress versus maximum operating frequency.

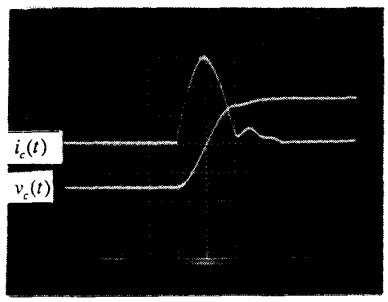

Fig. 16. Oscillograms of the type-1 inverter: commutation capacitor voltage and current (200 V/div, 10 A/div, 0.2 ms/div).

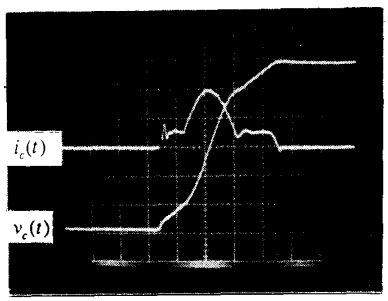

Fig. 17. Oscillograms of the type-2 inverter: commutation capacitor voltage and current (100 V/div, 10 A/div, 0.5 ms/div).

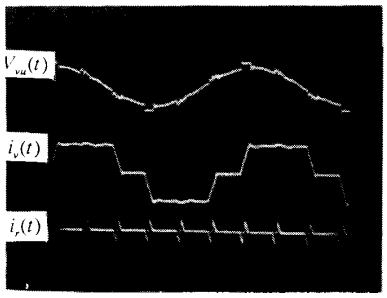

Fig. 18. Oscillograms of the type-1 inverter: line-to-line voltage, line current, and recovery capacitor current (200 V/div, 5 A/div, 5 ms/div).

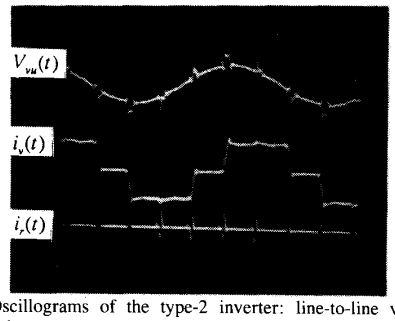

Fig. 19. Oscillograms of the type-2 inverter: line-to-line voltage, line current, and recovery capacitor current (200 V/div, 5 A/div, 5 ms/div).

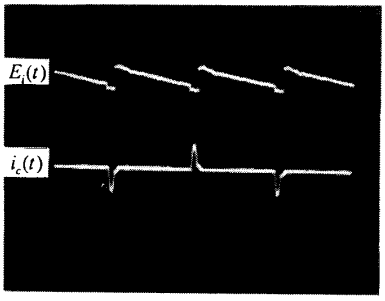

Fig. 20. Oscillogram of the type-1 inverter: inverter bus voltage and commutation capacitor current (200 V/div, 20 A/div, 2 ms/div).

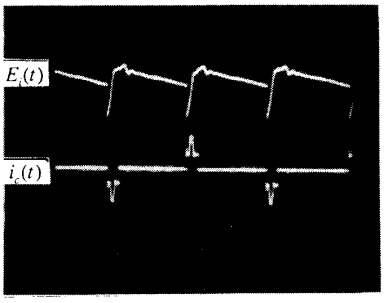

Fig. 21. Oscillogram of the type-2 inverter: inverter bus voltage and commutation capacitor current (200 V/div, 10 A/div, 2 ms/div).

respectively, from which it is shown that the voltage spike of the induction motor is clamped to the recovery capacitor voltage. Figs. 20 an 21 show the oscillograms of the dc bus voltage and the commutation capacitor current for type-1 and type-2 inverters, respectively, from which it is shown that the experimental results are similar to the simulated waveforms of Figs. 9 and 11.

VI. Conclusion

Two different types of new inverter circuits with simultaneous recovery and commutation concept are proposed and analyzed. The two inverter circuits show similar performance regarding the spike voltage clamp during the commutation interval. The type-1 circuit is superior to the type-2 circuit in the maximum operating frequency range by almost 1.5 times; however, there is little difference in performance between them up to a 1.5 p.u. load condition. The main difference in operation comes from the turn-off process of the main thyristor, that is, whether it is soft commutated or hard commutated. Since the new inverters have much lower voltage stresses and a higher operating frequency range in comparison with the conventional ASCI, we think that the proposed inverters would be excellent choices for future drive applications.

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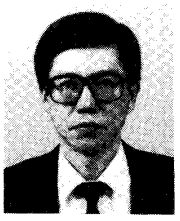

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