A 200MHz / 90dB Gain Range CMOS VGA

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Abstract

A novel CMOS Variable Gain Amplifier (VGA) with high frequency and high dynamic range is proposed. It has a controllable gain range from –45dB to +45dB by external control voltage as well as enhanced operating frequency up to 200MHz. It is fabricated in 0.35μm CMOS technology with the core area of 580μm x 660μm. It consumes only 10.8mA at 3.3V supply voltage.

I. INTRODUCTION

For the latest mobile phone transceivers such as IMT-2000, a VGA with high operating frequency and wide gain control range is one of the crucial components. From now, several VGA circuits using Bipolar, BiCMOS, and CMOS devices were introduced. However, recently a CMOS device is preferably chosen because of its low cost. A 25MHz 20dB variable gain amplifier in 1.2μm CMOS was introduced [1]. This architecture allows the gain to be varied over a wide range –more than 20dB– while bandwidth is almost independent of gain. But for large input signal over several 100mV, a large distortion is expected. The reason is that a large input signal force input transistors to come into the linear or cut-off region. And an input stage composed of PMOS transistors results in slower operation than that of NMOS. Furthermore, many transistors connected to the output nodes make the VGA slow too. A 2mA/3V 71MHz IF Amplifier in 0.4μm CMOS programmable over 80dB range was introduced [2]. In this circuit, in order to enhance operating frequency, an input and a gain control stages are composed of only NMOS transistors, and cascode structures are used to minimize the Miller effect. However, many NMOS transistors at the output node for gain control and PMOS transistors for bias make circuit slow. What is more, for large input signals, it also suffers from distortion. Because large input signals over several 100mV can force the input transistors to come into the cutoff or linear region. Recently, BiCMOS VGA that has high speed/wide dynamic range was introduced [3]. This circuit showed high operating frequency by using bipolar transistors as a gain stage and showed wide dynamic range by using emitter degeneration scheme for large input signal. However, this scheme also has two disadvantages. One is that it is more expensive than CMOS versions, and another is that this input structure has a limitation of operating frequency at low gain state. Because under the low gain and high frequency operating state, some part of emitter currents of an input stage leak to the ground node through parasitic capacitances between the emitter and ground. Therefore, it is very difficult to realize low distortion and large attenuation characteristics at high frequencies with these types of implementation.

II. Design

This paper proposes a novel VGA scheme with high bandwidth and high dynamic range in CMOS technology. A block diagram of the suggested VGA having exponential gain characteristic is shown in Fig. 1. It is composed of two parts. One is a gain block and another is a gain control block.

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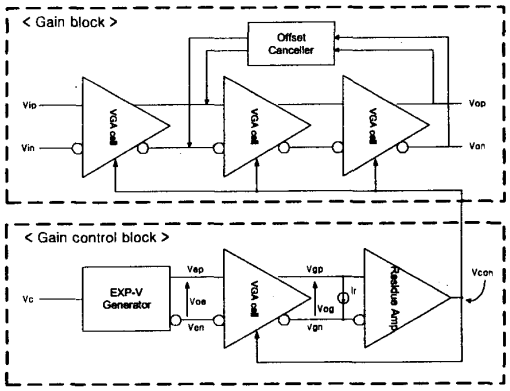

Fig. 1 A block diagram of a VGA

The gain block is composed of 3 VGA cells that have a same structure shown in Fig. 2 and an offset-canceller.

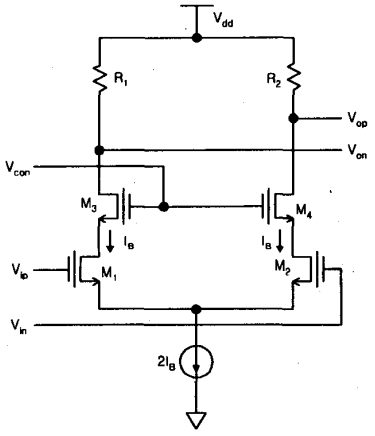

Fig. 2 A circuit schematic of novel VGA cell

The gain control block is composed of an exponential voltage generator, a VGA cell, and a residue amplifier. The VGA cell has a differential cascode structure with only two resistors as loads in order to maximize the operating frequency. Furthermore, bias voltages of the input and the output node is made to have the same value. So, it can make circuit simple and it is possible to connect cell by cell directly without additional bias circuits. The reason of using 3 VGA cells is that this type is easy to achieve large gain and to minimize interferences between the input and the output node by parting the stages physically. Because of large gain of VGA, very small DC offset voltage of VGA can force the output transistor to come into the saturation or the cutoff region. So, the offset-canceller minimizes the offset voltage of the output node and keeps circuit from distortion for large swing signal. The variable gain can be obtained by controlling the voltage Vcon. When the input signal is small magnitude and Vcon is in high-level state, two input transistors M1 and M2 stay in deep saturation region and high gain is obtained. In this state, since the magnitude of input signal is very small, the magnitude of distortion at the output becomes low-level value. On the contrary, when the input signal has large magnitude and the Vcon is in low state, the input transistors stay in deep linear region and low gain with low distortion is obtained. A quiescent point of the VGA cell is moved from Q1 to Q3 according to the control voltages (V_{conL}, V_{conM}, V_{conH}) and the small signal gain is also varied with control voltages as shown in Fig. 3.

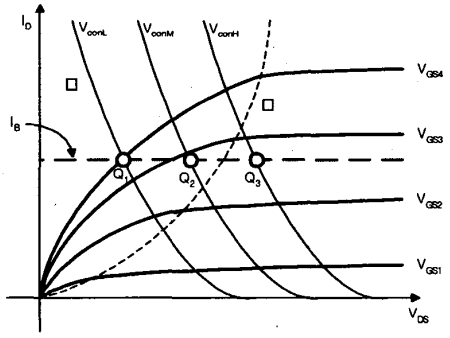

Fig. 3 Load line of VGA

Therefore, the variable gain can be easily obtained by adjusting the control voltage. To achieve an exponential gain characteristic by the control voltage (Vc), at first the input control voltage is scaled down and inverted for a proper polarity and amplitude as shown in Fig 4. The inverted voltage (Vcb) is applied to the emitters of bipolar

transistors B1 and B2.

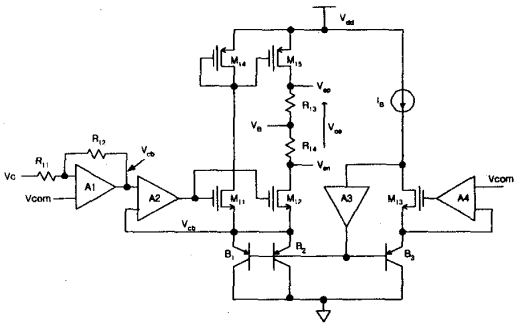

Fig. 4 Exponential voltage generator

Then, the currents of M11 and M12 have exponential characteristics, and accordingly, the output voltage (Voe) has the exponential function as represented by

$$Voe = K_1 \bullet EXP(-K_2 \bullet Vc) \quad \text{---------- (1)}$$

A current source I_B and a transistor B_3 are added to regulate the bias current of PNP transistors independent of the process and temperature variation. This exponential voltage (Voe) is applied to the input of VGA cell and then amplified as shown in the gain control block of Fig. 1. A constant voltage (V_k) is generated by an external current source Ir and two resistors (R1 and R2) of VGA cell and then subtracted from the output side of VGA cell. Therefore, if the VGA gain is Av, then the output of VGA cell (Vog) can be expressed as

$$Vog = Voe \bullet Av - V_k = K_1 \bullet EXP(-K_2 \bullet Vc) \bullet Av - V_k \text{------ (2)}$$

$$\text{(where, } V_k = I_r \bullet (R1 + R2))$$

This output voltage is amplified by a residue amplifier, and then the output (Vcon) of the amplifier is fed back to the control node of the VGA cell. In the steady state, the input voltage (Vog) of the residue amplifier becomes almost zero because of the large loop gain of the amplifier. Therefore, the gain of VGA can be written by eq.(3).

$$Av = V_k \bullet K_1^{-1} \bullet EXP(K_2 \bullet Vc) \quad \text{---------- (3)}$$

Finally, the total gain of VGA is given by

$$Av(total) = [V_k \bullet K_1^{-1} \bullet EXP(K_2 \bullet Vc)]^3 = (V_k \bullet K_1^{-1})^3 \bullet EXP(3K_2 \bullet Vc)$$

---------- (4)

Eq.(4) shows the total gain of VGA has exponential form for the control voltage(Vc).

In layout, the main VGA cells are arranged in series to maintain the gain control range by minimizing the feedback or feed-forward effect between cells. And in order to minimize the small signal resistance between a power source and a ground, a residue space of the chip is filled with capacitors. The position of the VGA cell in the gain control block is placed to the nearest side of the main VGA cells for close matching.

III. Experimental results

This chip was packaged and mounted on PCB for testing. The input signal is converted from single to differential structure for testing by a balun and connected with 1KΩ in parallel to match the input impedance. And the output is connected with 680Ω in parallel to match the output impedance and then also converted from differential to single structure by a balun. The experimental result of the gain is presented in Fig. 5 and it shows the gain in dB is quite linear with Vc.

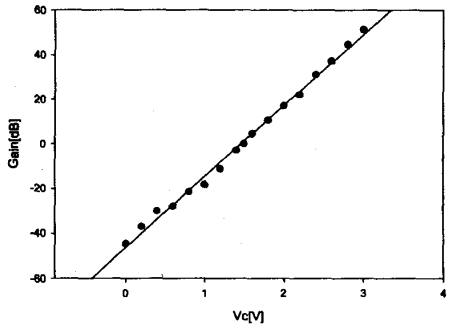

Fig. 5 Gain vs. control voltage (Vc) characteristic

The bandwidth and the IIP3 characteristics are presented in Fig. 6 and Fig. 7 respectively. It is shown that the bandwidth can reaches 200MHz with CMOS technology. The IIP3 has the minimum value of -30dBm

at Vc=3V and it is smaller than other structures.

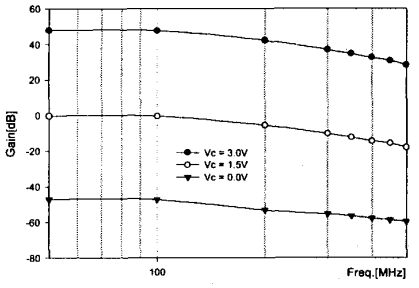

Fig. 6 Bandwidth characteristics

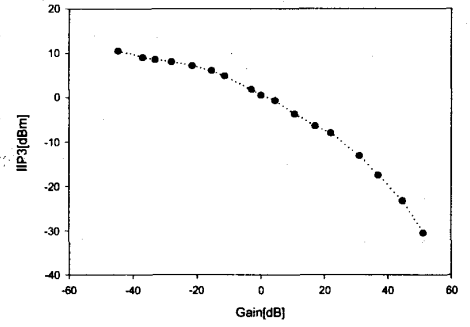

Fig. 7 IIP3 vs. Gain characteristics

This chip is fabricated in 0.35μm CMOS technology and the core area is 580μm x 660μm shown in Fig. 8. It consumes only 10.8mA at 3.3V supply voltage.

IV. Conclusions

This paper describes the design of 200MHz/90dB CMOS VGA. By using a novel scheme, the proposed circuit is proved to have high performance in both operating frequency and gain control range with low distortion in CMOS technology.

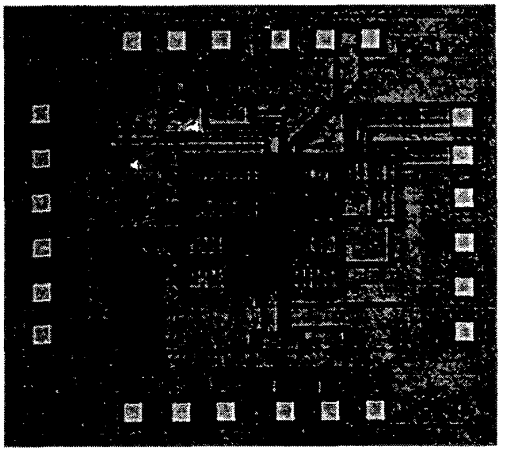

Fig. 8 Chip Microphotograph

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