DSP BASED CONTROL OF HIGH POWER STATIC VAR COMPENSATOR USING NOVEL VECTOR PRODUCT PHASE LOCKED LOOP

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Abstract - This paper presents a new dual loop control using novel vector product phase locked loop(VP-PLL) for a high power static var compensator(SVC) with three-level GTO voltage source inverter(VSI). Through circuit DQ-transformation method, a simple dq-axis equivalent circuit is obtained. From this, DC analysis is carried out to obtain maximum controllable phase angle α_{max} per unit current between the three phase source and the switching function of inverter, and AC open-loop transfer function is given. Because α_{max} becomes small in high power SVC, this paper proposes VP-PLL for more accurate α control. As a result, the overall control loop has dual loop structure, which consists of inner VP-PLL for synchronizing the phase angle with source and outer Q-loop for compensating reactive power of load. Finally, the validity of the proposed control method is verified through the experimental results.

I. INTRODUCTION

In recent years, there have been increased demands for high power static var compensator(SVC) to stablize transmission lines and compensate large industrial loads. In this trend, several control methods for high power SVC have been presented and analysized [1]-[7]. In the early times, approches using thyristor controlled reactor(TCR) were attempted, which had slow transient response in spite of its high power capacity[1]-[2]. After this, control methods with forced-commutated inverter were studied for fast response[3]-[4], and thus with multi-level inverter for high power SVC[5]. Also, with the development of high voltage/current device such as GTO, analysis and control of SVC using three-level GTO inverter were achieved to obtain lower harmoics and higher dc-link voltage at lower switching freguency(f_{sw} < 500Hz)[6]. However, so far, it has not been recognized that the role of PLL for phase synchronization becomes more important because the maximum controllable phase angle difference α_{max}, per unit current between ac source and switching function of inverter is smaller for high power SVC. Hence, a novel vector product phase locked loop(VP-PLL) is proposed in this paper for controlling α more accurately than the conventional hardware PLL.

This paper presents SVC system using three-level GTO voltage source inverter(VSI) for compensation of reactive power using phase angle control. By circuit-DQ transformation, a simple dq-axis equivalent circuit is obtained, from which DC analysis is done for lumped resistor R_s representing total system loss and α_{max}, and AC analysis for open-loop transfer function of system. Thus, overall controller with dual loop structure is composed of outer Q-loop for compensation of reactive power and inner VP-PLL for phase synchronization. In the end, experimental results confirm the usefulness of the proposed controller for high power SVC.

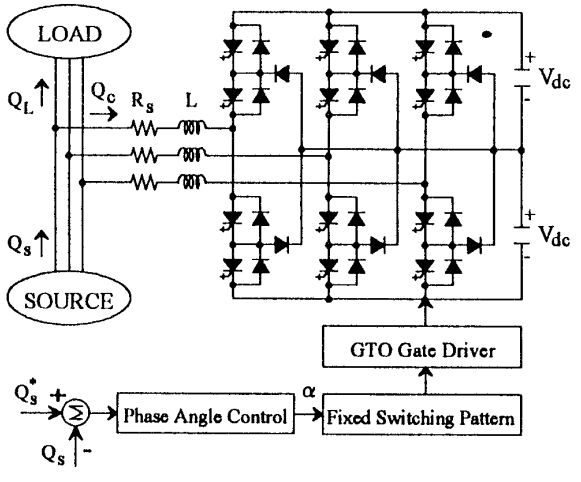

Fig. 1. An overall view of SVC system with three-level GTO inverter.

II. PRINCIPLES OF OPERATION

The proposed SVC system as shown in Fig.1 consists of a three-

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level GTO voltage source inverter, linked reactors, DC-side capacitors, three phase source and load. To compensate the reactive power Q_L injected by the load, the SVC generates reactive power Q_c to obtain unity power factor at the source by making the sum of Q_L and Q_c be zero. Here, the control of Q_c is achieved by controlling a phase angle, so called α-control method, and the operating principle of which is explained by per-phase fundamental equivalent circuit as shown in Fig.2.

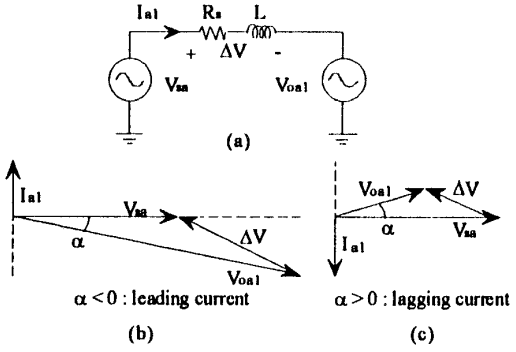


Fig. 2. Phase-angle, α-control method, (a). per-phase fundamental equivalent circuit, (b) and (c). phasor diagram for capacitive and inductive.

That is, by controlling phase angle difference $\alpha(=\alpha_1 - \alpha_2)$ between per-phase angle a_1 of source and α_2 of fundamental switching function imposed to the inverter, the system operates as inductive($\alpha>0$) or capacitive($\alpha<0$). Fig. 3 shows the proposed switching pattern with low switching frequency(180Hz), which is chosen due to the low operating frequency of GTO's as high voltage/current switching devices.

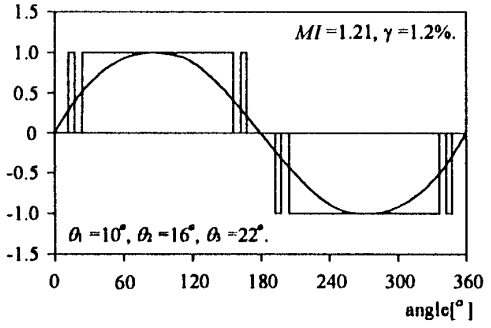


Fig. 3. Optimal switching pattern

Thus, per-phase fundamental output voltage of inverter, V_{oal} can be expressed as follows:

$$V_{oal} = \frac{1}{\sqrt{2}} MI \cdot V_{dc}. \tag{1}$$

where MI is the modulation index of pulse-width modulation (PWM) switching pattern of inverter, and V_{dc} is the voltage of DC-capacitor. Furthermore, the global coltrol of the proposed SVC system is carried out using DSP56001 processor.

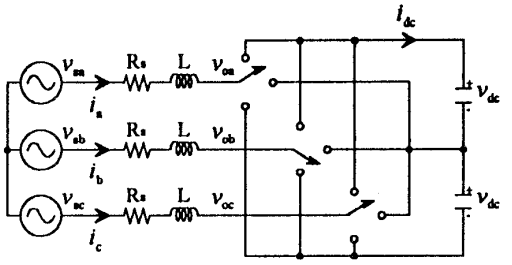


Fig. 4. The simplified main circuit of the SVC system.

III. MODELLING

The main circuit of the presented three-level GTO inverter of Fig. 1 can be simplified as shown in Fig. 4. By applying circuit DQ-transformation method, abc-axis circuit of system is transformed into dq-axis equivalent circuit, where modelling is carried out under the following assumptions [7]-[8]:

1) All switches are ideal,

2) The total loss of system is represented by lumped resistor R_s,

3) Fundamental component is only considered.

Considering the balanced system, source voltage($v_{s,abc}$), current(i_{abc}) and inverter output voltage($v_{o,abc}$) with a switching function S on abc-axis are given as follows:

$$v_{s,abc} = \sqrt{2/3}\, V_s \begin{bmatrix} \sin(\omega t) \\ \sin(\omega t - 2\pi/3) \\ \sin(\omega t + 2\pi/3) \end{bmatrix}, \quad i_{abc} = \begin{bmatrix} i_{oa} \\ i_{ob} \\ i_{oc} \end{bmatrix} \tag{2}$$

$$S = \sqrt{2/3}\, d \begin{bmatrix} \sin(\omega t+\alpha) \\ \sin(\omega t+\alpha-2\pi/3) \\ \sin(\omega t+\alpha+2\pi/3) \end{bmatrix}, \qquad v_{o,abc} = S\, v_{dc}. \tag{3}$$

where V_s is the rms line-to-line voltage of three phase ac source, $\sqrt{2/3}\,d$ denotes the modulation index(MI) of switching function and α is the phase angle between $v_{s,abc}$ and $v_{o,abc}$. An arbitrary abc-axis variable is transformed into the corresponding one on dq-axis by the following transformation matrix K [8].

$$K = \sqrt{2/3} \begin{bmatrix} \cos(\omega t+\alpha) & \cos(\omega t+\alpha-2\pi/3) & \cos(\omega t+\alpha+2\pi/3) \\ \sin(\omega t+\alpha) & \sin(\omega t+\alpha-2\pi/3) & \sin(\omega t+\alpha+2\pi/3) \\ \sqrt{1/2} & \sqrt{1/2} & \sqrt{1/2} \end{bmatrix} \tag{4}$$

Thus, by applying K to Fig. 4, the equivalent circuit transformed in

to dq-axis is obtained as in Fig. 5.

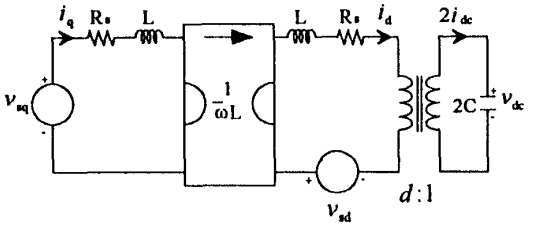


Fig. 5. Circuit DQ-transformed equivalent ciruit of SVC.

IV. ANALYSIS

A. DC ANALYSIS

Through DC analysis of Fig. 5, by assuming that inductor L is short and capacitor C open, the operating points of open-loop system can be characterized. Firstly, the equation of reactive power Q to flow into system is expressed by a function of α as follows [7]:

$$Q = V_{sq} I_d - V_{sd} I_q = \frac{V_s^2}{R_s} \frac{\sin 2\alpha}{2}. \quad (5)$$

Also, based on line to line voltage V_s(1 p.u.) and phase current I_s(1 p.u.) of source, the equivalent lumped resistence R_s and the maximum controllable phase angle α_{max} can be derived as a function of efficiency, η of system where phase angle shift of α_{max} causes 1 p.u. current to flow into the system.

$$R_s = \frac{1-\eta}{\sqrt{3}} \frac{V_s}{I_s} = \frac{1-\eta}{\sqrt{3}} [p.u.], \quad (6)$$

$$\alpha_{max} = \frac{1}{2} \sin^{-1}[2(1-\eta)]. \quad (7)$$

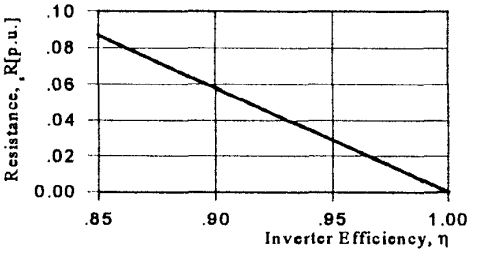


Fig. 6. Plot of R_s versus η.

The values of R_s and α_{max} can be redrawn with respect to η as in Fig. 6 and 7. These values become smaller as the efficiency η is larger. This means that R_s and α_{max} become small at high power applicaion because of high efficiency. For example, α_{max} becomes about 2.9° assuming that η is 0.95 at 100kVAR. Table 1 shows R_s, α_{max} with V_s and I_s for each reactive power capacity of 10k, 100k, 1MVAR, respectively.

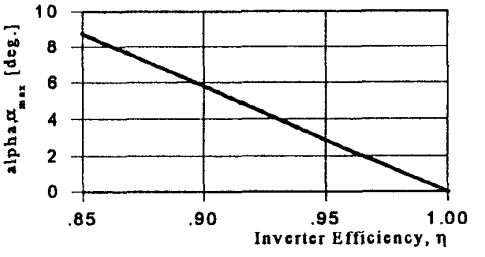


Fig. 7. Plot of α_{max} versus η.

VAR	V_s[V]	I_s[A]	η	R_s	α_{max}
10KVA	220	20	0.90	0.055 pu (0.46 Ω)	5.5°
100KVA	1100	56	0.95	0.03 pu (0.63 Ω)	3°
1MVA	3300	175	0.97	0.017 pu (0.32 Ω)	1.7°

Table. 1. R_s and α_{max} at each reactive capacity.

B. AC ANALYSIS

By solving small signal equations of Fig. 5, open-loop transfer function, $G_Q(s)$ of reactive power $Q(s)$ with respect to phase angle $\alpha(s)$ can be obtained as follows[7]:

$$G_Q(s) = \frac{Q(s)}{\alpha(s)} = \frac{V_s^2(2LC^2s+2R_sCs+D^2)}{2C^2L^2s^3+4LCR_Ss^2+[2C\{R_s^2+(\omega L)^2\}+D^2L]s+D^2R_s}. \quad (8)$$

Using the derived open-loop transfer function, it is possible to design the overall control loop by root locus method.

V. CONCEPT OF VP-PLL

In the conventional α-control compensation method, it becomes important to synchronize the phase angle of switching pattern with source voltage and the response of the control loop should be as fast as possible for accurate α-shift opearation. So far, the hardware PLL as given in Fig. 8 has usually been used for phase synchronization. However, the conventional hardware PLL is inadequate for accurate and fast phase synchronization owing to the following disadvantages: one is the lack of accuracy due to oscillation and noise around the zero-crossing point caused by a comparator, and the other slow response due to the detection of single zero-crossing signal during a half period. On the other hand, as α_{max} becomes

smaller in high power SVC as shown previously, a new PLL conventional hardware PLL.

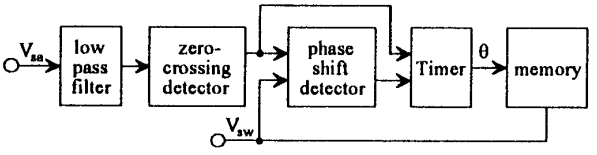


Fig. 8. the block diagram of the conventional hardware PLL.

Fig. 9(a) shows the block diagram of the general phase locked loop(PLL) composed of phase detector(PD), loop filter(LF) and voltage controlled oscillator(VOC). On the other hand, the proposed VP-PLL achieves phase detection by vector producting two normalized dq-vectors as shown in Fig. 9(b): one of which is dq-transformed source voltage $v_{s,qd}$, and the other switching pattern $v_{sw,qd}$ saved with 0.5° interval in memory. Finally, Fig. 9(c) shows the modified VP-PLL for controlling phase angle α corresponding to an arbitrary vector product command VP_{com}, and a PI controller used as LF. Here, the presented VP-PLL can control α more accurately than the conventional hardware PLL due to the following reasons: firstly, the lack of accuracy caused by noise and oscillation doesn't happen in software VP-PLL, and secondly, the slow response due to single phase detection during a period is improved by the presented VP-PD of every 0.5° interval during the period.

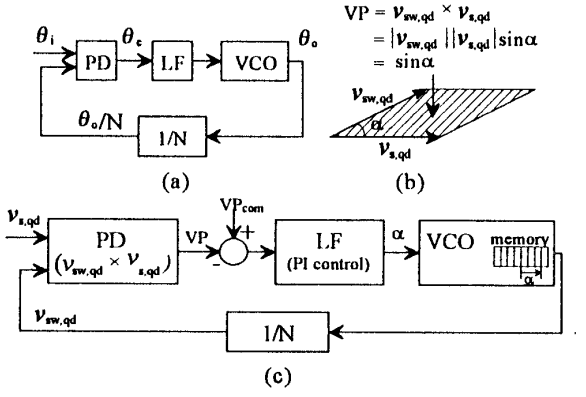


Fig. 9. The concept of VP-PLL (a). the block diargam of an general phase locked loop(PLL), (b). PD using the concept of vector product, (c). modified VP-PLL for controlling α to follow VP_{com}.

VI. CONTROLLER DESIGN

As shown in Fig. 10, the overall controller has dual-loop structure composed of both inner VP-PLL for controlling α to follow VP_{com} obtained from Q-loop and outer Q-loop for compensating reactive power Q for command Q_{com} by using PI controller. Actually gains of each PI controller are designed by root locus method,

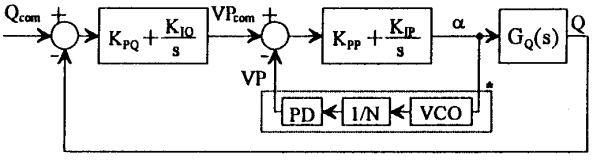


Fig. 10. The overall controller loop of the SVC system.

where the block denoted as an asterisk in Fig. 10 is excluded for simple design. That is, the equation of VP related to α can be expressed as the following equation under the condition of very small value of α:

$$VP = v_{s,qd} \times v_{sw,qd} = |v_{s,qd}||v_{sw,qd}|\sin\alpha = \sin\alpha \cong \alpha. \quad (9)$$

All of the PI gains and the parameter values of the system are given below. In this case, the unit-step response of Q for a step change of Q_{com} reaches the steady state within 2 period as in the simulation result shown in Fig. 11.

$$L = 8mH,\ C = 1000\mu F,\ V_s = 1100V_{rms},\ R_s = 0.63\Omega, \quad (10)$$

$$K_{PP} = 1.0e\text{-}1,\ K_{IP} = 1.0e3, \quad (11)$$

$$K_{PQ} = 2.0e\text{-}6,\ K_{IQ} = 7.6e\text{-}5. \quad (12)$$

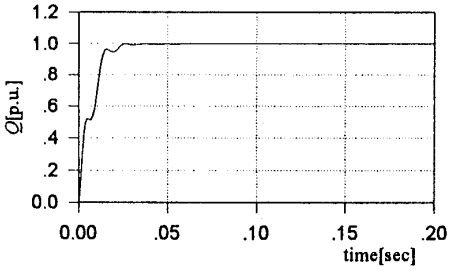


Fig. 11. Response of Q for unit step change of Q_{com}.

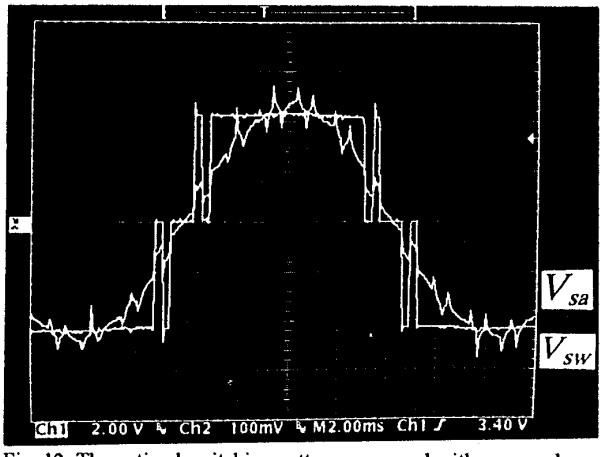
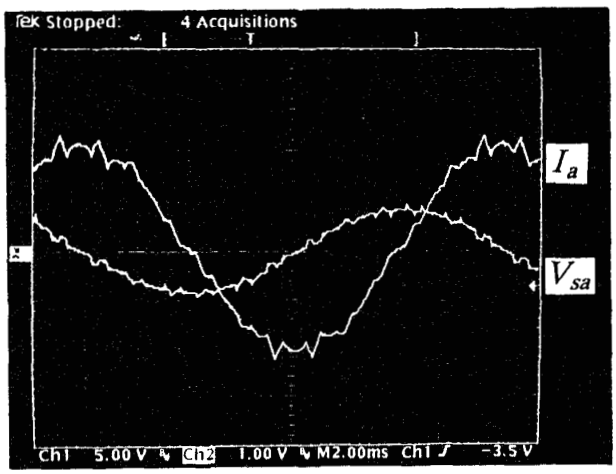
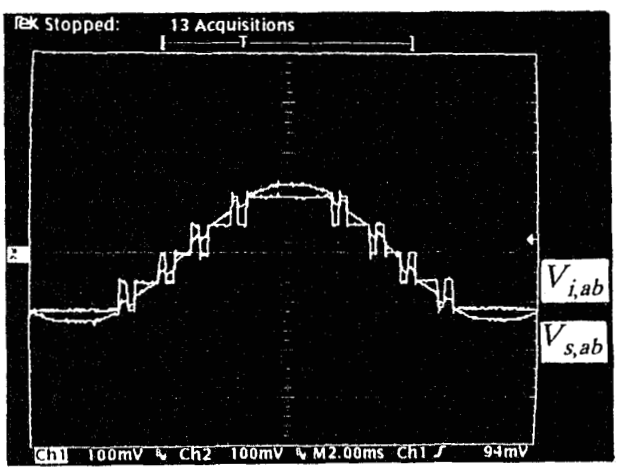


Fig. 12. The optimal switching pattern compared with source phase voltage; source phase voltage v_{sa} (400V/div), switching pattern of inverter v_{sw} (400V/div).

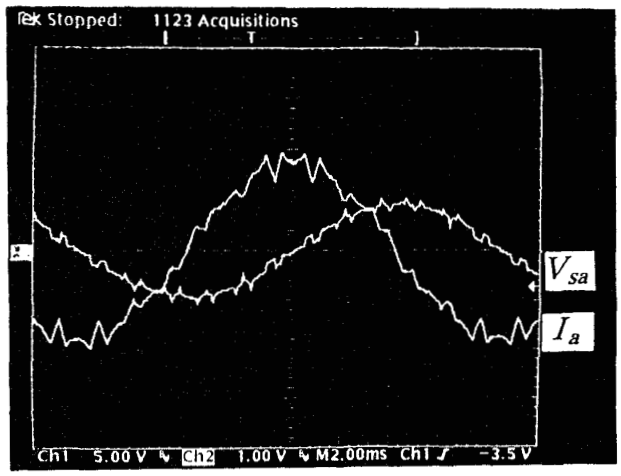


(a)

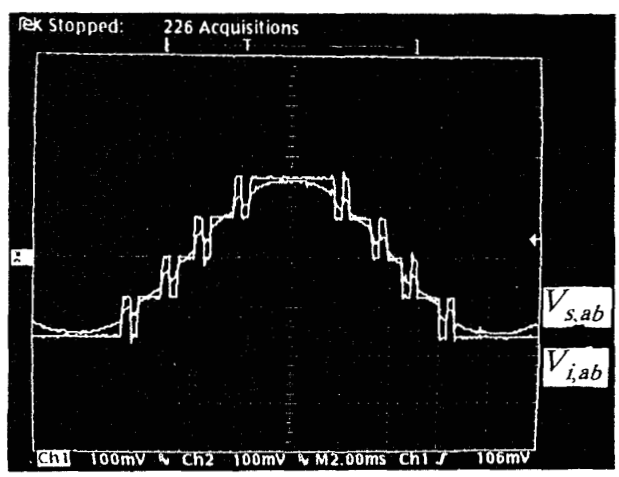


(b)

Fig. 13. Inductive operation for Q_{com} = 50 kVAR. (a) Line current I_a (20A/div) and source phase voltage V_{sa} (1kV/div). (b) Source line-to-line voltage $V_{s,ab}$ (1kV/div) and inverter output line-to-line voltage $V_{i,ab}$ (1kV/div).



(a)



(b)

Fig. 14. Capacitive operation for Q_{com} = -50 kVAR. (a) Line current I_a (20A/div) and source phase voltage V_{sa} (1kV/div). (b) Source line-to-line voltage $V_{s,ab}$ (1kV/div) and inverter output line-to-line voltage $V_{i,ab}$ (1kV/div).

VII. EXPERIMENTAL RESULTS

The validity of the presented control method is verified through the experiment using 50kVA prototype implemented by DSP56001 processor. Here, the parameters of the system and the gains of the PI controllers are the same as the values employed in the simulation of chapter VI. Fig. 12 indicates the optimal switching pattern compared with source phase voltage used in this experiment, the switching frequency of which is considered to be 180Hz in each GTO device. The harmonic components of the source phase voltage as shown in Fig. 12 are due to the switching noise in P.T.(Potential Transformer) caused by switching action at the line side, which do not exist in the actual waveform. Under the inductive operation of Q_{com} = 50kVA, Fig. 13(a) shows line current compared with phase voltage, and Fig. 13(b) line-to-line voltage of source and inveter, where the inverter output has leading current phase(α>0) with smaller magnitude than the source. Fig. 14 indicates the same case as in Fig. 13 under the capacitive operation of Q_{com} = -50kVA, where line-to-line voltage of inverter output has current lagging phase(α<0) with larger voltage magnitude than that of source.

where line-to-line voltage of inverter output has current lagging phase(α<0) with larger voltage magnitude than that of source.

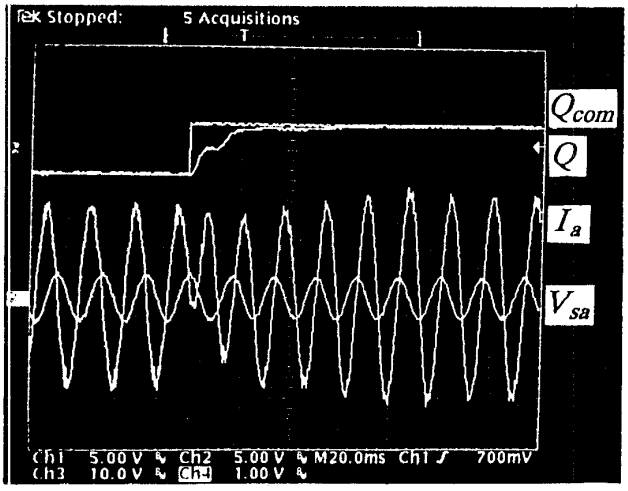


Fig. 15. The transient response for a step change in Q_{com} from capacitive (-50 kVA) to inductive(50 kVA); the desired var command Q_{com}, the actual generated var Q, line current I_a(20A/div) and source phase voltage V_{sa}(2kV/div).

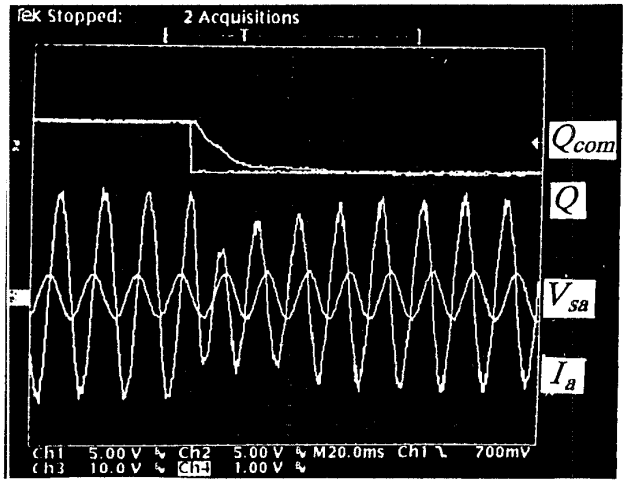


Fig. 16. The transient response for a step change in Q_{com} from inductive (50 kVA) to capacitive(-50 kVA); the desired var command Q_{com}, the actual generated var Q, line current I_a(20A/div) and source phase voltage V_{sa}(2kV/div).

Also, Fig. 15 shows the transient response for a step change of Q_{com} from -50kVA(capacitive) to 50kVA(inductive), and Fig. 16 the contrary case. From Fig. 15 and 16, line current I_a reaches the steady state within 2 period from the step change of Q_{com}, which shows that the presented controller has good performance for an application to high power SVC system using three-level GTO inverter.

VIII. CONCLUSION

The simple equivalent circuit of SVC system is obtained by circuit DQ-transformation and characterized in terms of DC and AC. R_s and α_{max} are derived from DC analysis, and open-loop transfer function is given. Because of smaller α_{max} in high power SVC, a novel method as the proposed VP-PLL is desired for more accurate phase synchronization than the conventional hardware PLL. Therefore, the global control loop is composed of inner VP-PLL for phase synchronization and outer Q-loop for reactive power compensation of load. It is confirmed by the experimental results that the proposed dual loop controller with VP-PLL has good performance to high power application.

REFERENCES

[1] L. Gyugyi, R. A. Otto, T. H. Putman, "Principles and applications of static, thyristor-controlled shunt compensators", *IEEE Trans. Power App. and Sys.*, vol. 97, no. 5, pp. 1935-1945, Sept./Oct. 1978.

[2] L. Gyugyi, "Reactive power generation and control by thyristor circuit", *IEEE Trans. Ind. Appl.*, vol. IA-15, no. 5, pp. 521-532, Sept./Oct. 1979..

[3] L. T. Moran, P. D. Ziogas, and G. Joos, "Analysis and design of a three-phase synchronous solid-state var compensator", *IEEE Trans. Ind. Appl.*, vol. IA-25, no. 4, pp. 598-608, July/Aug, 1989.

[4] G. Joos, L. Moran, and P. D. Ziogas, "Performance analysis of a PWM inverter VAR compensator", *IEEE Trans. Power Electron.*, vol. 6, no. 3, pp. 380-391, July 1991.

[5] Nam S. Choi, Guk C. Cho, and Gyu H. Cho, "Modeling and analysis of a static var compensator using multilevel voltage source inverter", *IEEE/IAS Annual Meeting*, pp. 901-908, 1993.

[6] Guk C. Cho, Gu H. Jung, Nam S. Choi, and Gyu H. Cho, "Analysis and controller design of static var compensator using three-level GTO inverter", *IEEE Trans. Power Electron.*, vol. 11, no. 1, pp. 57-65, Jan. 1996.

[7] C. T. Rim, D. Y. Hu, and G. H. Cho, "Transformers as equivalent circuits of switches: General proofs and DQ Transformation-based analyses", *IEEE Trans. Ind. Appl.*, vol. 26, no. 4, pp. 777-785, July/Aug. 1990.