Novel Soft Switching PWM Converter Using A New Parallel Resonant DC-Link

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ABSTRACT

A novel soft switching PWM converter for high frequency AC/DC and/or DC/AC power conversion is presented by using a new parallel resonant dc-link(PRDCL) and by adopting single phase soft switching(SPSS) technique. The new PRDCL provides variable link pulse position as well as variable link pulse width, which is quite different feature from the other resonant dc-links and thus the PWM capability can be remarkably increased. The SPSS technique is also adopted for further enhancement of PWM capability. Moderate combination of two soft switching operations enables the conventional space vector PWM technique to be used. Due to distinctive advantages including true PWM capability, minimum device voltage stresses(all V_s) and reasonable additional device count(3 devices), the proposed converter can be operated in a wide power range(20-200 KW). Operational principles, analyses and the realization of a space vector PWM of the proposed converter are presented. Simulation results are also shown to verify the operational principle.

I. Introduction

In recent years, the soft switching techniques in static power converters have been received considerable attentions due to their distinctive advantages over the conventional hard switching converters such as high power density, low EMI, low acoustic noise and high dynamic performance which result from the increase in switching frequency. Many converter topologies adopting soft switching techniques have been suggested and extensively studied.[1-14] In special case of voltage source converters, two soft switching approaches have been studied, one is resonant pole approach[2,12-14] and the other is resonant dc-link approach.[1-11]

The resonant pole inverter(RPI)[2,12,13] has advantageous features such as low device voltage stress(V_s), no additional devices, and fairly simple control. However, the power range is limited to several tens of KW because of high current stresses and losses in devices and components. The auxiliary resonant commutated pole inverter(ARCPI) reduces the current stresses and losses in the devices and components, however it is thought to be not cost effective at below 200 KW power level because of the large number of additional devices(6 devices).

For transistor based high frequency power conversion covering 1-200 KW power range, the resonant dc-link approach has rigorously been studied and several converter topologies and control methods were presented.[1-11] Among them, the actively clamped resonant dc-link(ACRDCL) inverter[1] which requires only one additional devices and limits device voltage stresses to 1.3-1.5V_s, is known as one of the most successful topology and covers 1-40 KW power range around 20-60 KHz switching frequency range. The ACRDCL inverter, however, has several disadvantages which are big obstacles in further increases of power range such as subharmonic problem resulted from discrete pulse modulation(DPM), still higher device voltage stress and conduction loss in resonant inductor. So, the possibility of realizing PWM in resonant dc-link converter preserving the advantages of zero switching loss and high switching frequency is quite desirable objective.

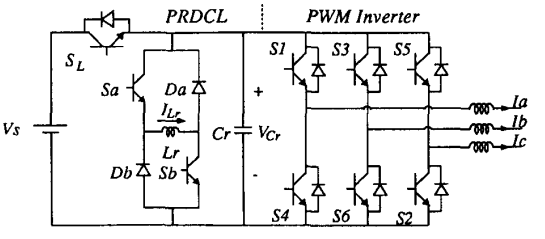

Fig. 1 Circuit topology of the proposed soft switching PWM-PRDCL converter.

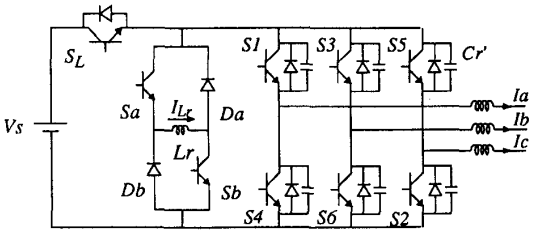

Fig. 2 Circuit topology of the proposed soft switching PWM-PRDCL converter with distributed resonant capacitors.

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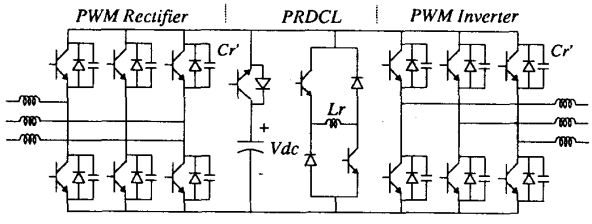

Fig. 3 Extension of the proposed converter to rectifier-inverter with either side soft switching PWM.

To eliminate subharmonic problem, several approaches realizing PWM in resonant dc-link converters were presented.[5-10] Synchronized resonant dc-link converter[5] showed a possibility of PWM operation by allowing the variable link pulse width subject to the limitations of a minimum pulse width. The PWM capability, however, is highly restricted[11] since it can not generate narrow dc-link pulses, and the device voltage stress(1.5-1.8V_s) and conduction losses in devices and components are further increased. References [8] and [9] presented similar approaches which also provide variable dc-link pulse width, and thus the PWM capabilities are also restricted by the same reason. Reference [11] realized PWM by adopting single phase soft switching(SPSS) technique instead of controlling the link pulse width. It also showed significantly higher losses and device current stresses, and the PWM capability is highly restricted by the condition of the charge balance in the clamp capacitor.

Another approach for soft switched PWM inverter was suggested by using a parallel resonant dc-link(PRDCL), which also provided variable dc-link pulse width.[6,7] In appearance, removing the resonant inductor from the main conduction path and clamping the voltage stress of inverter part devices with V_s, might allow it to be applied for high power level. However, it also has several disadvantages such as many additional devices(4 devices) including a fast and a high voltage(2.0V_s) devices and restricted PWM capability due to the limitation of narrow pulse generation in the dc-link.

In this paper, a novel soft switching PWM converter by using a new parallel resonant dc-link(PRDCL) and by adopting single phase soft switching(SPSS) technique[10] is presented. The proposed PRDCL depicted in Fig. 1 suppresses the dc-link voltage to zero to allow zero voltage switching of inverter part devices without imposing excessive device voltage and current stresses. The device voltage stress of the PRDCL circuit itself is also limited by V_s Thus, all devices including inverter devices are under minimum voltage stress(V_s). The PRDCL provides not only variable link pulse width but also variable pulse position which is quite different feature comparing to the only variable link pulse width with fixed pulse position of the other resonant dc-links.[5,6-9] Thus, the PWM capability of the proposed PRDCL converter can be highly increased even though the minimum link pulse width is limited like that of the other RDCLs. For further enhancement of PWM capability of the PRDCL converter, the SPSS technique is employed, which can be achieved by distributing the resonant capacitor to each inverter device as shown in Fig. 2. Moderate combination of the PRDCL operation and SPSS operation enables the conventional PWM techniques to be applied. Furthermore the proposed converter can be extended to soft switching PWM rectifier-inverter without further excessive devices as shown in Fig. 3.

Operational principles, analyses, and design consideration are presented and a space vector PWM is realized and verified by simulations.

II. Operational Principles and Analyses

The proposed converter depicted in Fig. 2 achieves soft switching PWM with combined operations of PRDCL and SPSS. To simplify the illustrations of operations, the following assumptions are made:

(1) The resonant inductor L_r is much smaller than the load inductor L_o so that the load current can be treated as a constant current source during a switching period.

(2) All of the devices and components are ideal.

The following variables are defined:

(1) Resonant frequency, $\omega_r = 1/\sqrt{L_r C_r}$.

(2) Characteristic impedance, $Z_r = \sqrt{L_r/C_r}$.

A. PRDCL Operation

The proposed PRDCL circuit depicted in Fig 1 consists of three active devices, two diodes and LC resonant components. The resonant inductor is connected at the center of H-bridge instead of main conduction path[1-5,8-10] and forms a parallel resonant circuit with resonant capacitor. The operation of the PRDCL circuit can be illustrated using the simplified circuit shown in Fig. 4. During the switching period, the inverter with three phase load can be replaced by a constant current source I_o from the dc-link side.

The PRDCL operation can be divided into six operational modes and the mode diagrams for each mode and related waveforms are shown in Fig. 4 and 5, respectively.

Mode 0 (S_L: on, $S_a - S_b$: off): The switch S_L flows load current during a desired link pulse width T_o. The LC resonant circuit rests with the following conditions.

$$I_{L_r}(t) = 0 \tag{1}$$

$$V_{C_r}(t) = V_s. \tag{2}$$

Mode 1 (S_L: on, $S_a - S_b$: on): When the switching is needed, the switches S_a and S_b are turned on with zero current conditions so that the inductor current is initialized to the desired reference value I_i. Thus, the inductor current is linearly increased while the capacitor voltage is kept with V_s as follows:

$$I_{L_r}(t) = \frac{V_s}{L_r} t \tag{3}$$

$$V_{C_r}(t) = V_s. \tag{4}$$

The duration of this mode T_1 is obtained from the condition of $I_{L_r}(T_1) = I_i$.

$$T_1 = \frac{L_r I_i}{V_s}. \tag{5}$$

Mode 2 (S_L: off, $S_a - S_b$: on): The switch S_L is turned off with zero voltage condition and then, the LC resonant circuit starts to resonate with offset current I_o as follows:

$$I_{L_r} = \frac{V_s}{Z_r} \sin(\omega_r t) + (I_i + I_o)\cos(\omega_r t) - I_o \tag{6}$$

$$V_{C_r} = V_s \cos(\omega_r t) - (I_i + I_o)\sin(\omega_r t). \tag{7}$$

The capacitor voltage V_{C_r} is decreased resonantly until V_{C_r} becomes zero. Then, this mode is completed and the duration of this mode T_2 can be obtained from the condition of $V_{C_r}(T_2) = 0$ as

$$T_2 = \frac{1}{\omega_r} \tan^{-1}\left(\frac{V_s/Z_r}{I_i + I_o} \right). \tag{8}$$

The peak resonant inductor current I_p is also obtained by

$$I_p = I_{L_r}(T_2) = \sqrt{(I_i+I_o)^2+(\frac{V_s}{Z_r})^2} - I_o. \quad (9)$$

Mode 3 (S_L: off, $S_a - S_b$: on): The resonant capacitor voltage V_{C_r} is kept zero while the inductor current I_{L_r} freewheels through paths of $S_a - D_a$ and $S_a - D_b$.

$$I_{L_r}(t) = I_p \quad (10)$$

$$V_{C_r}(t) = 0. \quad (11)$$

This zero dc-link voltage period provides zero voltage switching condition to inverter devices. It is noted that the duration of this mode T_3 is controllable and thus, the link pulse position can be located at any position which is given by PWM controller. During this mode, the upper devices(S_1,S_3,S_5) or lower devices(S_4,S_6,S_2) of inverter would better be turned on for convenience in controller design. Then , the load current always freewheels through inverter itself. At the end of this mode, the inverter devices change the states to the next one with zero voltage condition and the load current defined by I_o is also changed to the next load current I_{ox} which is decided by the next states of the inverter devices.

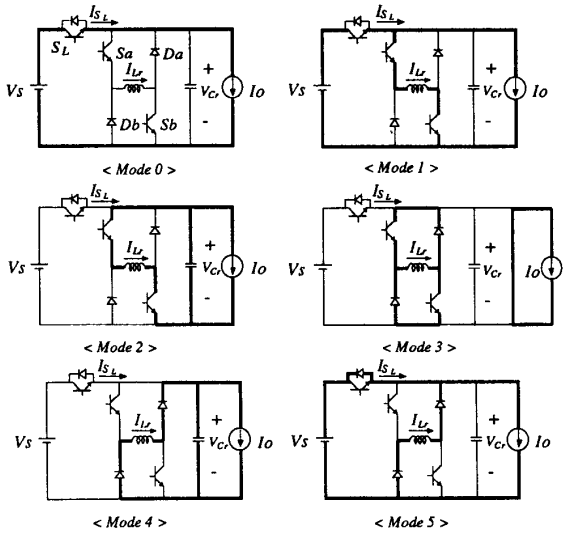

Fig. 4 Mode diagrams of the PRDCL operation.

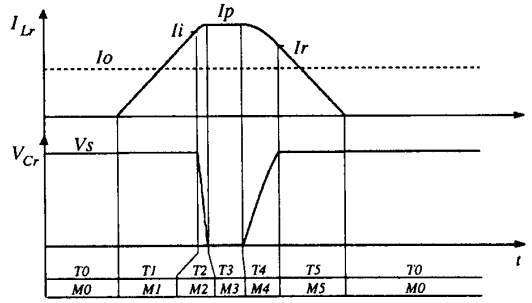

Fig. 5 Operational waveforms of the PRDCL circuit.

Mode 4 (S_L: off, $S_a - S_b$: off): When the switching of inverter devices is completed, the switches S_a and S_b are turned off with zero voltage condition to return the capacitor voltage V_{C_r} to V_s. Then, the flowing path of inductor current is switched into D_a, D_b and C_r and the capacitor voltage is built up by LC resonance until V_{C_r} reaches to V_s as follows:

$$I_{L_r} = (I_p - I_{ox})\cos(\omega_r t) + I_{ox} \quad (12)$$

$$V_{C_r} = Z_r(I_p - I_{ox})\sin(\omega_r t). \quad (13)$$

The duration of this mode T_4 is obtained from the condition of $V_{C_r}(T_4) = V_s$ as follows:

$$T_4 = \frac{1}{\omega_r}\sin^{-1}\left(\frac{V_s/Z_r}{I_p - I_{ox}}\right). \quad (14)$$

The remained energy in inductor(I_p) is also obtained as follows:

$$I_r = I_{L_r}(T_4) = \sqrt{(I_p - I_{ox})^2 - (\frac{V_s}{Z_r})^2} + I_{ox}. \quad (15)$$

Mode 5 (S_L: on, $S_a - S_b$: off): When the capacitor voltage V_{C_r} is increased slightly over V_s, the antiparallel diode connected in S_L is turned on with zero voltage condition. Then, the capacitor voltage V_{C_r} is clamped by source voltage V_s and the remained energy in the resonant inductor is returned to voltage source. The inductor current is linearly decreased from I_r to zero and the diodes D_a and D_b are turned off with zero current conditions.

$$I_{L_r}(t) = -\frac{V_s}{L_r}t + I_r \quad (16)$$

$$V_{C_r}(t) = V_s. \quad (17)$$

Duration of this mode T_5 depends only on the remained inductor current I_r and obtained as follows:

$$T_5 = \frac{L_r I_r}{V_s}. \quad (18)$$

One switching cycle of the PRDCL is completed at the end of this mode. The operational waveforms are shown in Fig. 5.

B. SPSS operation

The SPSS which was used for the realization of PWM in ACRDCL inverter[10], is adopted to enhance the PWM capability of the proposed PRDCL converter. As shown in Fig. 2, the resonant capacitor is distributed to the individual devices in the inverter side. The capacitor C_r' connected with individual devices is chosen as $C_r' = 1.5C_r$ so that the equivalent resonant capacitance becomes still C_r. Then, the PRDCL operation can be achieved in the same manner as the circuit shown in Fig. 1.

The operation of SPSS was already presented in reference [10]. However, it is briefly reviewed in this section to investigate the effect of SPSS on the PRDCL operation and characterize the overall operation. To simplify the illustration, the phase current is still assumed to a constant current source I_a. The mode diagrams and waveforms are shown in Fig. 6(a) and (b), respectively. Assuming that the active device S_1 is conducting as shown in Fig. 6(a), the S_1 can be turned off in a-phase itself with soft switching manner. When the S_1 is turned off, the phase voltage V_a is linearly decreased from V_s to zero as follows:

$$V_a(t) = -\frac{I_a}{C_r}t + V_s. \quad (19)$$

Then, the diode D_4 starts to conduct as shown in Fig. 6(b). It should be noted that it is possible to achieve the SPSS operation only when the active device is conducting and the *dv/dt* ratio of

phase voltage is governed only by the magnitude of phase current.

To investigate the effect of SPSS on the PRDCL operation, the situation that three active devices are conducting as shown in Fig. 7(a) is considered. The current in the switch S_L is decreased stepwise at every SPSS operation as shown in Fig. 7(b). In the PWM-ACRDCL inverter[10], this phenomenon deteriorates the overall converter efficiency and restricts PWM capability. In this case, the SPSS operation, however, increases the PWM capability of PRDCL and reduces the peak current stress of S_L which is generated by the Mode 1 operation of PRDCL circuit as shown in Fig. 7(b).

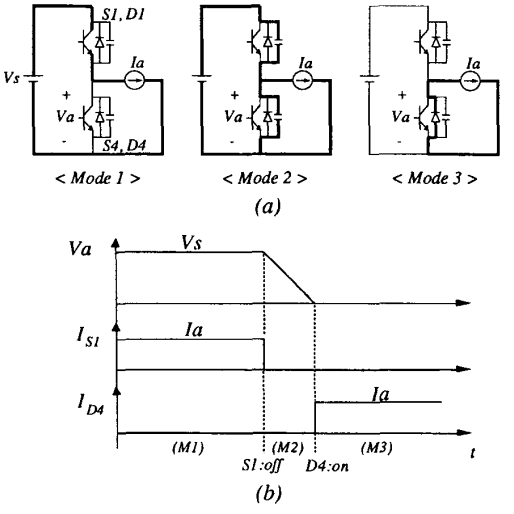

Fig. 6 Illustration of the SPSS operation.

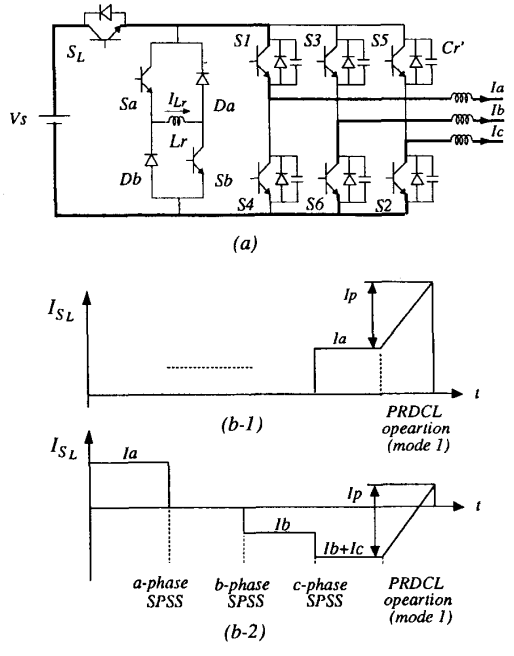

Fig. 7 Effect of SPSS on the PRDCL operation (comparison of the peak current stress of S_L): (a) switch states before the SPSS operations, (b-1) I_{S_L} for the case of PRDCL operation only, (b-2) I_{S_L} for the case of combined operation.

III. Design Consideration

For the repetition of safe PRDCL operation, the stored energy in the resonant inductor(I_p) must be large enough to return the capacitor voltage V_{C_r} back to V_s. Therefore, it is important to monitor and control of I_p to ensure the zero voltage switching of S_L. The condition of I_p for safe operation can be obtained from eq. (15)

$$I_p \geq \frac{V_s}{Z_r} + I_{ox} \tag{20}$$

where, the next load current I_{ox} can be predicted from the next switching patterns[4] as

$$I_{ox} = S_1 \cdot I_a + S_3 \cdot I_b + S_5 \cdot I_c . \tag{21}$$

To store the desired energy in the resonant inductor, the initialization of the inductor current in Mode 1 should be moderately done. From eq.(9) and (20), the required initializing current I_i in Mode 1 can be calculated as follows:

$$I_i \geq \sqrt{(\frac{V_s}{Z_r}+I_o+I_{ox})^2 - (\frac{V_s}{Z_r})^2} - I_o . \tag{22}$$

Fig. 8 shows this relation graphically. It is noted that the the conduction losses in the devices and components can be minimized by optimal initialization of I_i.

The minimum pulse width of PRDCL is restricted like that of the other RDCLs. Assuming that the initializing current I_i is optimally controlled, the minimum link pulse width *Twmin* in worst case can be obtained from eq.(5) and (18) as

$$T_{wmin} = \frac{2L_r}{V_s}\sqrt{I_{omax}(\frac{V_s}{Z_r}+I_{omax})} \tag{23}$$

where the I_{omax} represents the maximum load current. The PWM control strategy should be designed with consideration of T_{wmin}.

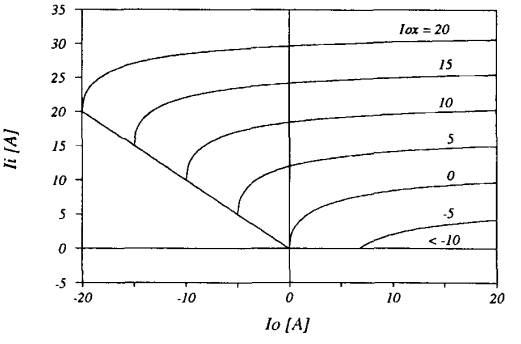

Fig. 8 Required initializing resonant inductor current(I_i) according to the present(I_o) and next(I_{ox}) load currents.

IV. Realization of Space Vector PWM

Due to high PWM capability of the proposed converter, several conventional PWM techniques can be applied. A simple and well known space vector PWM technique[15] is realized to test the true PWM capability.

The voltage vectors are shown in Fig. 9. The reference performance vector U^* rotates in the count-clockwise direction with an angular speed ω and the real performance vector U follows U^* locus by moderate selection of voltage vectors, $V_n(n=0,1,2,\cdots,6)$ and adjustment of its width in every sampling period T_s. Fig. 10(a) shows a sampling period that the U^*-locus is followed by the combination of three voltage vectors(V_0,V_1,V_2). The time durations of selected voltage vector represented by T_0, T_1 and T_2, respectively, can be calculated by various method keeping the relation of

$$T_s=T_0+T_1+T_2. \tag{24}$$

The realization of the space vector PWM is done by the following rules:

(1) The dc-link pulse width is controlled by the amount of duration(T_1+T_2).

(2) The dc-link short period is used for zero vector(V_0,V_7).

(3) The SPSS operation is used for switching of the nonzero vectors(eg. $V_1 \rightarrow V_2$).

Fig. 10(b) shows the phase voltages and line voltages governed by the above rules. It is seen that the voltage waveforms are the same as those of the hard switched PWM inverter[15] except smoothed transition of voltage waveforms. Fig. 11 shows the selection sequence of nonzero vectors to ensure safe SPSS operation. The selection sequence depends on the polarity of phase current as shown in Fig. 11(a) and (b).

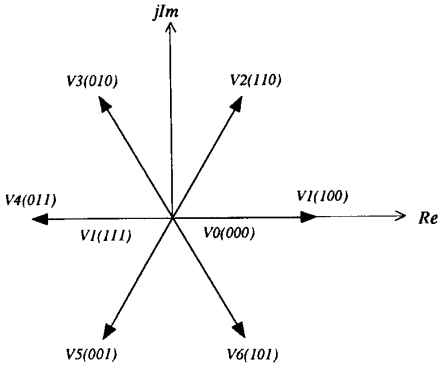

Fig. 9 Representation of voltage vectors.

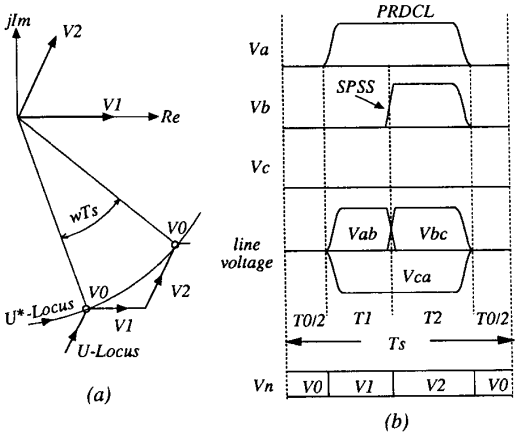

Fig. 10 Realization of the space vector PWM in the proposed converter: (a) Loci of U and U*, (b) relation among switching vectors and voltages for one sampling period.

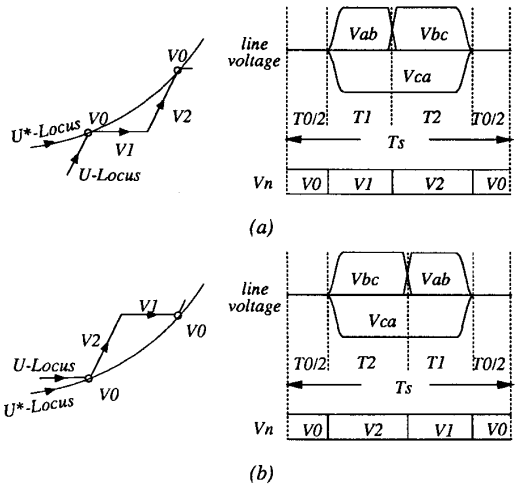

Fig. 11 Selection sequence of nonzero vectors enabling SPSS operation: (a) I_b: negative, (b) I_b: positive.

It should be noted that the lower bound of time duration T_1+T_2 which is proportional to modulation index, is limited by T_{wmin} because the narrow link pulse width is limited by T_{wmin}. In consequence, the modulation index has a lower bound. To alleviate this problem, the resonant frequency ω_r should be increased or the switching frequency should be reduced. A simple method is under investigation to overcome such a problem and will be presented latter in another issue.

V. Simulation Results

In order to verify the operational principles and true PWM capability, the proposed PRDCL inverter is simulated under 10 hp induction motor load and 20 KHz switching frequency. The circuit parameters used in the simulation are given as follows:

$$L_r = 60uH,$$
$$C_r = 0.1uF,$$
$$V_s = 300V.$$

Fig. 12 shows the simulated microscopic waveforms including dc-link voltage(V_{C_r}), phase voltages(V_a, V_b, V_c), line-to-line voltage(V_{ab}), resonant inductor current(I_{L_r}), load current(I_o) and switch current(I_{S_L}). All of the waveforms are fairly well matched comparing to the predicted ones. It can be seen that the PRDCL operation is performed with capability of variable link pulse position as well as variable link pulse width. The link pulse width is varied according to the sum of time durations of two nonzero vectors keeping the constant link pulse period($50\,us$). The SPSS operation occurs when the change of a nonzero vector to another nonzero vector is needed(eg. $V_1 \rightarrow V_2$). The line-to-line voltage V_{ab} shows the true PWM waveforms with satisfication of PPCR(pulse polarity consistency rule). The peak resonant inductor current is varied due to the optimal initialization of inductor current, which is obtained by the relation of the load current and

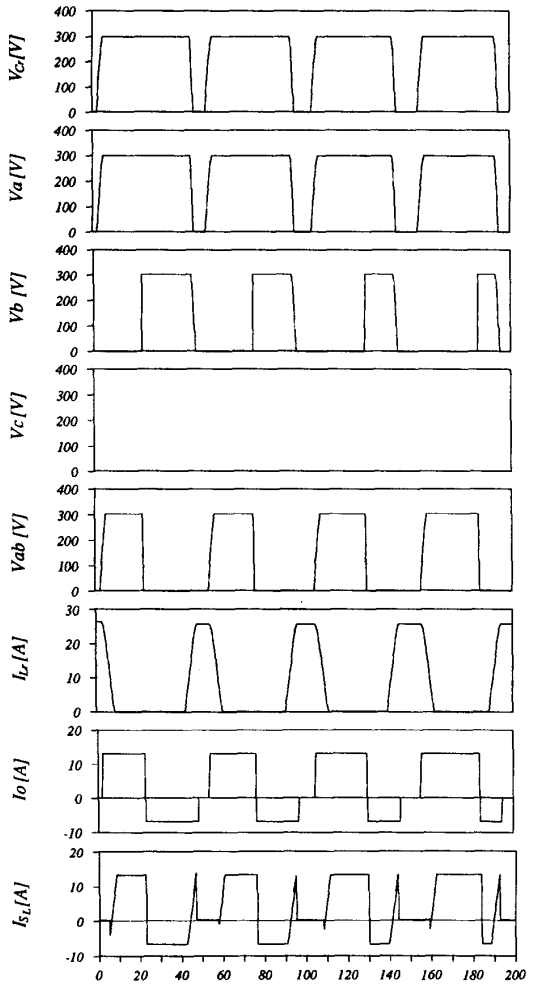

Fig. 12 Simulated microscopic waveforms of the proposed converter.

the next state load current. The current waveform of the switch I_{S_L} is changed stepwise by SPSS operation and linearly by initialization of the inductor current. The minimum link pulse width T_{wmin} in worst case is calculated as $10\,us$ for $50\,us$ switching period. Thus, the modulation index has operating range of about 20-100 %. Fig. 13 shows macroscopic waveforms of line-to-line voltage and the phase current governed by the space vector PWM. The line-to-line voltage shows that the true PWM is performed and the PPCR is completely satisfied. Accordingly, the phase current shows sinusoidal waveforms with very low ripple, near sine wave. Fig. 14 shows frequency spectra of the line-to-line voltage and it can be seen that the lower order harmonics are nearly eliminated without any subharmonic contents.

VI. Conclusion

A novel soft switching PWM converter is presented by using a new PRDCL and adopting the SPSS technique. Operational principles, analyses, and some characteristics are also illustrated and a space vector PWM technique is realized to test the true PWM capability of the proposed converter. The simulation results at 20 KHz switching frequency verified the operations and the validity of

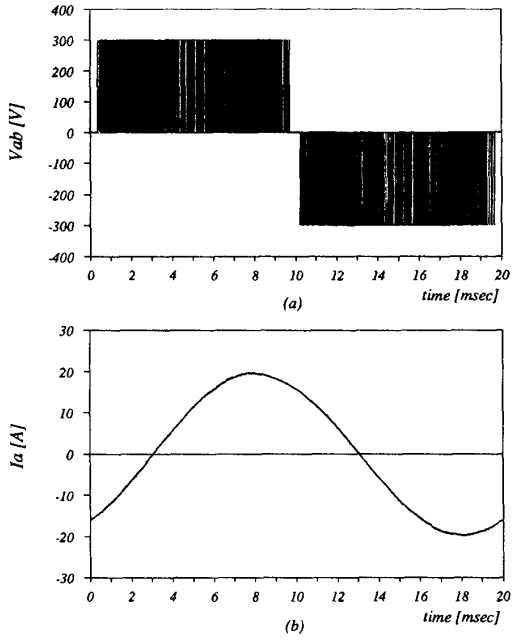

Fig. 13 Simulated macroscopic waveforms of the proposed converter with realization of space vector PWM: (a) line-to-line voltage(V_{ab}), (b) phase current(I_a).

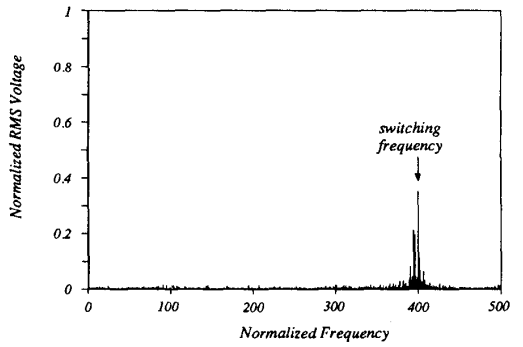

Fig. 14 Frequency spectra of the line-to-line voltage (fundamental frequency: 50 Hz).

PWM capability. The proposed converter is thought to be applied to a wide power range(20-200 KW) due to distinctive advantages over the PWM-RDCL converters including true PWM capability, minimum device voltage stress(all V_s) and low device current stress. Furthermore it can be extended to soft switching PWM rectifier-inverter without excessive devices and components.

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