Novel Snubberless Three-Level GTO Inverter with Dual Quasi-Resonant DC-link

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Abstract

Novel 3-level GTO inverter topology is presented. This new power circuit includes many advantages comparing with the conventional 3-level GTO inverter. The main advantages are snubberless and good device utilization by employing dual quasi-resonant dc-link which guarantees the complete zero voltage switching of the inverter GTO's. This 3-level GTO inverter can be operated with lower switching loss at higher switching frequency with complete zero voltage inverter switching.

I. Introduction

Three-level GTO topology is suitable for high voltage and high power applications because the device voltage stresses can be divided into one half of the dc-link voltage. GTO inverter requires snubber circuits to protect from the excessive dv/dt problem when the GTO is switched off. The stored energy in the snubber can not be neglected and additional snubber power recovery converters are usually required.

The conventional 3-level GTO inverter is illustrated in Fig. 1. This inverter topology has some serious disadvantages inherently. The voltage of the snubber capacitor, Cs, is clamped above the dc source voltage, Vs+VT, which increases the voltage stresses of GTO and diode. Another disadvantage is that the mid-GTO's have higher dv/dt stress problem since these GTO's are protected by the upper or lower snubber capacitors which have long current paths having large stray inductances. This effect increases the turn-off voltage spike of the GTO which is one of the most serious factors for the GTO failure during turn-off. To solve this problem, the inverter mechanical structure design should be very cautious and the snubber capacitors with larger capacitance is

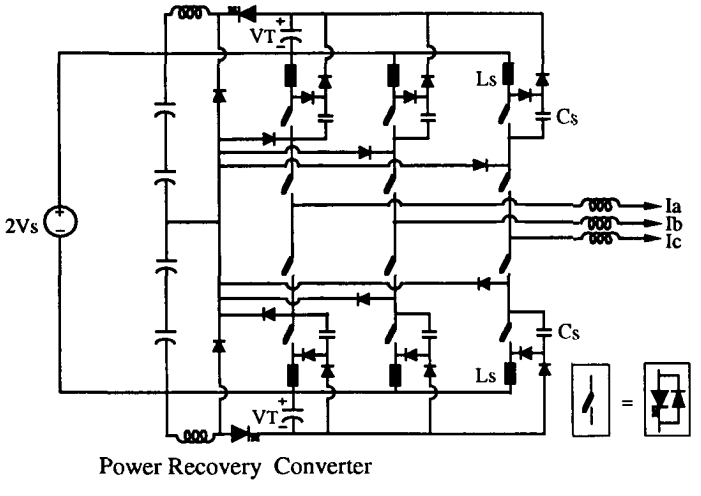

Fig. 1 Conventional 3-level GTO inverter with snubber enegy recovery

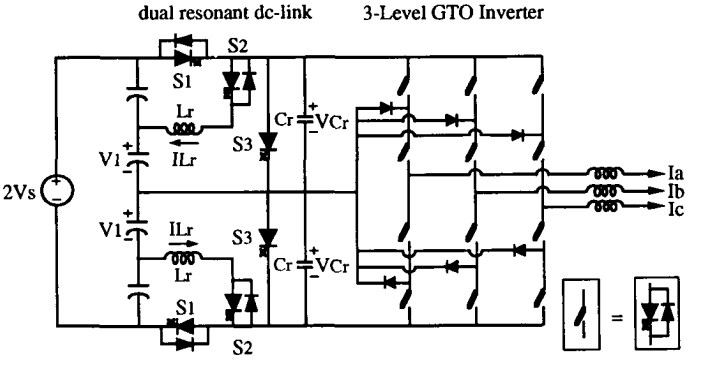

Fig. 2 Snubberless 3-level GTO inverter with dual resonant dc-link

required. Sometimes additional lossy snubber and bypass capacitor is needed [6]. It is clear that this phenomena will decrease the device reliability or the switching frequency.

The resonant dc-link is actively studied to reduce the device switching loss, however, the GTO inverter employing resonant dc-link is rare even the 2-level one [2, 3]. Snubber circuits have been mainly considered for the GTO applications taking into account that the voltage stress should be limited as low as possible close to 1 p.u. because in the high power application the device voltage margin is not enough. Some resonant dc-link inverters satisfy this requirement, however, the dv/dt problem for the GTO controlling the dc-link is another problem [10].

The quasi resonant dc-link [1] presented recently can predict the resonant interval of the dc-link in spite of the variable load current when the dc-link GTO is turned off. This can solve the aformentioned problem though it requires complex dc-link control. In this paper a dual resonant dc-link 3-level GTO inverter is proposed as illustrated in Fig. 2. This proposed inverter has several advantages comparing with the conventional one. First, the voltage stress is suppressed to 1.0 p.u.. The second, since the dominant loss of GTO occurs during switching interval, the complete zero voltage switching of the inverter side GTO's provides the lowest power stresses which could raise the device utilization factors to increase the repetitive current or switching frequency [3-5]. As a result, the reliability of the GTO is also increased and the number of snubber capacitors are reduced into two with removal of the power recovery converter. Considering that the cost of each snubber capacitor and snubber diode is comparable to the GTO and regenerative power converters are a big portion, the system complexity and the total cost of the proposed GTO inverter will not be increased in spite of the additional dc-link compared with the conventional 3-level one. If higher device utilization of the inverter side GTO's is abandoned by sacrificing some ZVS property, two of the GTO's, S3, could be detached maintaining the similar performance with the conventional 3-level topology, resulting in more cost effective structure.

II. Operations of Dual Resonant DC-link

The operation of the dual quasi-resonant dc-link is presented as follows. As the upper side dc-link and the lower side dc-link operation is identical, only one-side dc-link operation is presented. The mode diagrams and the dc-link waveforms are illustrated in Fig. 3 and Fig. 4, respectively.

Operation modes are divided into six which are composed of normal mode(mode 0), inductor current built-up mode(mode 1), pre-resonant mode(mode 2), inductor current re-build mode(mode 3), post-resonant mode(mode 4) and recovery mode(mode 5). The detailed dc-link operations are described as follows:

1) Mode 0 (S1: on, S2: off, S3 : off)

This mode is normal operation mode in which the load current Io is flowing through S1.

2) Mode 1 (S1 : on, S2 : on, S3 : off)

To switch the upper side GTO between the mid GTO's, the voltage of upper dc-link should be zero. This dc-link operation needs initial inductor current. When the switch S2 is turned on with zero current switching condition, the resonant inductor current ILr is increased linearly to the desired value of Ib1:

$$I_{Lr}(t) = \frac{(V_s - V_1)}{L_r} t ,$$

$$V_{Cr}(t) = V_s .$$

3) Mode 2 (S1 : off, S2 : on, S3 : off)

When the switch S1 is turned off with zero voltage condition, the Lr and Cr resonate with offset current Ib1 and the load current Io. At this time, the dv/dt of the switch S1 depends on the resonant interval which is the function of Io and Ib1:

$$I_{Lr}(t) = \frac{(V_s - V_1)}{Z_r} \sin(\omega t) + (I_{b1} + I_o)\cos(\omega t) - I_o ,$$

$$V_{Cr}(t) = (V_s - V_1)\cos(\omega t) - Z_r (I_{b1} + I_o)\sin(\omega t) + V_1 ,$$

$$\text{where } \omega = \frac{1}{\sqrt{L_r C_r}} \text{ and } Z_r = \sqrt{\frac{L_r}{C_r}} .$$

4) Mode 3 (S1 : off, S2 : on -> off, S3 : on)

When the resonant capacitor voltage VCr reaches zero, the inductor current is decreased linearly through the neutral voltage clamping diode and freewheeling diode. From this operation the S3 and inverter side GTO's can be switched off with complete zero voltage condition. When the inductor current direction is reversed, the current increases

with reverse direction continuously through S3, and then S2 is turned off with zero voltage and zero current condition:

$$I_{Lr}(t) = I_{r1} - \frac{V_1}{L_r} t ,$$
$$V_{Cr}(t) = 0.$$

5) Mode 4 (S1 : off, S2 : off, S3 : off)

To return the capacitor energy to the source voltage Vs, the switch S3 is turned off with zero voltage condition. When S3 is turned off, the inductor and the capacitor resonate with the initial inductor current Ib2 plus the new load current Iox.

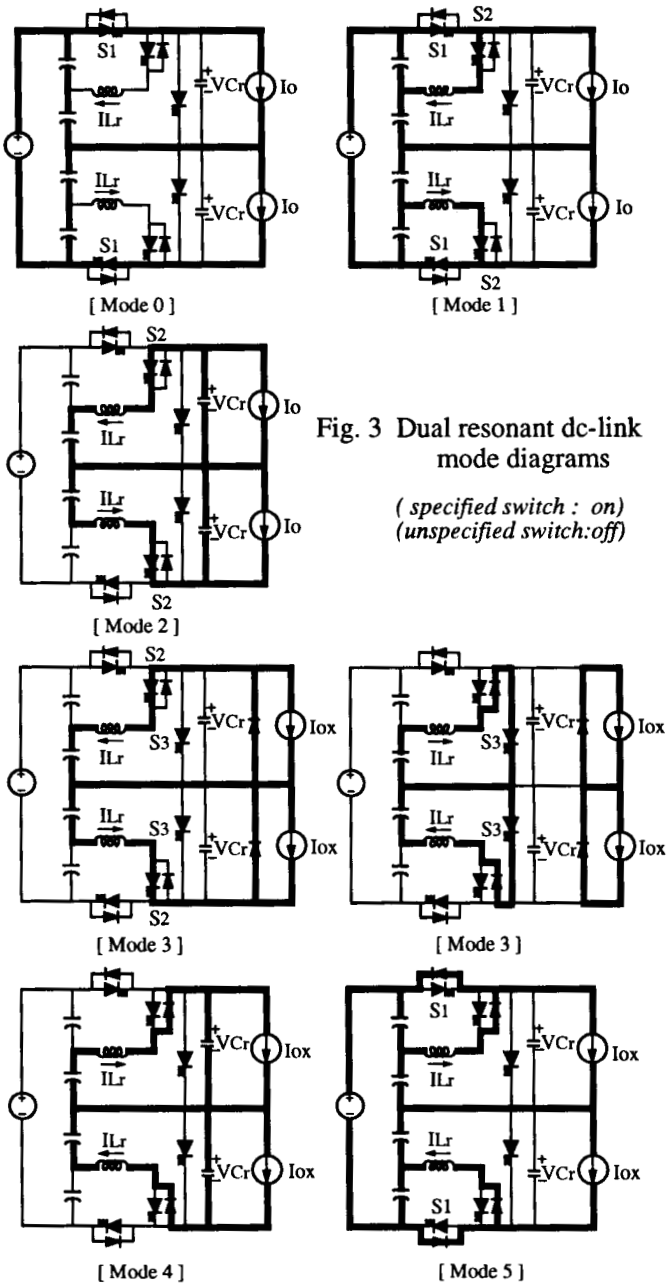

Fig. 3 Dual resonant dc-link mode diagrams

(specified switch : on)
(unspecified switch:off)

This resonant interval will guarantee the dv/dt of GTO S3:

$$I_{Lr}(t) = -\frac{V_1}{Z_r} \sin(\omega t) + (I_{b2} + I_{ox}) \cos(\omega t) - I_{ox} ,$$

$$V_{Cr}(t) = -V_1 \cos(\omega t) - Z_r (I_{b2} + I_{ox}) \sin(\omega t) + V_1 .$$

6) Mode 5 (S1 : off -> on, S2 : off, S3 : off)

When the resonant capacitor voltage VCr exceeds the source voltage Vs, the resonant period is ended and the VCr is clamped to the Vs. The remaining energy in the inductor is returned to the source Vs. In this mode the switch S1 is turned on with zero voltage condition:

$$I_{Lr}(t) = \frac{(V_s - V_1)}{L_r} t - I_{r2} ,$$
$$V_{Cr}(t) = V_s.$$

III. Dual Resonant DC-link Control

The dual resonant dc-link control is the most important part to operate this power circuit. For the robust dc-link operation, the resonant intervals of mode 2 and mode 4 should be longer than a certain time which is enough to limit the dv/dt of the dc-link GTO S1 and S3. The resonant interval T2 and T4, however, is a function of the built-in current of the resonant inductor and the present state load current Io or the next state load current Iox, respectively. The

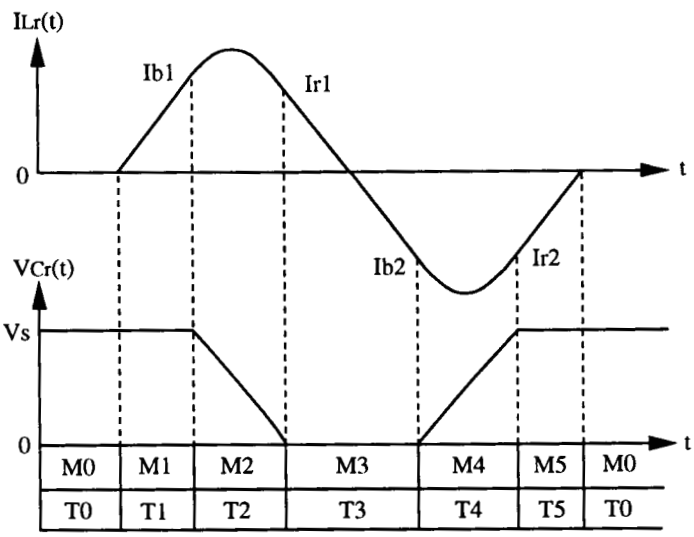

Fig. 4 Dual resonant dc-link waveforms

resonant inductor current build-up is adjusted so that the pre- and post-resonant intervals keep a certain time. The inductor currents Ib1 and Ib2 to maintain required resonant intervals for safe operation of S1 and S3 just before the resonant operation are derived from the mode equations as

$$Ib1 = \frac{(Vs - V1)\cos(\omega T2) + V1}{Zr \sin(\omega T2)} - Io ,$$

$$Ib2 = \frac{- V1 \cos(\omega T4) - (Vs - V1)}{Zr \sin(\omega T4)} - Iox .$$

where T2 and T4 are the pre- and post-resonant intervals, respectively, and Io and Iox are measured values.

For robust dc-link operation, the build-up currents in the inductors have to be larger than the minimum values which are given the difference between the resonant current and the load current as

$$Ib1 > (Vs - V1) / Zr - Io$$

and $$Ib2 > (Vs - V1) / Zr - Iox .$$

The two capacitor voltage balance at the dc-link side is considered satisfying the above conditions. Practically there exists no problem for balance because the capacitor is large enough to be regulated within a boundary during the dc-link interval. In other words, if T2 and T4 are selected with some marginal values, the adjustment of the mode intervals can be used to regulate the capacitor voltage within a bounded voltage deviation.

As mentioned above, the dual resonant dc-link have to be controlled in real time by measuring the load currents and the source-side capacitor voltages and the dc-link control sequences should also be changed for each dc-link. The capacitor charge balance control is another factor varying the dc-link sequence.

IV. Experiments

The experiments are performed with the GFF90B60 GTO, 50 uH resonant inductor and 1uF resonant capacitor with 300V dc voltage source. The power circuit is controlled by ADSP-21020 DSP with 32kwords program and data memories.

As predicted, the initial voltage spike from the GTO turn off appears in the measured waveform of dc-link operation which is captured in Fig. 5. The upper side dc-link operations are shown in Fig. 6

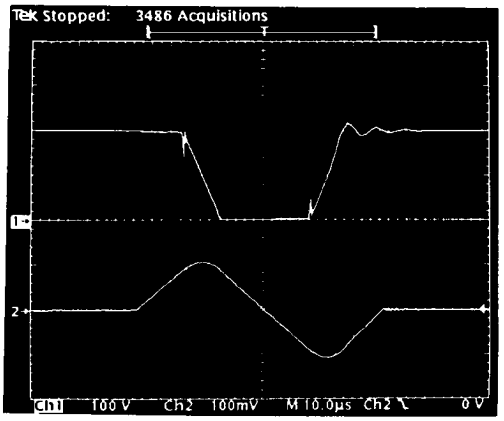

Fig. 5 Waveforms of upper side dc-link operation
Ch1: dc-link voltage
Ch2: resonant inductor current (20 A/div)

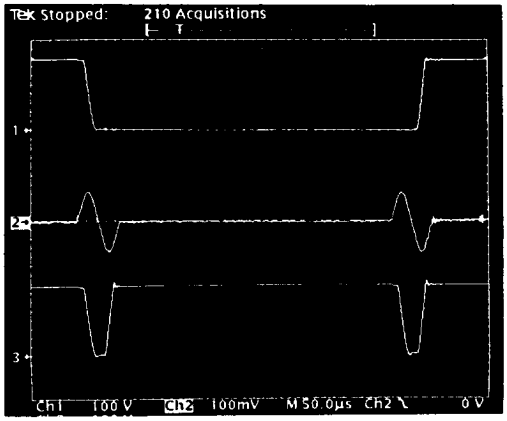

Fig. 6 DC-link operations with pole voltage
Ch1: pole voltage
Ch2: resonant inductor current (20 A/div)
Ch3: dc-link voltage

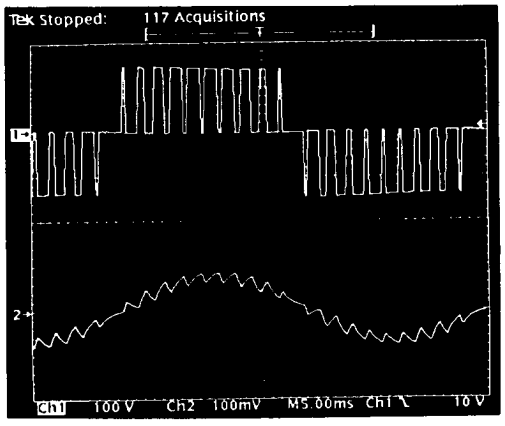

Fig. 7 Pole voltage and line current
Ch1: pole voltage
Ch2: line current (20A/div)

including the pole voltage, the resonant inductor current and the dc-link voltage. One period of pole voltage and load current is shown in Fig. 7 for the operating frequency of 50Hz at the modulation index of 0.8 with the dc-link switching frequency of somewhat above 1kHz.

V. Conclusion

Novel snubberless 3-level GTO inverter has been explored and presented. This new topology is applicable for high power GTO inverter or higher switching frequency operation with the same GTO of the conventional 3-level inverter. The dual quasi-resonant dc-link results in the complete zero voltage switching of the inverter GTO's eliminating the snubbers for each device. Since the snubber capacitors are omitted, the cost of the dc-links become lower than the conventional one . The DSP is adopted to control the dual resonant dc-link which require real-time measuring the load current and the capacitor voltage.

This snubberless 3-level GTO inverter operates with lower switching losses. It is verified that this topology is possible for higher switching frequency with robust inverter switching having higher device utilization and the reduced mechanical structure design effort.

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