AIP Applied Physics Letters

Determination of the density of states at the Fermi level of hydrogenated amorphous silicon in thinfilm transistor structure by space charge limited current measurement

Hoe Sup Soh, Choochon Lee, Jin Jang, Moon Youn Jung, and Soon Sung Yoo

Citation: Appl. Phys. Lett. **63**, 779 (1993); doi: 10.1063/1.109905
View online: http://dx.doi.org/10.1063/1.109905
View Table of Contents: http://apl.aip.org/resource/1/APPLAB/v63/i6
Published by the American Institute of Physics.

Additional information on Appl. Phys. Lett.

Journal Homepage: http://apl.aip.org/
Journal Information: http://apl.aip.org/about/about_the_journal
Top downloads: http://apl.aip.org/features/most_downloaded
Information for Authors: http://apl.aip.org/authors

ADVERTISEMENT

Downloaded 16 Apr 2013 to 143.248.118.122. This article is copyrighted as indicated in the abstract. Reuse of AIP content is subject to the terms at: http://apl.aip.org/about/rights_and_permissions

Determination of the density of states at the Fermi level of hydrogenated amorphous silicon in thin-film transistor structure by space charge limited current measurement

Hoe Sup Soh and Choochon Lee
Department of Physics, Korea Advanced Institute of Science and Technology, Yusung-ku, Daejeon 305-701, Korea

Jin Jang, Moon Youn Jung, and Soon Sung Yoo
Department of Physics, Kyung Hee University, Dongdaemoon-ku, Seoul 130-701, Korea

(Received 14 September 1992; accepted for publication 26 May 1993)

We studied the space charge limited current effect in hydrogenated amorphous silicon (*a*-Si:H) thin-film transistors (TFTs). We demonstrate that the drain current is space charge limited when the source-drain voltage is large and the gate voltage is small. Using this space charge limited current we determined the density of states in the gap of *a*-Si:H in *a*-Si:H TFT.

There is a considerable interest in the application of hydrogenated amorphous silicon (*a*-Si:H) film to the fabrications of thin-film transistors (TFTs) for use in active matrix liquid crystal displays (LCDs).[1–5] The *a*-Si:H TFT requires the deposition of at least three layers: *a*-Si:H, gate insulator, and heavily doped (n^+) *a*-Si:H. A full characterization of all these layers in the TFT structure is needed to improve the performance of *a*-Si:H TFTs. The quality of the gate insulator can be tested by the measurement of leakage current through the source (or drain) and gate electrodes, and the quality of the ohmic contact layer can be assessed from the output characteristics of the TFT at low drain voltages. For example, high contact resistance gives rise to the current crowding in the output. However, the quality of *a*-Si:H in the TFT structure is not easy to determine because both the interface between *a*-Si:H and the gate insulator, and bulk *a*-Si:H contribute to the performance of *a*-Si:H TFTs.

In *a*-SiH n^+-i-n^+ sandwich structure, where the n^+ layer is used to inject carriers into the intrinsic (i) layer, space charge limited currents are typically observed and used to determine the density of states in the gap.[6–8] The current voltage characteristics are ohmic at low applied voltage, followed by the space charge limited current which rapidly increases with voltage. The voltage at which the space charge limited current starts to appear depends on both the electric field applied across the i layer and the quality of *a*-Si:H.

On the other hand, an n^+-i-n^+ lateral structure is used in an *a*-Si:H TFT. The drain current in n^+-i-n^+ *a*-Si:H TFT, might therefore also be space charge limited. In this work, we have studied the space charge limited current in *a*-Si:H TFTs.

We used remote plasma chemical vapor deposition (RPCVD) to deposit our *a*-Si:H and silicon nitride (gate insulator) films. The cylindrical quartz tube of a diameter of 3.8 cm is connected on the upside of a remote deposition chamber. 20% silane in hydrogen is introduced into the downstream reactor and the helium passes through the quartz tube. The rf power is applied through the coil which is wrapped around the outside of the quartz tube. Some of the helium atoms fed are excited into a metastable state or ionized by passing through the plasma-generating region.[9,10]

We fabricated inverse-staggered type *a*-Si:H TFTs. The device fabrication starts by depositing 1000 Å thick Cr on a Corning 7059 glass plate. After gate patterning, the silicon-nitride (SiN) gate insulator was deposited at 350 °C with a rf power of 15 W. The flow rates of He, NH_3, and SiH_4 were 63, 5, and 0.5 sccm, respectively. The substrate temperature was lowered to 250 °C for the deposition of undoped *a*-Si:H and n^+ microcrystalline (μC)-Si layers. To make the μC-Si film, a hydrogen silane mixture of $H_2/SiH_4=50$ was used, resulting in the electrical conductivity of 30 S/cm for the 400 Å thick film. The thicknesses of the SiN, *a*-Si:H, and μC-Si layers were 3000, 2000, and 400 Å, respectively. After patterning of the source/drain electrodes, the n^+ layer between the source and drain electrodes was removed by plasma etching using CF_4. All measurements reported in this letter were performed using structures with a channel length of 12 μm and width of 60 μm.

Figure 1 shows the *a*-Si:H TFT output characteristics for various low gate voltages. The drain current increases rapidly above 15 V of drain voltage (V_d) and the currents for the different gate voltages merge at high drain currents, as shown in the right-hand side of Fig. 1. The current is independent of the source/drain polarity because of the symmetric n^+-i-n^+ structure. The drain currents at three different gate voltages (0.5, 0.6, and 0.7 V) merge at drain voltages above 30 V, since the space charge limited current is dominant compared with the current caused by electron accumulation layer. From Fig. 1, it is clear that the rapid increase in drain current at high drain voltage (around 30 V in this experiment) is caused by the space charge limited current flow.

Figure 2 shows the drain current-voltage characteristics of *a*-Si:H TFT measured at gate voltages of 0, −2, and −2.5 V. Generally, the current-voltage curve for zero gate voltage does not show ohmic behavior because interface charges cause an electron accumulation layer near the SiN/*a*-Si:H interface. Flat band conditions can be achieved

 © 1993 American Institute of Physics

Downloaded 16 Apr 2013 to 143.248.118.122. This article is copyrighted as indicated in the abstract. Reuse of AIP content is subject to the terms at: http://apl.aip.org/about/rights_and_permissions

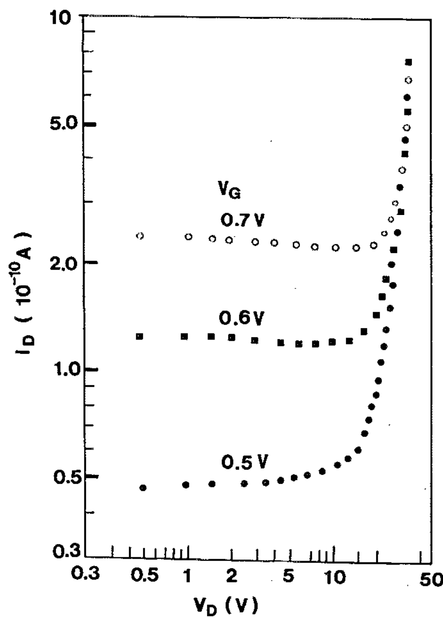

FIG. 1. The drain current as a function of drain voltage for subthreshold gate voltages in a-Si:H thin-film transistors. The increasing part of the drain current at the right-hand side is due to the space charge limited current.

by applying a negative gate potential. Figure 2 shows that the current is proportional to a drain voltage at a gate voltage (V_G) of -2.5 V. In general, for the a-Si:H TFTs made by RPCVD, this linear current-voltage curve at low drain voltages can be achieved for a gate voltage between 0 and -3 V, depending on the preparation conditions. We can see a slope of 1 below 7 V for $V_G=-2.5$ V, and a rapid increase in current above 10 V. This increasing current is dominated by space charge limited current and independent of gate voltage for $V_G=-2.0$ to -2.5 V.

Another interesting point from Fig. 2 is that the flat band voltage of this TFT is -2.5 V. To obtain the density of states in the gap of a-Si:H from field effect experiments, it is necessary to know the flat band voltage.[11] This can be

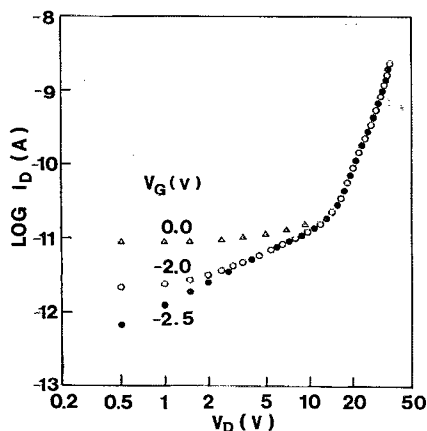

FIG. 2. The drain current vs voltage curves for various negative gate voltages. The curve for $V_G=-2.5$ V was used to calculate the density of states in the gap of a-Si:H.

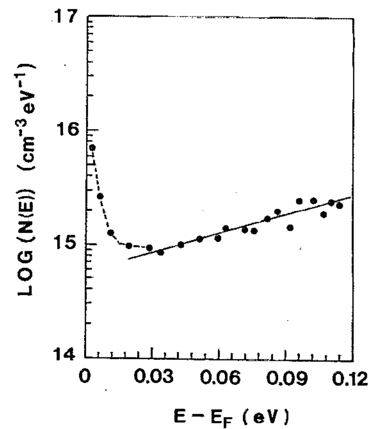

FIG. 3. The density of states in the gap of a-Si:H calculated from the space charge limited current in a-Si:H TFT by a step by step method.

done by varying the gate voltage until a linear drain current voltage relationship at low drain voltages is achieved.

From the space charge limited current in the symmetric n^+-i-n^+ structure, the density of states in the gap can be obtained. Several assumptions are needed to obtain the quasi-Fermi level and the density of states at the quasi-Fermi level; (i) the sample is homogeneous, (ii) only electrons are injected from the n^+ electrode, (iii) diffusion current is neglected, and (iv) the injected charge from the contact is, at all times, in equilibrium with the population of deep states.

The density of states in the gap, $N(E)$, and the shift of the quasi-Fermi level, ΔE_F, is obtained from the assumptions of constant electric field and uniform charge density:[12]

$$\Delta E_F = kT\,Ln(j_2V_1/j_1V_2) \quad (1)$$

$$N(E) = 2\epsilon_s(V_2-V_1)/eL^2\Delta E_F. \quad (2)$$

Here, (V_1, j_1) and (V_2, j_2) indicate the voltage and corresponding current on a voltage current curve, L is the separation between the source and drain electrodes, e the electronic charge, and ϵ_s the electric permittivity of a-Si:H.

Figure 3 shows the density of states in the gap of a-Si:H calculated from the space charge limited current behavior shown for $V_G=-2.5$ V in Fig. 2. To obtain the density of states we have to select two pairs of (j_1, V_1) and (j_2, V_2). There is a large uncertainty in the density of states calculated from the "knee" region around $V_d\sim 20$ V in Fig. 2 since a small experimental error for the pair of current-voltage values can give rise to a large error in $N(E)$ because the ΔE_F is very small (less than meV). Therefore, we show the corresponding $N(E)$ data as a dotted line. A similar decreasing trend in $N(E)$ with $E-E_F$, as obtained from the space charge limited current measurement can be found in the data by Weisfield.[13] The $N(E)$ obtained for $V_d>20$ V data in Fig. 2 shows an exponential dependence on energy, as indicated by the solid straight line in Fig. 3. The characteristic temperature (T_0), defined from $N(E)$ being proportional to $\exp(E/kT_0)$, is 950 K. This temperature can also be obtained from the analytic formula developed by Rose:[14]

Downloaded 16 Apr 2013 to 143.248.118.122. This article is copyrighted as indicated in the abstract. Reuse of AIP content is subject to the terms at: http://apl.aip.org/about/rights_and_permissions

$$I = C.V^{[T_0/T+1]}. \quad (3)$$

Here V is drain voltage, T the sample temperature, and C the constant independent of V. From the straight line of the right-hand side of Fig. 2, the drain current is proportional to $V^{4.5}$, so that the characteristic temperature, T_0, is 1026 K, which is in good agreement with the value obtained from the numerical analysis of the space charge limited current.

In summary, the space charge limited current in n^+-i-n^+ a-Si:H in TFT at a gate voltage of -2.5 V was used to determine the density of states in the gap. We show that the assumptions needed to obtain the density of states in a-Si:H in n^+-i-n^+ sandwich structure, can be equally applied to determine the density of states at the Fermi level of a-Si:H in TFT. The method can be used to measure the density of states of the a-Si:H layer during various fabrication steps of a-Si:H TFT-LCDs.

This work was supported by the Korea Science and Engineering Foundation through the Semiconductor Physics Research Center.

[1] M. J. Powell, IEEE Trans. Electron Device **ED-36**, 2753 (1989).
[2] K. Hiranaka, T. Yoshimura, and T. Yamaguchi, Jpn. J. Appl. Phys. **28**, 2197 (1989).
[3] J.-L. Lin, W.-J. Sah, and S.-C. Lee, IEEE Electron Device Lett. **EDL-12**, 120 (1991).
[4] M. Matsui, H. Nagayoshi, G. Muto, M. Tanimoto, K. Kuroiwa, and Y. Tarui, Jpn. J. Appl. Phys. **29**, 62 (1990).
[5] K. Suzuki, in *Amorphous and Microcrystalline Semiconductor Devices: Optoelectronic Devices*, edited by J. Kanicki (Artech House, Boston, 1991), Chap. 3.
[6] K. D. Mackenzie, P. G. LeComber, and W. E. Spear, Philos. Mag. B **46**, 377 (1982).
[7] S. Gangopadhyay, S. Iselborn, H. Rubel, B. Schroder, and J. Geiger, Philos. Mag. B **51**, L33 (1985).
[8] C. Manfredotti and L. Montaldi, J. Non-Cryst. Solids **77&78**, 347 (1985).
[9] S. C. Kim, M. H. Jung, and J. Jang, Appl. Phys. Lett. **58**, 281 (1991).
[10] J. Jang, T. G. Kim, S. C. Kim, J. M. Jun, and K. C. Park, Appl. Phys. Lett. **60**, 2880 (1992).
[11] M. S. Shur, M. Hack, and C. Hyun, J. Appl. Phys. **56**, 382 (1984).
[12] W. den Boer, J. Phys. (France) Colloq. **42**, C4-451 (1981).
[13] R. L. Weisfield, J. Appl. Phys. **54**, 6401 (1983).
[14] A. Rose, *Concepts in Photoconductivity and Allied Problems* (Wiley-Interscience, New York, 1963), Chap. 4.

Downloaded 16 Apr 2013 to 143.248.118.122. This article is copyrighted as indicated in the abstract. Reuse of AIP content is subject to the terms at: http://apl.aip.org/about/rights_and_permissions