Ultra-thin Body SOI MOSFET for Deep-sub-tenth Micron Era

Yang-Kyu Choi, Kazuya Asano*, Nick Lindert, Vivek Subramanian, Tsu-Jae King, Jeffrey Bokor and Chenming Hu

Department of Electrical Engineering and Computer Sciences, University of California at Berkeley, CA 94720 USA
Tel: (510) 643-2558; FAX: (510) 643-2636; e-mail: ykchoi@eecs.berkeley.edu
* Present address : NKK Corp., Japan

A 40nm-gate-length ultra-thin body (UTB) nMOSFET is demonstrated. A self-aligned thin body SOI device has previously been proposed for suppressing the short channel effect. UTB structure can eliminate the punchthrough path between source and drain [1] and provide a more evolutionary alternative to the double-gate MOSFET for deep-sub-tenth micron technology. Fig. 1 and Fig. 2 illustrated the advantage of using UTB. The data in these figures were obtained through device simulation (with the aid of Silvaco ATLAS) using simple doping profiles for the body (uniform 10^{15} cm^{-3}) and S/D (simple Gaussian). 8nm thick UTB can meet the goals of 3nA/um I_{off} and 600uA/um I_{on} for L_g=25nm. Smaller L_g can be accommodated by scaling the thickness of the ultra-thin body.

Our novel UTB device fabrication process is shown in Fig. 3. 100nm SOI film (BOX=400nm) was reduced to 20nm by thermal oxidation (Fig. 3a). The 2.4nm thin gate oxide illustrated in the TEM picture of Fig. 5 was grown at 750 °C and 15min. For tuning the threshold voltage, B-in-situ doped poly-SiGe was adopted because the work function can be adjusted with the Ge mole fraction [2]. Therefore, the channel can be lightly doped to eliminate a dopant or V_t fluctuation effect. All masking steps were done by i-line lithography. The gate pattern was defined by using the i-line resist followed by resist ashing and the oxide hard mask trimming. The oxide spacer was formed in a conventional manner. In-situ-doped poly-Si was deposited and patterned with the same active mask as shown in Fig. 3c. A thin cap oxide was deposited (Fig. 3c) in order to protect the S/D and for a wide process window during the subsequent photo-resist etch-back. The resist-etch back process was used to make raised S/D (Fig. 3d, e), which are self-aligned to the gate for the reduction of the parasitic resistance as shown in tilted SEM picture of Fig. 4b. Metal electrodes in this experiment were not used so that additional S/D extension diffusion by RTA can be performed. Fig. 6 shows the cross-sectional TEM of a device that has 90nm L_g and 40nm L_{eff}.

Typical I-V characteristics of the 40nm channel length device are illustrated in Fig. 7. Fig. 8 shows that DIBL is suppressed even though there is little channel doping ($N_{sub} = 5.4 \times 10^{14}$ cm^{-3}). The subthreshold swing is 87 mV/dec. Good Vt roll-off characteristics are shown in Fig. 9. Fig. 10 shows that the parasitic series resistance is 240Ω. This value is high because the S/D extension doping was not optimized.

In short, the UTB SOI MOSFET with self-aligned raised poly-Si S/D shows well-behaved I-V characteristics. The special features of the new device structure for deep-sub-tenth-micron CMOS are : (1) ultra-thin body for suppressing the short-channel effects. (2) self-aligned raised poly-Si S/D are raised on UTB to reduce the parasitic resistance. (3) gate is patterned with i-line lithography and reduced from 0.5um to 0.045um with ashing+trimming technique. (4) the topography is quite flat and the process is similar to today's planar CMOS technology.

In conclusion, an ultra-thin body SOI nMOSFET is demonstrated to be a promising structure for deep-sub-tenth micron CMOS technology. 40nm channel length was achieved with the ultra-thin body which suppresses the short-channel effect. A 12nm-gate-length CMOS should be attainable if a 4nm ultra-thin body is used.

Acknowledgement : This research is sponsored by DARPA AME Program under Contract N66001-97-1-8910

[1] B. Yu et al., Int'l Semicon. Device Res. Symp., p. 623-626,
[2] T.-J. King et al., IEEE Trans. on Electron Devices, vol.ED-41, no.2, p. 228-231, 1994.

0-7803-5410-9/99/$10.00 © 1999 IEEE

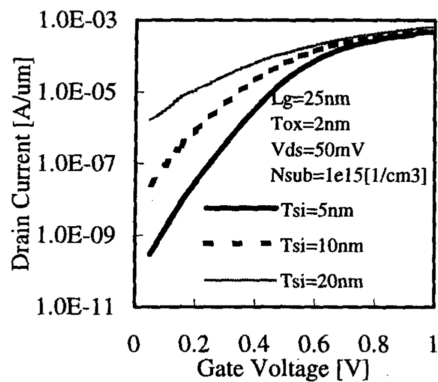


Fig. 1 Impact of Tsi on the Ids-Vgs characteristics of UTB SOI device.

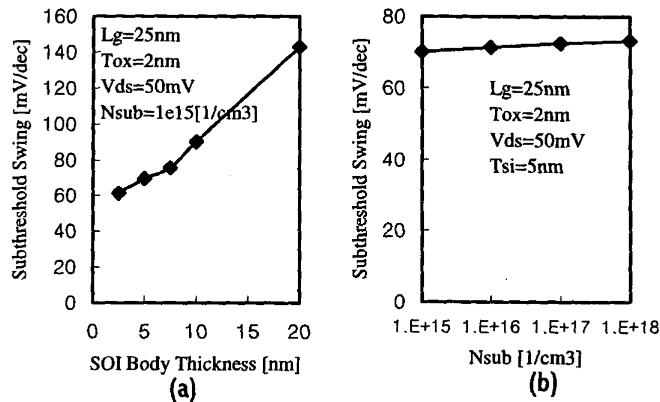
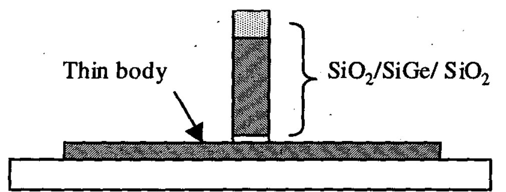
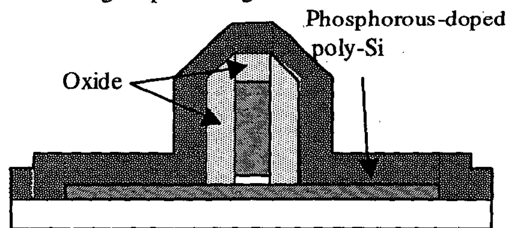


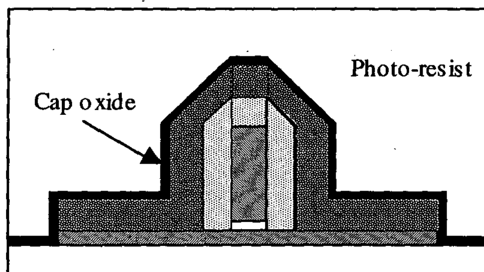
Fig. 2 Impact of (a) Tsi and (b) Nsub on the subthreshold swing of UTB SOI device



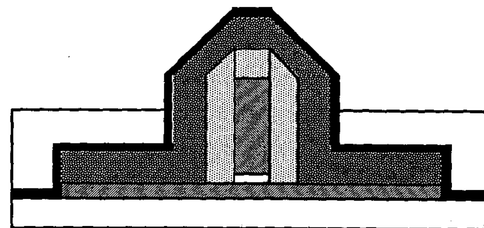
(a) After thin body formation, active area and gate patterning.



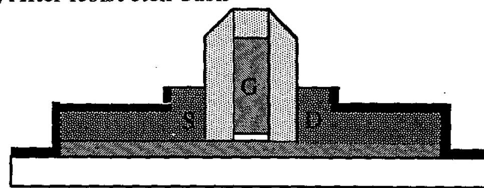
(b) After oxide spacer formation and n+ poly Si deposition



(c) After S/D patterning and the deposition of cap oxide, photo resist was coated.

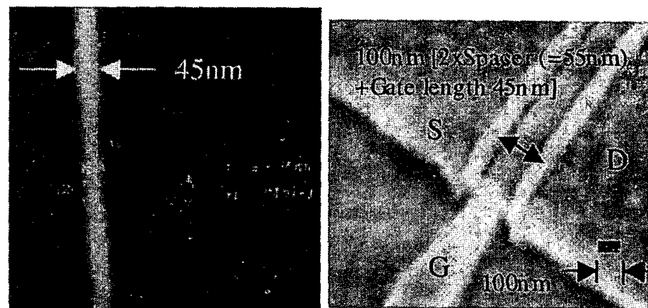


(d) After resist etch-back



(e) After cap oxide and n+ poly Si etch back

Fig. 3 Process flow of UTB SOI MOSFET [(a)~(e)]



(a) After gate etch (Lg=45 nm) (b) After poly-Si etch-back

Fig. 4 SEM picture of UTB SOI MOSFET

3.7.2

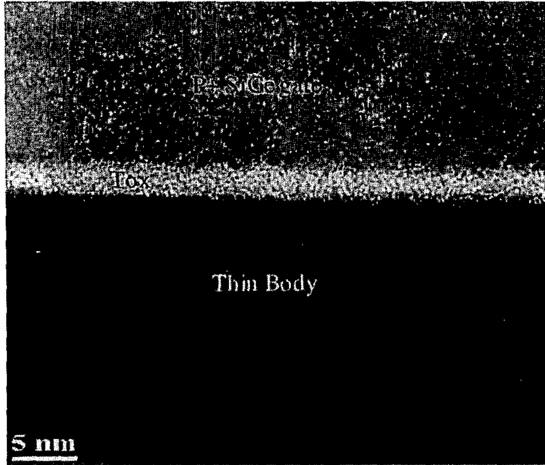


Fig. 5 Cross-sectional TEM picture of 2.4 nm gate oxide

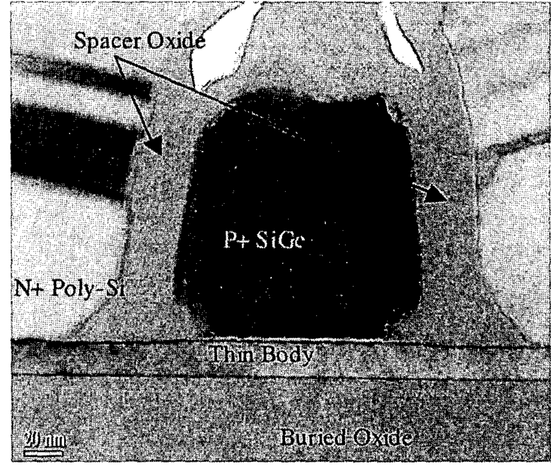


Fig. 6 Cross-sectional TEM picture of 90nm gate

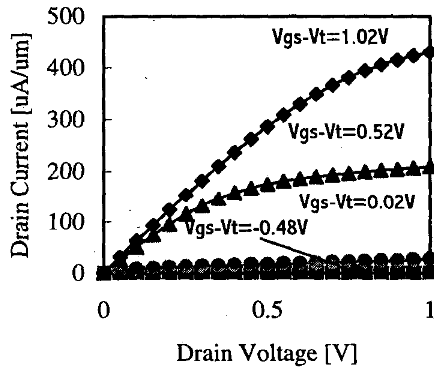


Fig. 7 UTB SOI nMOSFET Ids-Vds characteristics for 50nm gate length and 20nm Tsi

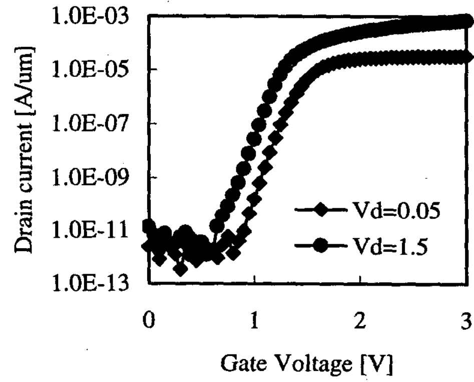


Fig. 8 UTB SOI nMOSFET Ids-Vgs characteristics for 50nm gate length and 20nm Tsi

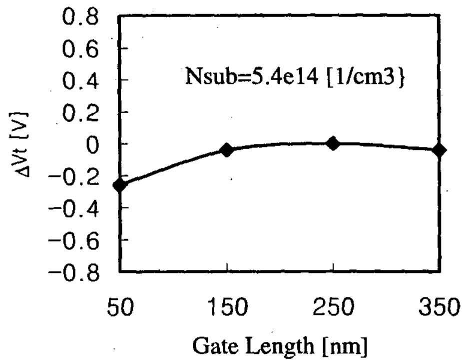


Fig. 9 Threshold voltage dependence on the channel length

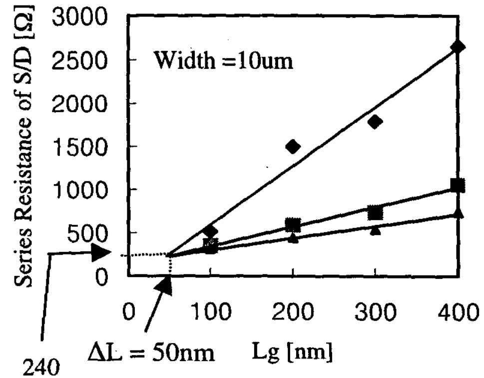


Fig. 10 Extraction of parasitic S/D series resistance and ΔL

3.7.3