Analysis and Suppression of SSN Noise Coupling Between Power/Ground Plane Cavities Through Cutouts in Multilayer Packages and PCBs

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***Abstract*—We introduce a model of simultaneous switching noise (SSN) coupling between the power/ground plane cavities through cutouts in high-speed and high-density multilayer packages and printed circuit boards (PCBs). Usually, the cutouts are used in multilayer plane structures to isolate the SSN of noisy digital circuits from sensitive analog circuits or to provide multiple voltage levels. The noise-coupling model is expressed in terms of the transfer impedance. The proposed modeling and analysis results are compared with measured data up to 10 GHz to demonstrate the validity of the model. It is demonstrated that the cutout is the major gate for SSN coupling between the plane cavities, and that substantial SSN coupling occurs between the plane cavities through the cutout at the resonant frequencies of the plane cavities. We also analyze and discuss the coupling mechanism and characteristics of the noise coupling, from which we evaluate a method of suppression of the SSN coupling. Proper positioning of the cutout and the devices at each plane cavity achieves significant noise suppression at certain resonant frequencies. The suggested suppression method of the SSN coupling was successfully proved by frequency domain measurement and time domain analysis.**

***Index Terms*—Cutout, modeling, multilayer package, multilayer printed circuit board (PCB), noise coupling, power/ground noise, simultaneous switching noise (SSN).**

I. Introduction

THE design of low-impedance and low-noise power/ground distribution networks for high-speed digital or mixed-signal packages and printed circuit boards (PCBs) has become a major challenge due to significant switching noise [1]. The switching power dissipation becomes higher, and the average supply current is increased significantly, even if the power supply voltage is reduced by advances in semiconductor device technology.[1] As a result, combined with higher clock frequencies, the increased switching current changes (di/dt) produce considerable power supply switching noise that ultimately degrades the eye patterns and timing margins on critical clock and signal paths, thereby limiting the attainable clock frequencies in digital devices or systems. This limitation is further compounded by the reduced voltage noise margins in complementary metal–oxide–silicon (CMOS) logic circuits that result from the power supply voltage reduction [2]. Furthermore, this power supply simultaneous switching noise (SSN) can be a source of electromagnetic noise coupling and interference to nearby interconnections, circuits, and other devices that is difficult to circumvent. Therefore, the switching noise must be under the designer's control to ensure reliable circuit, device, and system operation.

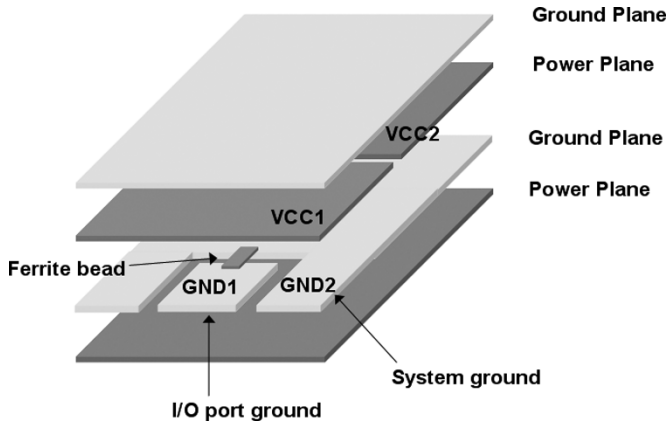

Fig. 1. Example of the cutout structures in multilayer package and PCB. These cutouts are designed to isolate power supply noise and to provide several voltage levels in a power plane. A ferrite bead is used for dc connection between the split grounds.

High-frequency switching noise is generated when a rapid switching of current occurs in inductive circuit components of the power/ground network. These inductive parasitic circuit elements of the network are due to the interconnection structures, such as the packaging, vias on the PCB, traces on the PCB, and decoupling capacitors [3]. The SSN causes the voltage level at a position in a plane cavity to fluctuate; it propagates to other positions by electromagnetic propagation in the plane cavity and is also coupled to other plane cavities through cutouts or through other interconnection structures, including the via [4]. The analysis and measurement of the noise coupling through the cutout is the main subject of this paper, as it is the major gate for noise coupling between the plane cavities. Usually, the cutouts are used to partition the planes or to separate the planes to isolate the SSN of noisy digital circuits from sensitive analog circuits or to provide various voltage levels in a power plane layer, as illustrated in Fig. 1. In other cases, the cutout is made unintentionally to allocate a series of parallel-aligned vias for signal

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or power/ground connections, or a group of through-holes to mount devices, packages, or connectors on a multilayer package or PCB.

Several modeling methodologies have been proposed for the analysis of multilayered distribution networks, including a two-dimensional discrete transmission line model [5], a quasi-three-dimensional distributed model [6], and a cavity resonator model [7]–[9]. These methodologies assume that the plane cavities are isolated from each other and that noise couplings between the plane cavities are not to be considered. This approach enables modeling of the multilayer power distribution network by simply cascading each plane cavity, which is modeled as electrically uncoupled. Field penetration through the metal planes has been studied [10]. This study showed that the assumption of noncoupling between plane cavities is only valid for thick metal planes with highly conductive metal film, in which the skin depth of the metal plane is smaller than the metal plane thickness. We have extended this study to the case of cavities with cutouts. If there are cutouts in the planes, the skin effect assumption cannot be applied around the cutout and substantial coupling between plane cavities occurs through the cutouts.

In this paper, we introduce a modeling and analysis of SSN coupling between plane cavities through the cutouts in multilayer planes. To describe the coupling mechanism through the cutouts, we have developed an analytical model of a multilayer plane structure that has cutouts in its planes. The validity and accuracy of the analytical model has been validated in a frequency range of up to 10 GHz by high-frequency time and frequency-domain measurements. The measurements show acceptable agreement with the predictions based on the model and its analysis.

Based on the modeling and measurement, it is demonstrated that the cutout is the major cause of power/ground noise coupling between the plane cavities, and that substantial SSN coupling occurs between the plane cavities, through the cutout, at resonant frequencies of the plane cavities. The resonant frequencies are determined by the shape, material, and size of the partitioned plane cavities. We also have analyzed, and discuss, the coupling mechanism and characteristics of the noise coupling as functions of the positions of the cutout, the noise source in a plane cavity and the receiver in the other plane cavity in terms of the transfer impedance and time domain noise waveform. From the analysis, we propose a suppression method of noise coupling between the plane cavities through the cutout. Proper positioning of the cutout and the devices at each plane cavity achieves significant noise suppression at certain resonant frequencies. We used a four-layer and two-cavity power/ground structure on a PCB for the analysis and measurement to demonstrate the SSN suppression effect. The coupling noise suppression effect is demonstrated in terms of the transfer impedance at the resonant frequencies, and the time-domain SSN noise waveforms by changing the locations of the noise source and the noise receiver. The suggested noise suppression method can be usefully adopted in high-performance package and PCB design.

Section II describes the analytical modeling of SSN coupling through the cutouts. The transfer impedances from the analytical model and measurement are compared to demonstrate the model's accuracy. In Section III, a suppression method of the coupled noise is presented. The suppression effect of the optimal positioning method is demonstrated in both the frequency and time domain using the analytical model and measurement.

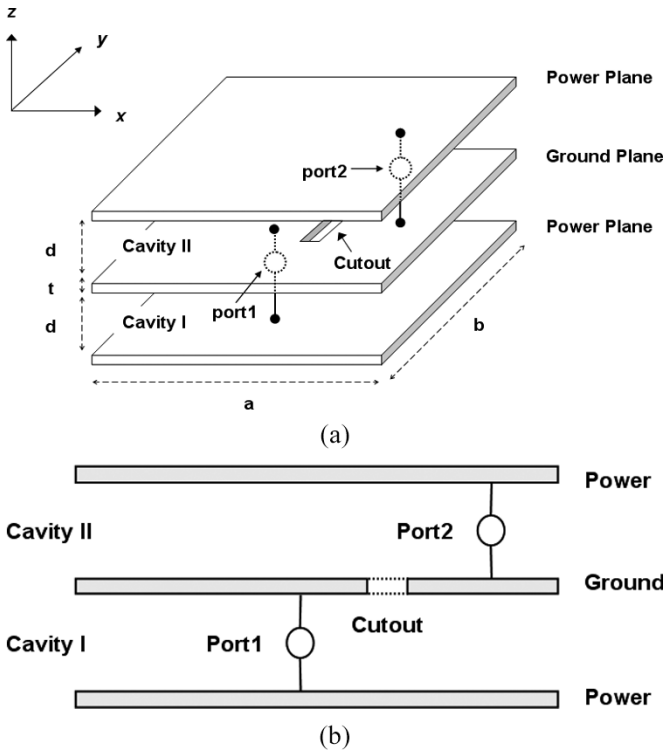

Fig. 2. Three-layer power/ground plane cavity structure, which has a cutout in the second metal plane. (a) 3-D view. (b) Cross section.

II. Modeling of SSN Coupling Through Cutouts in Multilayer Power/Ground Cavities

A. Analytical Model

Consider a multilayer plane cavity structure having a cutout in the second conductor plane, as shown in Fig. 2. The planes of dimension "$a \times b$" are separated by a distance d. The cutout dimension is "$L \times W$," where L and W are the length and the width of the cutout, respectively. When the current switches at port 1, it excites electric and magnetic fields in cavity I. Because $a, b \gg d$, where d is much smaller than the wavelength of the field, the major field components are E_z, H_x, and H_y. These field components can be calculated using the cavity resonator model [7], [8], [14]

$$E_{z,\mathrm{cavI}} = \frac{j\omega\mu J_s}{ab} \sum_{m=0}^{\infty}\sum_{n=0}^{\infty} \frac{\varepsilon_m^2 \varepsilon_n^2}{k_{mn}^2 - k^2} \cos\frac{m\pi x_i}{a} \times \cos\frac{n\pi y_i}{b} \cos\frac{m\pi x_j}{a} \cos\frac{n\pi y_j}{b} \tag{1a}$$

$$H_{x,\mathrm{cavI}} = \frac{J_s}{ab} \sum_{m=0}^{\infty}\sum_{n=0}^{\infty} \frac{\varepsilon_m^2 \varepsilon_n^2}{k_{mn}^2 - k^2} \frac{n\pi}{b} \cos\frac{m\pi x_i}{a} \times \cos\frac{n\pi y_i}{b} \cos\frac{m\pi x_j}{a} \sin\frac{n\pi y_j}{b} \tag{1b}$$

$$H_{y,\mathrm{cavI}} = \frac{J_s}{ab} \sum_{m=0}^{\infty}\sum_{n=0}^{\infty} \frac{\varepsilon_m^2 \varepsilon_n^2}{k_{mn}^2 - k^2} \frac{-m\pi}{a} \cos\frac{m\pi x_i}{a} \times \cos\frac{n\pi y_i}{b} \sin\frac{m\pi x_j}{a} \cos\frac{n\pi y_j}{b} \tag{1c}$$

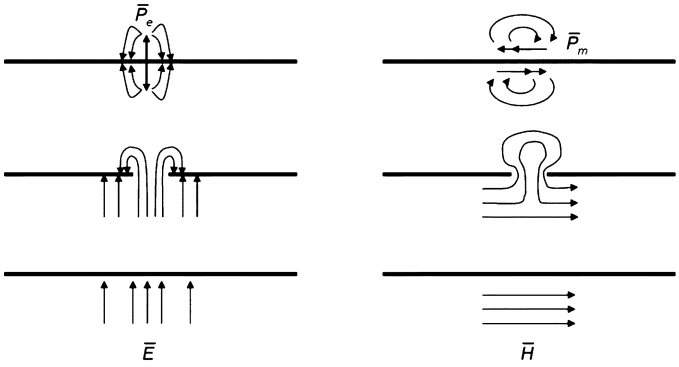

Fig. 3. Illustration of Bethe's small aperture coupling theory, where the fringing field effect of the cutout can be replaced by the polarization currents and are missed.

where, (x_i, y_i) and (x_j, y_j) are the coordinates of port 1 and the center position of the cutout, respectively. In the above (1), $k = k' - jk''$ where $k' = \omega\sqrt{\mu\varepsilon}$ and, $k'' = \omega\sqrt{\mu\varepsilon}(\tan\delta/2 + r/(2d))$, $k_{mn}^2 = (m\pi/a)^2 + (n\pi/b)^2$ where m, n are propagating modes in the cavity, and μ, ε and $tan\delta$ are the permeability, permittivity, and loss tangent of the dielectric material, respectively, $r = \sqrt{2/(\omega\mu\sigma)}$, where σ is the conductivity of the metallization, and $\varepsilon_m, \varepsilon_n = 1$ for $m, n = 0$, and $\sqrt{2}$, otherwise.

Because the cutout is designed in the second conductor layer in Fig. 2, the electric and the magnetic fields in the cavity I will fringe through and around the cutout. These fringing fields are similar to those from an electric polarization current, $\overline{P}_e$ normal to the plane and a magnetic polarization current, $\overline{P}_m$ tangential to the plane, both at the center of the cutout as shown in Fig. 3 [11]. This similarity suggests that polarization currents $\overline{P}_e$ and $\overline{P}_m$ can replace the fringing effect of the cutout. This approximation is valid and gives reasonable results on the assumptions that the cutout is small relative to the electrical wavelength and is away from the plane edges and that, in addition, the current source is not located too close to the cutout. Otherwise, the similarity between the fringing fields around and through the cutout and those from the polarization currents is lost, which degrades the accuracy of the model.

Quantitatively, the polarization currents are given by

$$\overline{P}_e = \varepsilon_0\alpha_e\overline{E}_n\delta(x - x_0)\delta(y - y_0)\delta(z - z_0) \quad (2a)$$

$$\overline{P}_m = -\alpha_m\overline{H}_t\delta(x - x_0)\delta(y - y_0)\delta(z - z_0) \quad (2b)$$

where the proportionality constants α_e and α_m are defined as the electric and the magnetic polarizabilities of the cutout, respectively, and (x_0, y_0, z_0) are the coordinates of the center of the cutout. The electric and the magnetic polarization currents are proportional to the strength of the normal electric field and the tangential magnetic fields, respectively. The normal electric field strength, E_n in (2a), corresponds to $E_{z,\mathrm{cavI}}$ in (1a), and the tangential magnetic field strength, H_t in (2b), corresponds to $H_{x,\mathrm{cavI}}$ in (1b) and $H_{y,\mathrm{cavI}}$ in (1c), because both x and y directional magnetic fields are tangential to the plane surface. Therefore, (2) can be rewritten as

$$\overline{P}_e = \varepsilon_0\alpha_e\overline{E}_{z,\mathrm{cavI}} \quad (3a)$$

$$\overline{P}_m = -\alpha_{mx}\overline{H}_{x,\mathrm{cavI}} - \alpha_{my}\overline{H}_{y,\mathrm{cavI}} \quad (3b)$$

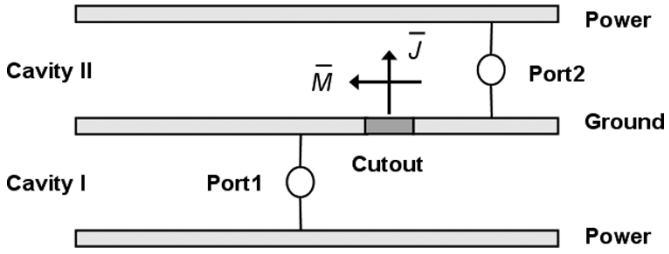

Fig. 4. Illustration of the equivalent current sources of the cutout. The cutout can be replaced by the equivalent current sources, $\overline{J}$ and $\overline{M}$, as if the cutout was filled in to form a solid conductor plane.

where α_{mx} is the magnetic polarizability for $H_{x,\mathrm{cavI}}$ and α_{my} is that for $H_{y,\mathrm{cavI}}$.

The coupling through the cutout is modeled as equivalent currents, as described by Pozar [11] because of its structural similarity. The major difference in the structure is that Pozar deals with rectangular waveguides in which fields propagate, whereas this paper describes plane cavities where fields reflect off the cavity walls causing multiple scattering as the reflected fields can in turn couple back through the cutout. The coupling of reflected fields is significant near resonance, although it is relatively weak when the cutout is small. To take into account the multiple-scattering effect, we need to solve every reflected field and its coupling, as does a full-wave numerical tool. In this paper, the model adopts stationary fields in (1) as primary fields in cavity I for quick estimation and simplicity of modeling. This approximation again requires the small cutout assumption. The polarizabilities for the fields are empirically extracted by fitting to measured S-parameters

$$\alpha_e = \frac{3\pi WL^2}{16} \quad (4a)$$

$$\alpha_{mx} = \frac{\pi WL^2}{16}\frac{1}{3.5}$$

$$\alpha_{my} = \frac{\pi LW^2}{16}\frac{1}{3.5} \quad (4b)$$

where W and L are the width and length of the cutout, respectively, as shown in Fig. 5(a). In case of a large cutout, where the dimensions W or L are comparable to the wavelength, an aperture resonance correction factor [12] and field averaging factor [13] should be included in the polarizabilities to account for cutout resonance and the nonuniform field distribution along the cutout dimensions.

The electric and the magnetic polarization currents can be related to the electric and magnetic current sources [11]

$$\overline{J} = j\omega\overline{P}_e \quad (5a)$$

$$\overline{M} = j\omega\mu_0\overline{P}_m \quad (5b)$$

The cutout may be replaced by equivalent current sources, $\overline{J}$ and $\overline{M}$, as if the cutout is filled by a solid conductor plane, as depicted in Fig. 4. The next step is to find out the fields in cavity II due to the equivalent current sources $\overline{J}$ and $\overline{M}$.

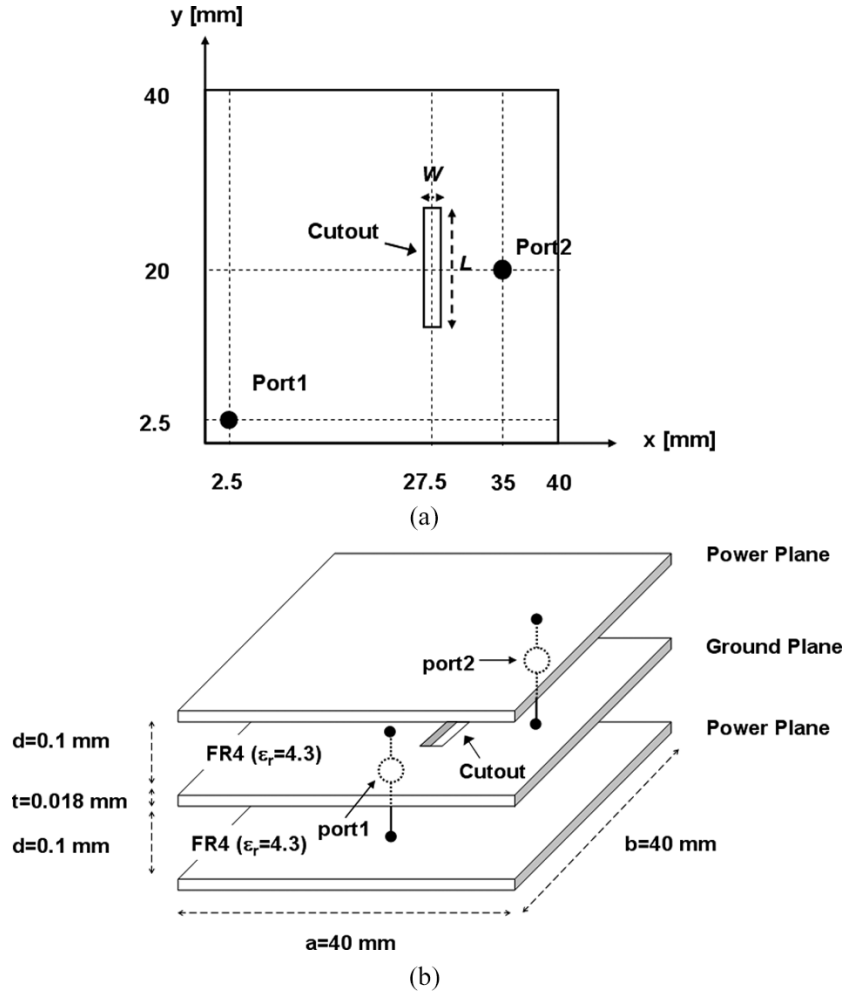

Fig. 5. Test sample structure. (a) Top view of the test samples having port 1 located at (2.5 mm, 2.5 mm) and port 2 located at (35 mm, 20 mm). (b) 3-D view of the test sample, where the cutout is located at (27.5 mm, 20 mm) on the second metal layer, and its dimension is 0.5 × 10 mm.

Let the stationary fields in cavity II be expressed as [14]

$$E_{z,\text{cavII}} = \sum_{m=0}^{\infty}\sum_{n=0}^{\infty} A_{mn}\frac{\varepsilon_m\varepsilon_n}{\sqrt{ab}} \times \cos\frac{m\pi x}{a}\cos\frac{n\pi y}{b} \tag{6a}$$

$$H_{x,\text{cavII}} = \sum_{m=0}^{\infty}\sum_{n=0}^{\infty} A_{mn}\frac{\varepsilon_m\varepsilon_n}{j\omega\mu\sqrt{ab}}\frac{n\pi}{b} \times \cos\frac{m\pi x}{a}\sin\frac{n\pi y}{b} \tag{6b}$$

$$H_{y,\text{cavII}} = \sum_{m=0}^{\infty}\sum_{n=0}^{\infty} A_{mn}\frac{\varepsilon_m\varepsilon_n}{j\omega\mu\sqrt{ab}}\frac{-m\pi}{a} \times \sin\frac{m\pi x}{a}\cos\frac{n\pi y}{b} \tag{6c}$$

where A_{mn} is the unknown amplitude of field of the (m,n) mode.

From Poynting's theorem, the power delivered by the current sources $\overline{J}$ and $\overline{M}$ (P_s), is equal to the sum of the power transmitted through the edge surface (P_o), the power lost to heat in the volume (P_l), and 2ω times the net reactive energy stored in the volume [11]

$$P_s = P_o + P_l + 2j\omega(W_m - W_e) \tag{7}$$

Each term in (7) can be found from (1), (3), (5), and (6) as

$$P_o = \frac{1}{2}\oint_S \overline{E}\times\overline{H}^*\cdot d\overline{s} = 0 \tag{8a}$$

$$\begin{aligned} P_s &= -\frac{1}{2}\int_V (\overline{E}\cdot\overline{J}^* + \overline{H}^*\cdot\overline{M})dv \\ &= \sum_{m=0}^{\infty}\sum_{n=0}^{\infty} A_{mn}\frac{-1}{2}\frac{\varepsilon_m\varepsilon_n}{\sqrt{ab}} \times\Bigg(\cos\frac{m\pi x_j}{a}\cos\frac{n\pi y_j}{b}\overline{J}^* - j\frac{1}{\omega\mu} \\ &\quad\times\Big(\frac{n\pi}{b}\cos\frac{m\pi x_j}{a}\sin\frac{n\pi y_j}{b}\overline{M}_x \\ &\quad -\frac{m\pi}{a}\sin\frac{m\pi x_j}{a}\cos\frac{n\pi y_j}{b}\overline{M}_y\Big)\Bigg) \end{aligned} \tag{8b}$$

$$\begin{aligned} P_l &= \frac{R_s}{2}\int_{S_0}|\overline{H}|^2 ds + \frac{w}{2}\int_V \varepsilon''|\overline{E}|^2 dv \\ &= \sum_{m=0}^{\infty}\sum_{n=0}^{\infty} A_{mn}^2 \\ &\quad\times\left[\frac{R_s}{\omega^2\mu^2}\left(\left(\frac{m\pi}{a}\right)^2+\left(\frac{n\pi}{b}\right)^2\right)+\frac{\omega}{2}\varepsilon'' d\right] \end{aligned} \tag{8c}$$

$$W_e = \frac{\varepsilon}{4}\int_V \overline{E}\cdot\overline{E}^* dv = \sum_{m=0}^{\infty}\sum_{n=0}^{\infty} A_{mn}^2 \frac{\varepsilon d}{4} \tag{8d}$$

$$W_m = \frac{\mu}{4}\int_V \overline{H}\cdot\overline{H}^* dv = \sum_{m=0}^{\infty}\sum_{n=0}^{\infty} A_{mn}^2 \frac{\mu}{4}\frac{d}{\omega^2\mu^2}\left(\left(\frac{m\pi}{a}\right)^2+\left(\frac{n\pi}{b}\right)^2\right). \tag{8e}$$

In (8c), $R_s = \sqrt{\omega\mu_0/2\sigma}$ is the surface resistivity of the conductor planes, and $\varepsilon'' = \varepsilon_r\varepsilon_0\tan\delta$. The power transmitted through the edge surface (P_o) is zero because the tangential magnetic fields at the edge surface are zero. This result is derived from the assumption that, at places along the plane periphery, the boundary condition is given as a magnetic wall. The open boundary assumption is valid only when the dielectric thickness is much smaller than the wavelength $(4d \ll \lambda)$.

The unknown amplitude of the fields A_{mn} can be determined from (7) and (8) as (9), shown at the bottom of the page. In (9), $\overline{J}$, $\overline{M}_x$, and $\overline{M}_y$ can be determined from (1), (3), and (5). By analogy to *RLC* resonant circuits, the stored electric and magnetic energies are equal at resonance. Therefore, the denominator of (9) is minimized at the resonant frequency, $f_{mn} = k_{mn}/(2\pi\sqrt{\varepsilon\mu})$, which results in maximizing A_{mn}.

Finally, the transfer impedance Z_{21} can be obtained as

$$Z_{21} = \frac{E_{z,\mathrm{cavII}}\times d}{J_s} = \sum_{m=0}^{\infty}\sum_{n=0}^{\infty}\frac{A_{mn}}{J_s}\frac{\varepsilon_m\varepsilon_n}{\sqrt{ab}} d\cos\frac{m\pi x_k}{a}\cos\frac{n\pi y_k}{b} \tag{10}$$

where (x_k, y_k) are the coordinates of port 2. The transfer impedance contains the information of the plane dimensions, the material properties, the ports and cutout locations, and the cutout dimensions.

The input impedance is obtained similarly. The presence of the cutout also results in scattered waves in the primary plane cavity (cavity I). If the cutout is assumed to be filled, the electric field in the cavity I at the center of the cutout can be written as

$$E_{z,\mathrm{cavI}} = \frac{j\omega\mu J_s}{ab}\sum_{m=0}^{\infty}\sum_{n=0}^{\infty}\frac{\varepsilon_m^2\varepsilon_n^2}{k_{mn}^2-k^2}\left(\cos\frac{m\pi x_i}{a}\right)^2\left(\cos\frac{n\pi y_i}{b}\right)^2. \tag{11}$$

The equivalent currents on the cavity I side of the center conductor plane are in the opposite direction to those on the cavity II side as depicted in Fig. 3. The fields scattered by the cutout are considered to be produced by the equivalent currents, $-\overline{P}_e$ and $-\overline{P}_m$, where $\overline{P}_e$ and $\overline{P}_m$ can be found from (3). Then, the scattered electric field in the cavity I can be written as

$$E_{\mathrm{scattered,cavI}} = \sum_{m=0}^{\infty}\sum_{n=0}^{\infty} A_{mn}\frac{\varepsilon_m\varepsilon_n}{\sqrt{ab}}\cos\frac{m\pi x_i}{a}\cos\frac{n\pi y_i}{b}. \tag{12}$$

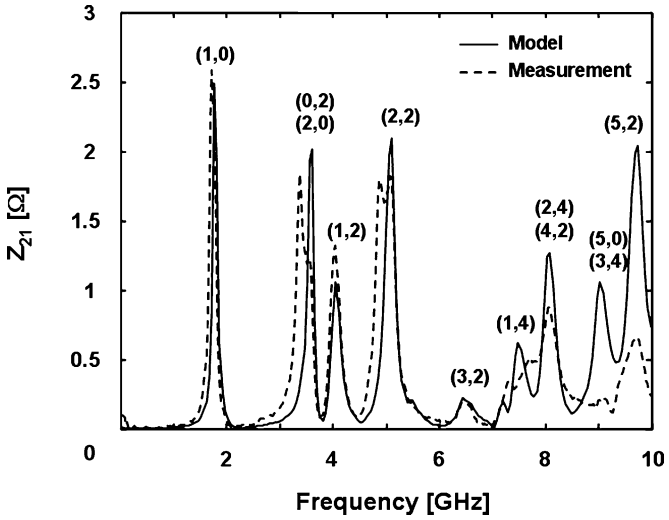

Fig. 6. Comparison of the modeling and the measurement of the Z_{21}-parameter up to 10 GHz. The solid line represents the transfer impedance calculated using the analytical model, whereas the dotted line represents the transfer impedance obtained from the measured S-parameters.

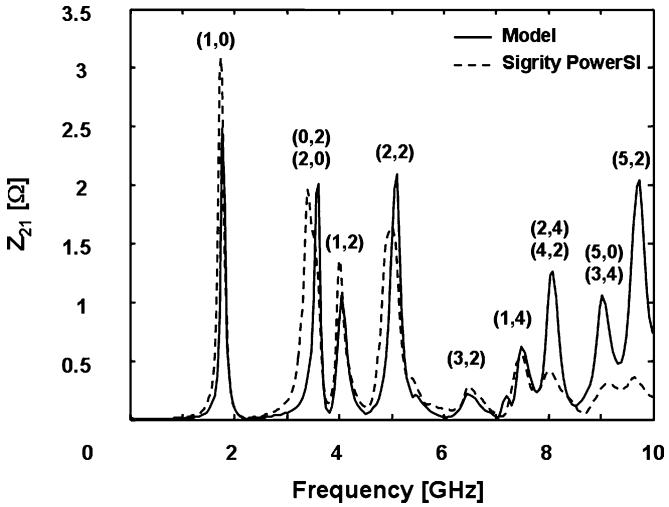

Fig. 7. Comparison of the modeling and the full-wave simulation of the Z_{21}-parameter. The solid line represents the transfer impedance calculated using the analytical model, whereas the dotted line represents the transfer impedance obtained using Sigrity PowerSI.

The complete electric field can now be written as

$$E_{\mathrm{cavI}} = E_{z,\mathrm{cavI}} + E_{\mathrm{scattered,cavI}}. \tag{13}$$

The input impedance can be written as

$$Z_{11} = \frac{E_{\mathrm{cavI}}\times d}{J_s}. \tag{14}$$

$$A_{mn} = \frac{-\frac{1}{2}\frac{\varepsilon_m\varepsilon_n}{\sqrt{ab}}\left(\cos\frac{m\pi x_j}{a}\cos\frac{n\pi y_j}{b}\overline{J}^* - j\frac{n\pi}{\omega\mu b}\cos\frac{m\pi x_j}{a}\sin\frac{n\pi y_j}{b}\overline{M}_x + j\frac{m\pi}{\omega\mu a}\sin\frac{m\pi x_j}{a}\cos\frac{n\pi y_j}{b}\overline{M}_y\right)}{\frac{R_s}{\omega^2\mu^2}\left(\left(\frac{m\pi}{a}\right)^2+\left(\frac{n\pi}{b}\right)^2\right)+\frac{\omega}{2}\varepsilon'' d + 2jw\left(\frac{\mu}{4}\frac{d}{\omega^2\mu^2}\left(\left(\frac{m\pi}{a}\right)^2+\left(\frac{n\pi}{b}\right)^2\right)-\frac{\varepsilon d}{4}\right)} \tag{9}$$

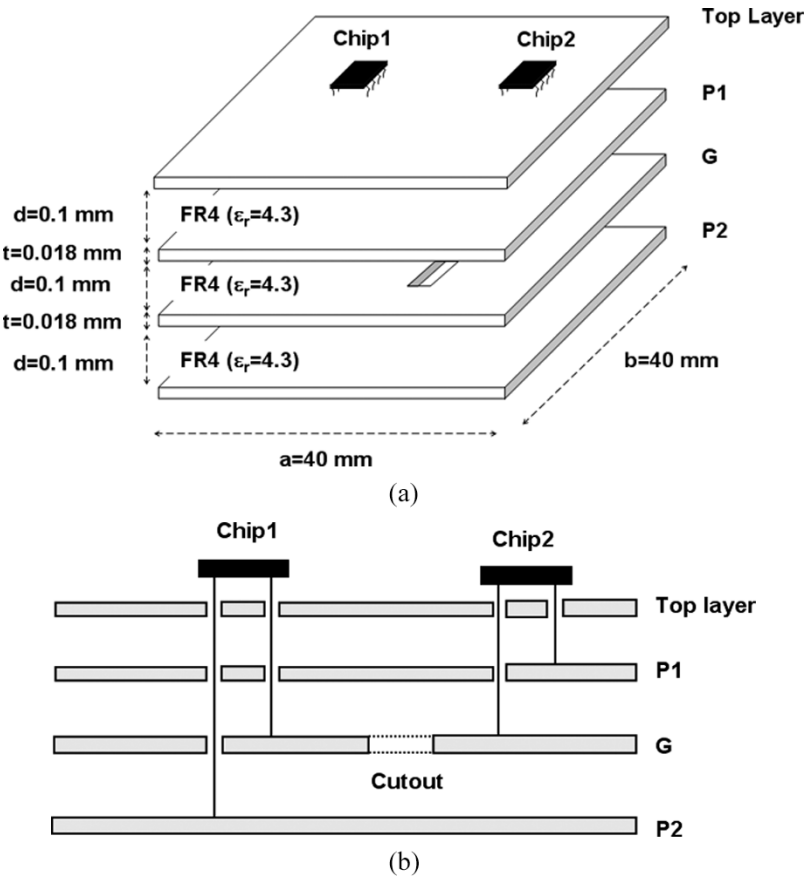

Fig. 8. Structure of the test sample to demonstrate the port optimization method. In the test sample, chip 1 is powered by P2 plane and ground layers and chip 2 is powered by P1 and ground layers. The third layer serves as a common ground, which has a cutout on it. (a) 3-D view. (b) Cross section.

B. Comparison of Transfer Impedance Z21 Parameter From the Model and Measurement

Test samples were designed and fabricated for S-parameter measurement and the measured results were compared with the model results from (10) to verify the accuracy and usefulness of the model. Fig. 5 illustrates the layout and the cross section of one of the test samples. It consists of three conductor layers with dimensions of $a = 40$ mm and $b = 40$ mm. FR4 was used as the dielectric material with a permittivity $\varepsilon_r = 4.3$ and $d = 0.1$ mm. Copper metallization was used with a metal thickness $t = 0.018$ mm and conductivity $\sigma = 5.813 \times 10^7$ S/m. The cutout is located at $x = 27.5$ mm and $y = 20$ mm, with dimensions of $L = 10$ mm and $W = 0.5$ mm. The coordinates of ports 1 and 2 were ($x = 2.5$ mm, $y = 2.5$ mm), and ($x = 35$ mm, $y = 20$ mm), respectively. Port 1 was used as the source port and port 2 was used as the coupled port. The measured S-parameters were converted to Z-parameters using the following (15), and were compared with the analytical model. Theoretical data were obtained by solving the previous equations with $m, n = 0$ to 20 modes using MATLAB.

$$Z_{21} = Z_0 \frac{2S_{21}}{(1 - S_{11})(1 - S_{22}) - S_{12}S_{21}}. \tag{15}$$

As shown in Fig. 6, the calculated transfer impedance from the model agrees well with the measurement up to 10 GHz, demonstrating the validity and usefulness of the modeling. As observed in Fig. 6, at resonant frequencies, the transfer impedance reaches 2.5 Ω, which means that substantial SSN coupling occurs at these resonant frequencies. These resonant frequencies are determined by the dimensions, the material, and edge boundary condition of the power/ground plane cavity. In the first resonance mode (1,0), the position of the resonance mode and the peak impedance is well matched, whereas at the higher resonance modes, there are small discrepancies in the peak impedance heights. These discrepancies can be explained from the assumption of small-size cutout. Since the cutout is modeled by equivalent current sources under the assumption of small-size cutout, the model starts to lose its accuracy at high frequencies where the cutout dimensions become more comparable to the wavelength. Another potential reason is the inaccuracy of the dielectric constant and the loss tangent of the FR4 at the higher resonant frequencies. According to [16], [17], the loss tangent increases as frequency increases, which results in greater dielectric loss in the measurement. The test sample has a relatively small size (4 × 4 cm) as shown in Fig. 5, which results in gigahertz range resonant frequencies. If we use a test sample with a larger size cavity, such as (20 × 20 cm), the resonant frequencies are lowered to below the gigahertz range, resulting in much closer agreement of the resonant frequencies and the peak impedance heights. For a more accurate analysis, a full-wave numerical tool is available. We simulated the test structure shown in Fig. 5 using Sigrity PowerSI,[2] and the result was compared with the model, as shown in Fig. 7. The

[2]Sigrity Inc. http://www.sigrity.com

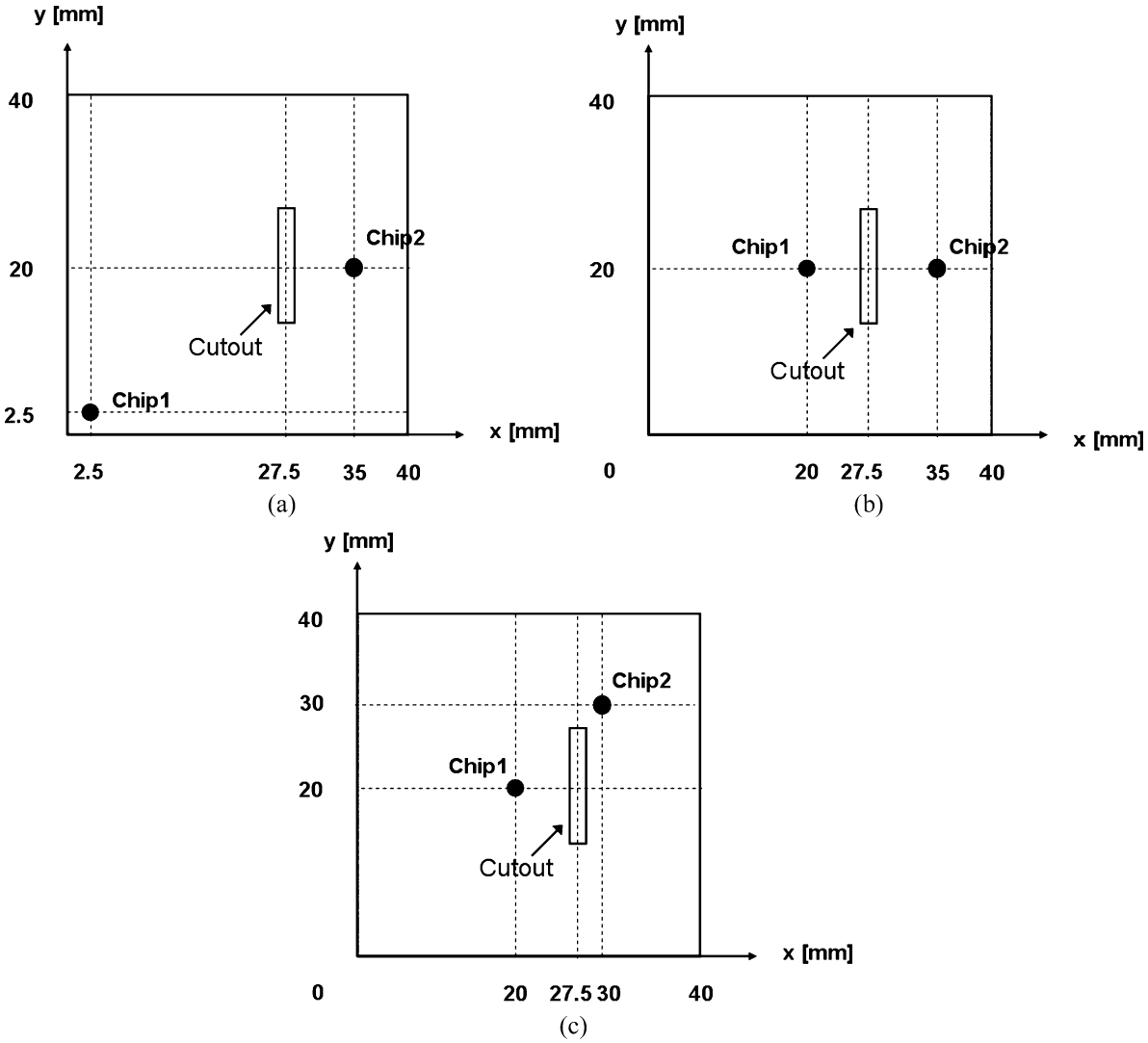

Fig. 9. Configurations of the chip locations for the three test samples. (a) Chip 1 located at (2.5 mm, 2.5 mm) and chip 2 located at (35 mm, 20 mm). (b) Chip 1 located at (20 mm, 20 mm) and chip 2 located at (35 mm, 20 mm). (c) Chip 1 located at (20 mm, 20 mm) and chip 2 located at (30 mm, 30 mm).

numerical tool shows good correlation with the measurement. Solving the problem using the numerical approach required approximately 30 min, whereas the proposed model required less than 30 s, with the same computing resources. Therefore, the model is useful for quick estimates and initial optimization and the numerical tool can be used for fine-tuning.

Consequently, it is necessary to design the cavity carefully so that the resonant frequencies of the cavity are not close to the clock harmonic frequencies of the switching current at port 1. If one of the clock harmonic frequencies is close to these resonant frequencies, significant SSN coupling occurs at the clock harmonic frequency. To predict the position of the resonant frequencies, and the peak height of the transfer impedance at the resonant frequencies, the suggested modeling approach proved to be very useful.

III. Suppression of SSN Coupling Through a Cutout

The coupled noise through a cutout in multilayer packages and PCBs can be suppressed by using any method that minimizes the transfer impedance between the two ports. Such a method includes allocating decoupling capacitors at cavities I and II. These decoupling capacitors reduce the self-impedance at each port as well as the transfer impedance between the ports. However, the conventional decoupling capacitor has a self-resonant frequency below 100 MHz due to its serial inductance. Therefore, above the resonant frequency, the suppression effect of the noise coupling diminishes significantly. However, decoupling capacitors in their inductive region may detune the modal resonance frequencies of the cavities and may diminish the cavity resonance if the method is applied to larger printed circuit boards, where the resonance frequencies may not be orders of magnitude above the series resonance frequencies of the bypass capacitors. This effect needs to be taken into account because decoupling capacitors are commonly used to suppress SSN in the low frequency region, below hundreds of megahertz. An alternative method to suppress the coupled noise between the plane cavities through the cutout is to optimize the locations of the ports and the cutout. Proper location of the ports and the cutout eliminates the resonance peaks at certain resonant frequencies. The basic mechanism of the optimization method is

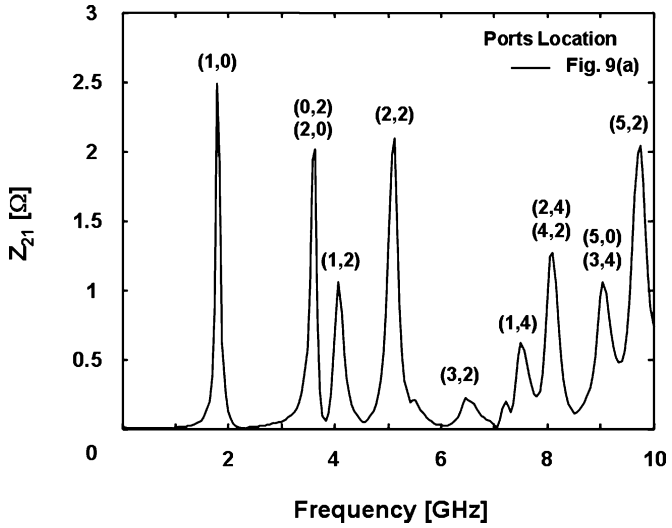

Fig. 10. Simulated transfer impedance for the test sample shown in Fig. 9(a); peaks are annotated with the dominant mode numbers (m, n).

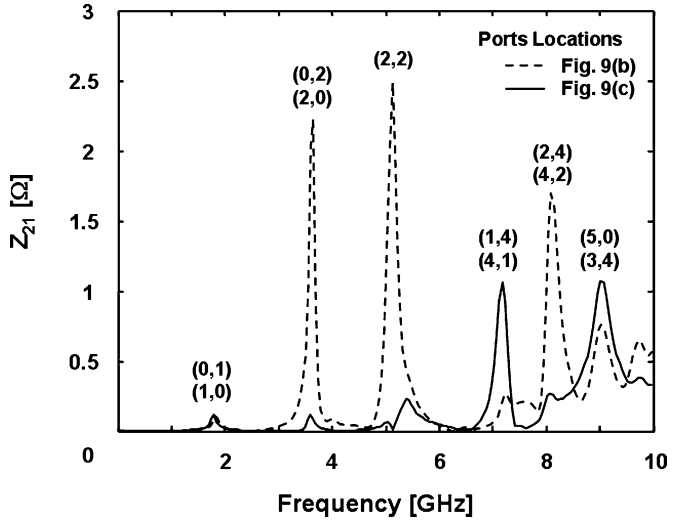

Fig. 11. Simulated transfer impedance for the test samples of Fig. 9(b) and (c). The dotted line is for the case shown in Fig. 9(b); and the solid line is for the case shown in Fig. 9(c). It demonstrates that by repositioning chips 1 and 2, the resonance modes are suppressed significantly.

introduced in [15] and can be understood by examining the cosine and the sine factors in (1) and (6). The formulas for the electric and the magnetic fields in both cavity I and cavity II contain cosine or sine factors because the fields form standing waves in the steady state. When the relationship between the plane cavity dimensions, the port and the cutout locations, and the mode numbers forces the cosine or the sine factor to be zero, the coupled noise is suppressed.

A. Simulation of the Suppression Effect on Test Samples

The simplest way to describe the port optimization method is by examples. Consider a test sample, which has two chips on a multilayer PCB, namely chip 1 and chip 2 as shown in Fig. 8(a). Three layers are used to supply power to the chips where the bottom plane is a voltage plane for chip 1 and the second plane is a voltage plane for the noise-sensitive chip 2 as depicted in Fig. 8(b). The third plane serves as a common ground and has 0.5×10 mm cutout at the coordinate of $x = 27.5$ mm, $y = 20$ mm. FR4 was used as a dielectric material with a permittivity $\varepsilon_r = 4.3$ and thickness $d = 0.1$ mm. Copper metallization was used with a metal thickness $t = 0.018$ mm and conductivity $\sigma = 5.813 \times 10^7$ S/m. Three types of the test samples were studied based on the analytical model described in the previous sections, depending on the chip locations as shown in Fig. 9.

The sequence of Fig. 9(a), (b), and (c) shows the sequential procedure to select the positions of chips 1 and 2, whereas the location and direction of the cutout is already fixed. In the case of Fig. 9(a), chip 1 is located at $x_i = 0$ and $y_i = 0$, which forces $\cos(m\pi x_i/a)\cos(n\pi y_i/b)$ in (1) to be one for all modes. The y-coordinate of the cutout, $y_j = b/2$ forces $\cos(m\pi x_j/a)\sin(n\pi y_j/b)$ in (1b) to be zero for even-numbered n. Therefore, all modal fields except H_x in cavity I can exist with maximum amplitude. In cavity II, the modal impedances for all odd-numbered modes n is suppressed as shown, because the y-coordinate of chip 2 is $b/2$, which forces the $\cos(m\pi x/a)\cos(n\pi y/b)$ factors in (6a) to be zero for odd-numbered n. The simulated transfer impedance, to confirm the suppression effect for the odd-numbered modes n, is shown in Fig. 10.

If chip 1 moves to the center of the plane as shown in Fig. 9(b), all the modal impedances for odd-numbered m or n are suppressed because $x_i = a/2$ and $y_i = b/2$ forces $\cos(m\pi x_i/a)\cos(na\pi y_i/b)$ in (1) to be zero for odd-numbered m or n. The simulated suppression of these odd-numbered m or n is demonstrated by the dotted line in Fig. 11. However, the modal impedances for the even-numbered modes (0, 2), (2, 0), and (2, 2) are still very high, as shown as the dotted line in Fig. 11. The even-numbered modal impedance can be suppressed further by positioning chip 2 at $x = 3d/4$ and $y = 3d/4$ as can be seen in Fig. 9(c). The simulation result is shown by the solid line in Fig. 11. As expected, the coupled noise was successfully suppressed below 7 GHz at the resonant frequencies by simply relocating chips 1 and 2.

The suggested suppression method does not require extra components, or cost, compared with using decoupling capacitance or thin dielectric material with high permittivity. However, the method could not be applied when the optimal placement conflicts with the physical design of the package and PCB. In addition, it is sometimes difficult to use the method, especially when many ports (devices) are mounted on a single package or PCB. In this case, we may simplify the problem by selecting the critical devices. The optimization method assumes that the ports are point-like; however, the method is reasonable for a real chip with several millimeter package dimensions because the amplitude of the standing wave is relatively low around the minimum point. The measurement results shown in the following section demonstrate this because the through-vias made in the test vehicle for measuring ports, which mimic the power and ground vias of a chip, are at a spacing of approximately 1 mm. However, with the ever-increasing chip sizes and operating frequencies, the method is limited by the electrical size of a chip and its package.

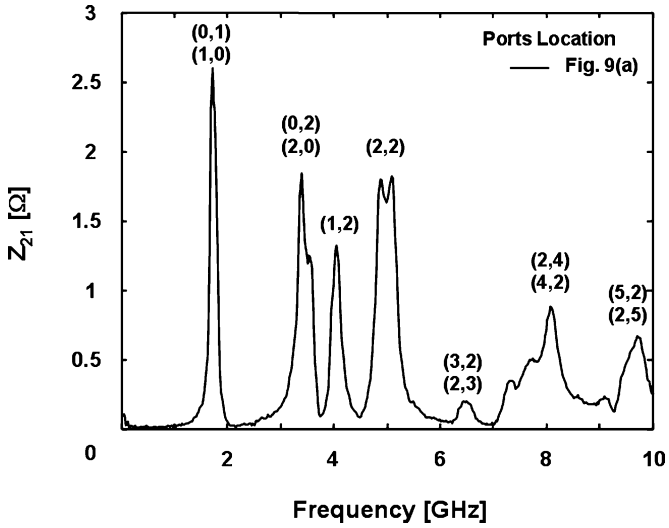

Fig. 12. Measured transfer impedance for the test sample shown in Fig. 9(a).

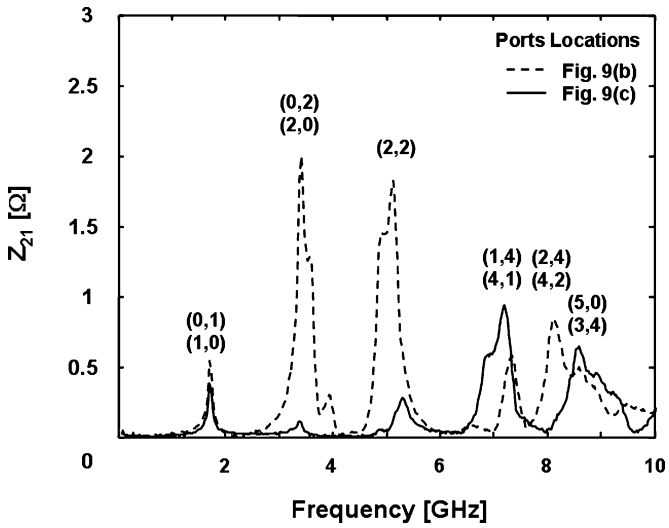

Fig. 13. Measured transfer impedance: the dotted line is for the case shown in Fig. 9(b); and the solid line is for the case shown in Fig. 9(c). Measurements show good agreement with the simulation results shown in Fig. 11, which demonstrates the validity of the port optimization method and also that of the analytical model.

B. Measurement Results of the Suppression Effect on Test Samples

Test samples with the same structures as those shown in Fig. 8 were fabricated to demonstrate the validity of the optimal positioning method described in the previous section. The chips 1 and 2 in Fig. 8 correspond to the ports 1 and 2 in the test samples, respectively. The port locations are the same as those shown in Fig. 9. The cutout size is 0.5×10 mm. Fig. 12 shows the measured transfer impedance for the sample shown in Fig. 9(a). As shown in the simulation results, Fig. 10, all the modal impedances except the odd-numbered n can be still seen. In Fig. 13, the dotted line represents the measured transfer impedance for the sample of Fig. 9(b), and the solid line is for the sample of Fig. 9(c). The measurements show the same trend as the simulation results, as shown in Fig. 11, which demonstrates that the optimal positioning method suppresses the coupling noise between

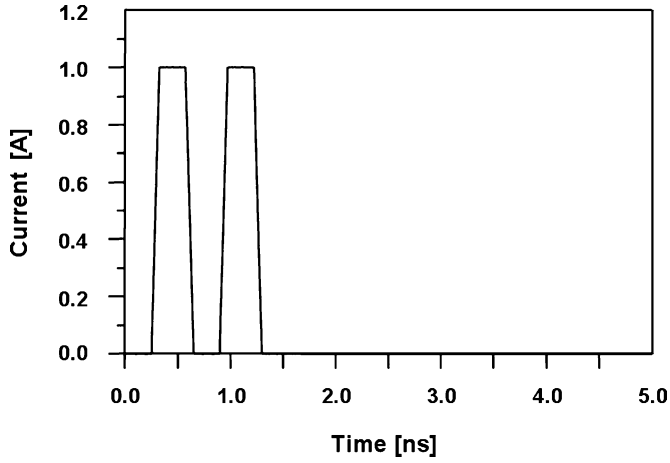

Fig. 14. Assumed current source waveform at port 1 of Fig. 8, for two clock cycles for the time domain noise simulation. Period is 0.65 ns with rise and fall time of 75 ps.

the plane cavities through the cutout and the analytical model captures the coupling effect. Measurement confirmed that all the modal impedances for odd-numbered m or n are suppressed by repositioning chip 1 and that the even-numbered modal impedances are suppressed further by the positioning of chip 2. We conclude that the noise coupling between plane cavities through the cutout can be reasonably suppressed by simply placing the chips and the cutouts at the proper locations. The suggested analytical model can be used to determine the optimal locations of the chips or the cutouts in multilayer packages and PCBs.

C. Time Domain Analysis of Suppression Effect on Test Samples

In this section, the effect of the power/ground noise coupling between plane cavities through the cutout is discussed in the time domain. Consider the test sample shown in Fig. 8 and assume that chip 1 has a 1 A current source. The current source has a 0.65-ns period with rise and fall times of 75 ps, and switches for two clock cycles as shown in Fig. 14. Then, the current source generates switching noise in the lowest plane cavity I and the noise is coupled into the neighboring plane cavity II through the cutout. The coupled noise can affect the signal integrity of chip 2 as well as the signal integrity of chip 1.

Fig. 15(a) shows the time domain coupled noise waveform when chip 1 is located at $x = 2.5$ mm, $y = 2.5$ mm, and chip 2 is at $x = 35$ mm, $y = 20$ mm as shown in Fig. 9(a) with the source current as defined in Fig. 14. The coupled noise waveform was obtained using Agilent ADS from the convolution of the input signal and the impulse response of the two-port network. The impulse response was generated from the inverse Fourier transform of the measured S-parameters of the test sample. As can be seen from Fig. 15(a), the maximum coupled noise for the two switching cycles is ± 200 mV. Noise voltage fluctuation lasts for more than 5 ns due to the high quality factor of the cavity structure, even after the current source has stopped the switching. Because of this long-lasting noise fluctuation, the coupled noise can be accumulated every time the current switches, which means that higher coupled noise is expected

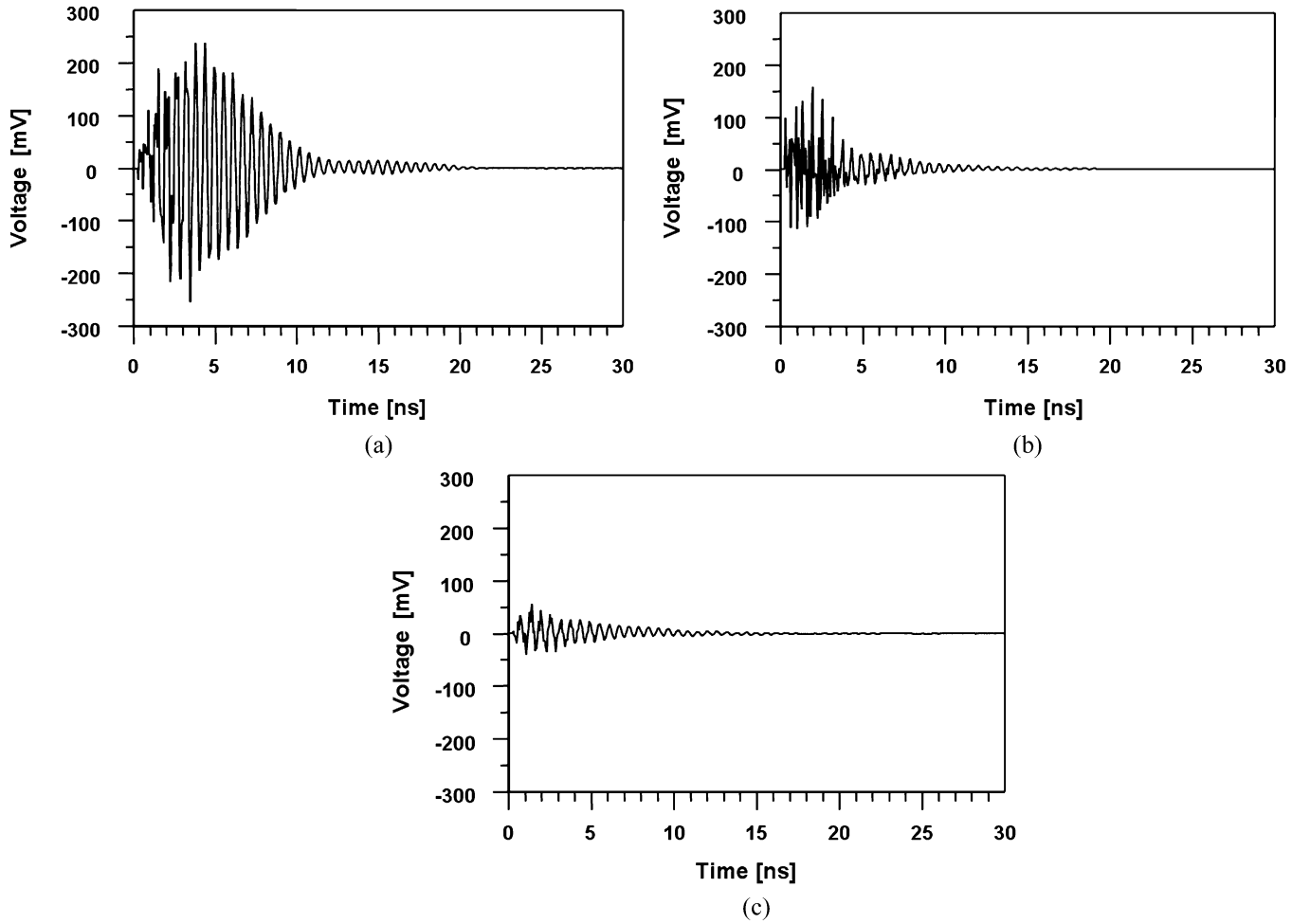

Fig. 15. Time domain coupled noise waveform at port 2, between P1 and ground plane at the chip 2 location due to the switching current of the chip 1 shown in Fig. 14, which is supplied by P2 and ground plane. (a) Coupled noise waveform in the case of Fig. 9(a). (b) Coupled noise waveform in the case of Fig. 9(b). (c) Coupled noise waveform in the case of Fig. 9(c).

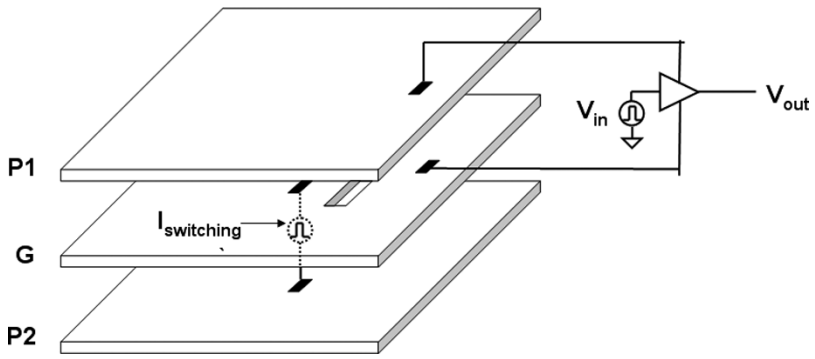

Fig. 16. Test sample for the simulation of the signal integrity of the chip 2. $I_{switching}$ represents the switching current of chip 1 at port 1 in Fig. 8, and the I/O buffer in chip 2 is powered by the P1 and G plane pair that contains the coupled noise through the cutout.

for more switching cycles. Moreover, the coupled noise is compounded by the increased magnitude of the switching current. Therefore, the coupled noise through the cutout cannot be ignored, bearing in mind the tendency for rapidly increasing currents and reduced noise margins. To confirm the suppression effect of the coupled noise through the cutout by repositioning chips 1 and 2, time domain transient coupled noise responses for the case of Fig. 9(b) and (c) have been simulated and the reduced coupled noises are shown in Figs. 15 (b) and (c), respectively. As predicted in the frequency domain simulation and measurement, the optimal positioning method is effective when applied in time domain analysis. The maximum coupled noise for the two switching cycles is ± 40 mV for the case of Fig. 9(c), which is only 20% of that in the case of Fig. 9(a). Once the specification of the voltage fluctuation $(V_{\max})$ is defined, for example, as five percent or ten percent of the supply voltage, we can determine the maximum allowable power-ground impedance from the ratio of switching current profile and $V_{\max}$. We can de-

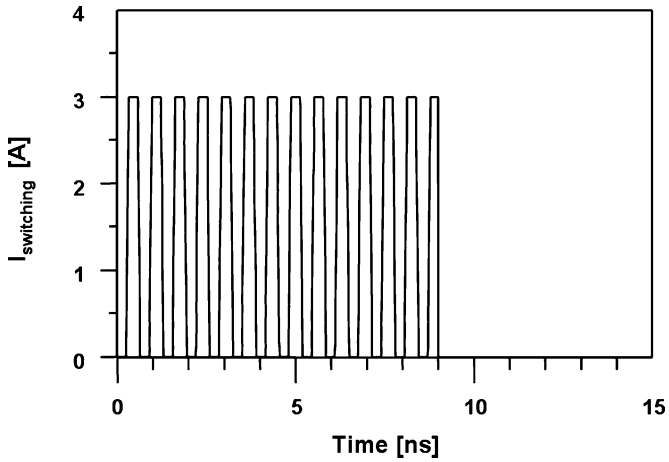

Fig. 17. Assumed current waveform of the switching current at port 1.

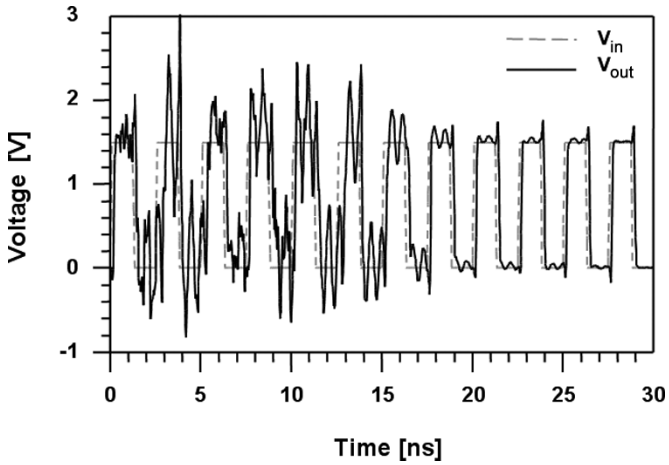

Fig. 18. Input and output voltage waveform of the buffer for the chip 2 at port 2, with the chips located as shown in Fig. 9(a).

fine a keep-out zone for placement to meet the power-ground impedance specification by calculating the impedance profile in terms of chip locations using the model.

The coupled voltage fluctuations shown in Fig. 15 through the cutout directly affect the signal integrity of chip 2 in Fig. 8. Consider also the case where the output buffer in chip 2 is powered by P1 and the ground plane pair, while chip 1 switches currents for many cycles, not two cycles as in the previous analysis. The plane configuration and the switching current waveforms are shown in Fig. 16 and Fig. 17, respectively. The output buffer in chip 2 simply consists of two cascaded CMOS inverters. The assumed waveform of the switching current $(\mathrm{I_{switching}})$ at port 1 is shown in Fig. 17. The amplitude of the switched current is 3 A, and it switches for fourteen clock cycles. Fig. 18 shows the input and the output voltage waveforms of the buffer for the chip 2 at port 2 for the case of the chip locations as shown in Fig. 9(a). The output signal shows substantial overshoot and ringing due to the coupled power noise through the cutout. However, the signal output noise is successfully reduced by placing the chips at the locations of Fig. 9(c), as shown in Fig. 19. The power/ground noise gradually decreases depending on the Q factor of the cavity and the switching cycles, as shown in Fig. 15; thus, the signal-to-noise ratio gradually increases

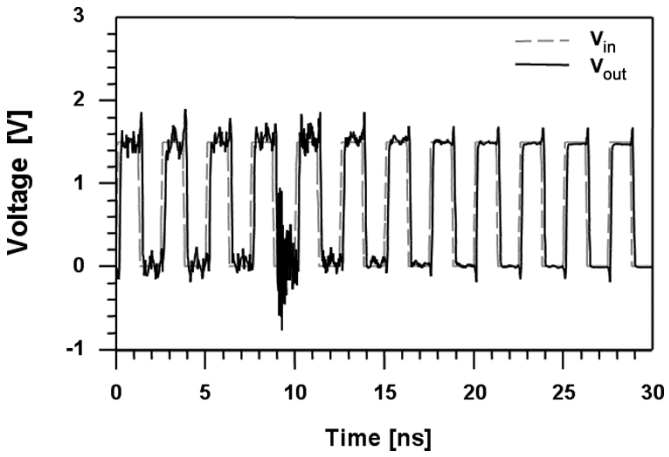

Fig. 19. Input and output voltage waveforms of the buffer for chip 2 at port 2, with the chips located as shown in Fig. 9(c).

in Fig. 18. From the time domain analysis, we conclude that the power/ground noise coupling through the cutout can significantly degrade signal integrity and it should be managed. It was successfully demonstrated that optimal positioning is one of the reasonable solutions.

IV. Conclusion

In this paper, we describe an analytical modeling approach of SSN coupling phenomena through the cutout in multilayer power/ground plane structures. The model shows good correlation with measurements up to 10 GHz. Based on the analysis and the experiment, it is found that substantial coupled noise is transmitted to the adjacent plane cavities through the cutout. The quantity of the coupled noise depends on the size, shape, and locations of the cutout as well as the locations of the ports. By examining the analytical formulation of the model, we have developed a better understanding of the coupled noise through the cutout. According to the analytical model, the transfer impedance is a combination of an infinite number of modal impedances, while each modal impedance consist of sinusoidal functions that exhibit peak and null patterns across the plane surface. It suggests that we can choose the optimal positions of the ports and the cutouts to minimize the coupled noise through the cutouts based on the analytical model. The suppression method of the coupled noise through the cutout was successfully demonstrated by both frequency and time domain analysis and measurement. The suppression was achieved by the suggested optimal positioning method. Once the coupled noise is minimized, we could ignore it and avoid the complex modeling and longer simulation time required for evaluation of a high-speed digital or mixed-signal system.

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