A HIGH PERFORMANCE LOW POWER DYNAMIC PLA WITH CONDITIONAL EVALUATION SCHEME

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ABSTRACT

This paper proposes a high performance and low power dynamic CMOS PLA that minimizes active power consumption. The proposed PLA uses a conditional evaluation scheme to reduce short circuit power consumption during the evaluation phase. The proposed PLA reduces delay by 13.8%, dynamic power by 46%, and total power delay product (PDP) by 53.4% compared to the conventional clock-delayed PLA in a 0.25um CMOS process technology.

1. INTRODUCTION

PLA has been widely used as an important building block of a control logic in a microprocessor and functional logic in any other VLSI application. In recent VLSI logic design, PLA is still attractive to design high performance digital circuits due to its simplicity and regularity [1]. The regular structure of PLA implies that the implemented area and the operation timing of the designed circuit can be easily predictable and reconfigurable. Therefore, the design efforts to implement the functional unit of the control logic are quite smaller than other methods.

The low power design is essential in modern digital circuits to extend the operation lifetime of battery-supplied mobile systems. At the same time, the operation speed should be maintained to achieve low power and high performance digital circuit. A couple of PLA designs are proposed to increase the operation speed and to reduce the active power consumption [2],[3]. In Blair's PLA, the power consumption of PLA can be reduced by using a pre-discharge scheme in AND-plane [2]. Wang's PLA reduces not only power consumption but also operating speed by using a charge-sharing technique and a pseudo-footless dynamic circuit scheme [3]. However, the power consumption of Blair's PLA is still large due to the short circuit power consumption during evaluation phase. In addition, the design overhead on Wang's PLA exists to implement accurate capacitor for the charge-sharing technique.

To solve these problems, we propose a new high performance and low power dynamic PLA design which uses a conditional evaluation scheme. The proposed conditional evaluation scheme performs the evaluation of AND-plane conditionally according to its output value. Therefore, the short circuit power consumption is minimized and no accurate capacitor is needed for the charge-sharing scheme.

This paper is organized as follows. Section 2 describes the conventional PLA designs and their logic problems in detail. Section 3 proposes a new high speed low power dynamic CMOS PLA. The operation and design consideration will be described. In section 4, the simulation results and the comparisons are shown. This paper is concluded in section 5.

2. THE CONVENTIONAL PLA DESIGNS

Figure 1(a) shows the critical path of conventional clock-delayed CMOS PLA [4]. This design is composed of the two NOR type dynamic logic connected in cascade. The first NOR-plane performs the AND operation and the second NOR-plane performs the OR operation of the Boolean function. Since the output evaluation is performed by NOR type dynamic logic, the evaluation speed at each NOR-plane is relatively fast. However, the shortcoming of this scheme is the intrinsic race problem. The output of the AND-plane that has not finished the evaluation yet may wrongly turn on the OR-plane. Consequently, the clock supplied to the OR-plane should be delayed enough to eliminate the race problem until the evaluation of AND-plane finishes. Moreover, the foot-NMOS of the each NOR-plane that produces large parasitic capacitance, Cp, increases evaluation delay.

Figure 1(b) shows the critical path of Blair's PLA design. In this design, the foot-NMOS's of both NOR-planes are eliminated and the AND-plane evaluates its output by using pre-discharge mechanism. When the clock is HIGH the AND-plane pre-discharges node 'a', and the OR-plane pre-charged node 'b' to VDD since node 'c' is GND. When the clock changes to LOW, the AND-plane evaluates HIGH if the input is LOW or evaluates LOW if the input is HIGH.

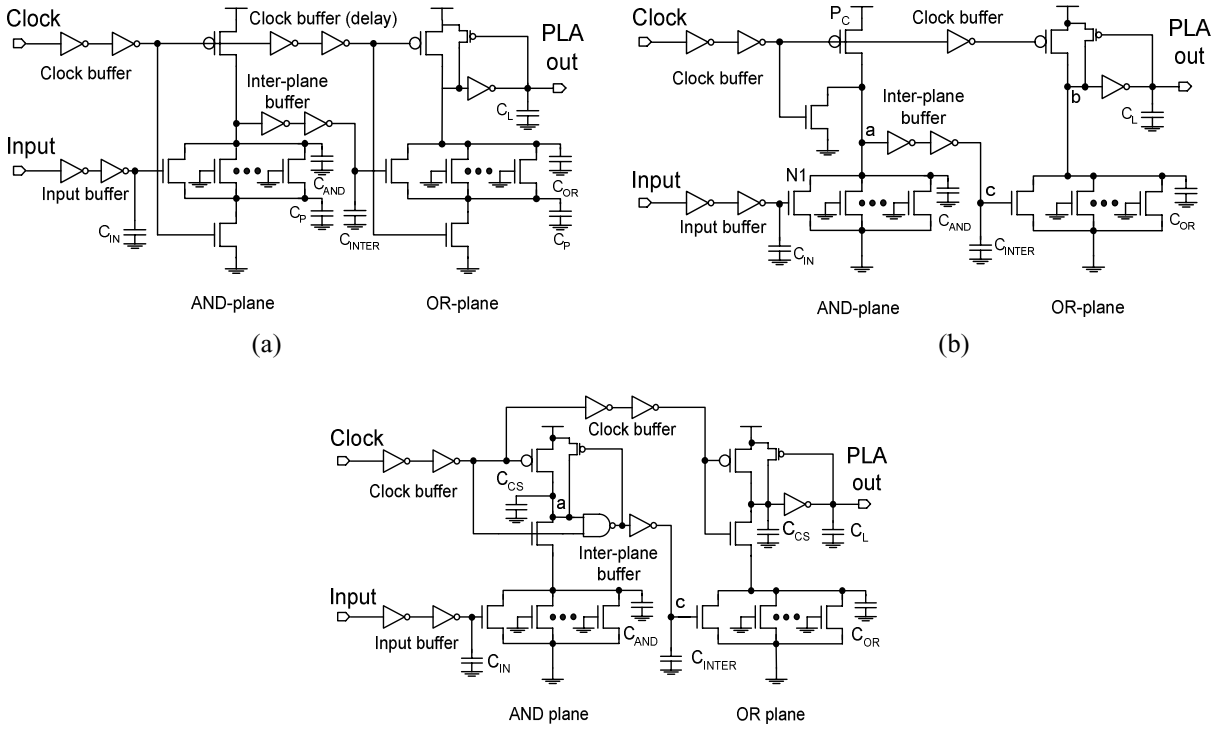


Figure 1: The critical path of conventional PLA designs,
(a) Convention clock-delayed PLA, (b) Blair's PLA, (c) Wang's PLA

Of course, the current driving capability of the single pull down NMOS 'N1' is designed stronger than the single pre-charge PMOS 'P_C' for correct operation. According to the voltage of node 'c', the OR-plane evaluates and the output is determined. However, the short circuit power consumption exists during the evaluation phase when the input is HIGH. Because each plane is designed by NOR type dynamic logic, the probability of the pull down NMOS to be turned ON is high. Therefore, the power consumption due to short circuit current is significant.

Figure 1(c) shows the critical path of Wang's PLA design. This design also eliminates the foot-NMOS to reduce parasitic capacitance. The charge-sharing scheme is used to reuse the conserved charge at the next evaluation cycle. Thus, low power and high performance operation is enabled. When the clock is LOW, the node 'a' is pre-charged to VDD. If the clock changes to HIGH and the input at the AND-plane is LOW, the charge at the C_{CS} is shared with the C_{AND} and the PMOS keeper pulls up the rest of voltage. The charge-sharing operation in OR-plane is the same. Basically, this scheme uses the conventional precharge-and-evaluation scheme. However, the NAND gate make the voltage level of node 'c' maintain LOW for most of input to PLA in spite of NOR type dynamic logic. However, the problem of this scheme is the high design effort for the implementation of accurate capacitor to enable the charge-sharing mechanism at each NOR logic. And a glitch exist at node 'c' during evaluation.

3. THE PROPOSED HIGH SPEED LOW POWER CMOS PLA DESIGN

Figure 2 shows the critical path of the proposed high performance and low power CMOS PLA with the conditional evaluation scheme. Its configuration is similar to the Blair's PLA except for the conditional evaluation circuit which is composed of the inverter and NOR gate. Since these additional circuits are implemented with minimum size transistor, the delay overhead on the critical path is negligible. In fact, this conditional evaluation circuit minimizes the active power consumption due to the elimination of short circuit power consumption. Only one of the pull down NMOS is connected to the input node and other inputs are GND to configure the worst case pull down condition.

The figure 3 shows the abstract timing diagram of the conditional evaluation scheme in the proposed PLA. The operation when the input is LOW is as follows. While the clock is HIGH, the node 'a' is pre-discharged to GND. And the node 'b' is pre-charged to VDD. This is the 'pre-discharge phase'. The input value does not affect the output node even if the foot NMOS does not exist due to the pre-discharge mechanism. When the clock changes to LOW, the circuit enters the evaluation phase. Since the input is LOW, all of the pull-down NMOS in the AND-plane are off. Then the PMOS pulls up the node 'a' to VDD and the output of the PLA goes HIGH. During the

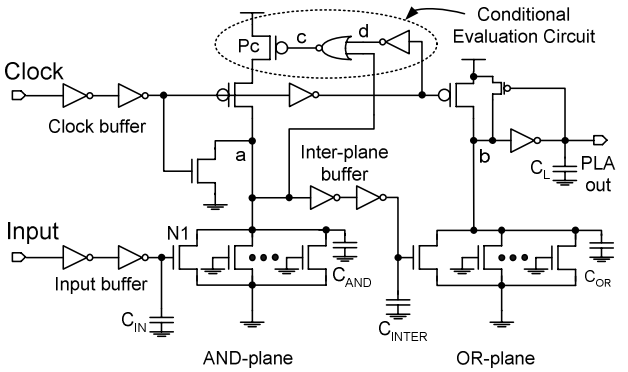


Figure 2: The critical path of the proposed high speed low power dynamic CMOS PLA

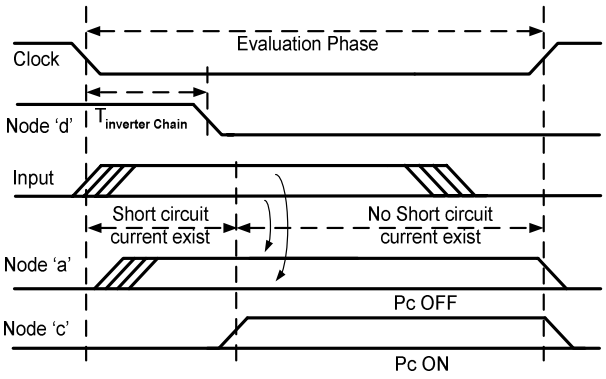
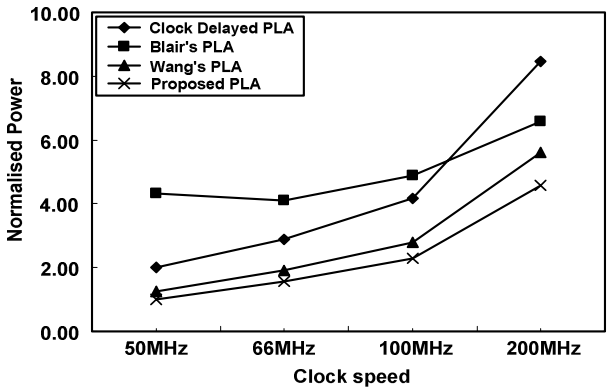


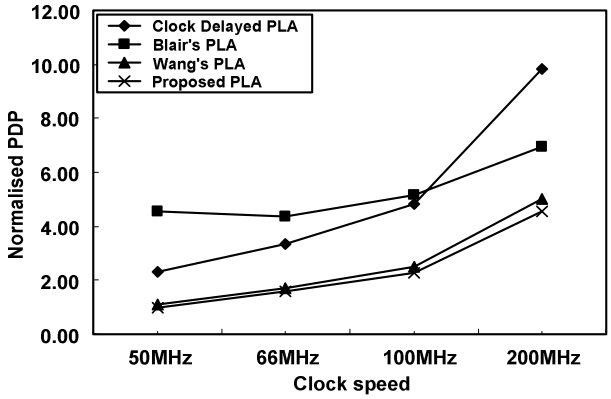
Figure 3: The timing diagram of the proposed PLA

evaluation when the input is LOW, the short circuit power consumption is not significant. However, this operation can rarely happen because all the input connected to the AND-plane has to be LOW.

The short circuit power consumption exists during the evaluation phase when the input is HIGH and this is biggest weak points of the Blair's PLA. However, the proposed conditional evaluation scheme solves this problem and reduces the short circuit power consumption dramatically. At the starting point of evaluation phase the PMOS has to be fully turned ON to evaluate the PLA output. However, during the rest of evaluation, it is not required for the PMOS to be turned on because the evaluation of the output has finished and only short circuit power is consumed for this interval. Therefore, the conditional evaluation circuit cuts off the path between VDD and node 'a' to eliminate the short circuit power. This is the key idea of proposed PLA. Its operation is as follows. When the clock changes to LOW and if the input is HIGH, pull down NMOS 'N1' is turned ON and the node 'a' remains LOW. During the propagation time of clock delay chain, the NOR gate output of the conditional evaluation circuit is LOW and maintains the path between VDD and node 'a' to evaluate the PLA. After the propagation time of clock delay chain the output of NOR gate remains LOW if the node 'a' is HIGH or changes to



(a)



(b)

Figure 4: The Power and PDP comparisons for the Proposed PLA to previous approach

HIGH if the node 'a' is LOW. By using this mechanism, the short circuit power is consumed during only short propagation time of clock delay chain. Since the proposed conditional evaluation circuit consists of minimum sized MOS transistor, the additional delay overhead for the critical path is minimal.

4. SIMULATION RESULTS AND COMPARISONS

We compared the performance and the power consumption of the proposed PLA with the conventional clock-delayed PLA, Blair's PLA, and Wang's PLA. These PLAs are simulated at the 50MHz, 100MHz, 150MHz, and 200MHz clock frequency using a 0.25um CMOS technology with 2.5V supply voltage.

Figure 4(a) and (b) show the normalized power and the normalized PDP at the critical path of the proposed PLA versus various clock frequency condition. The power consumption and the PDP curves of the conventional clock-delayed PLA, Blair's PLA, and Wang's PLA are also plotted in each graph. The active power consumption is defined as the average power consumption in the each

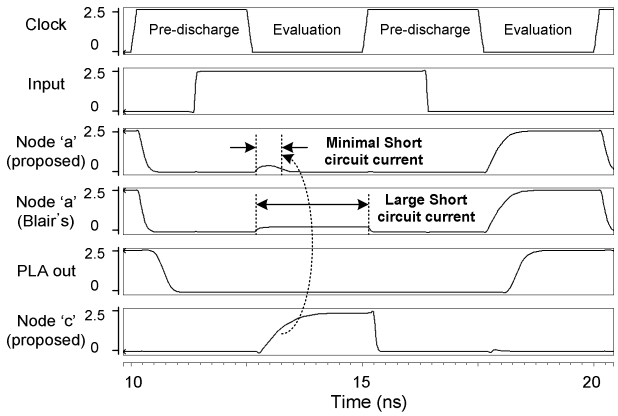


Figure 5: The simulated waveforms of the proposed PLA and Blair's PLA @ 200MHz Clock

clock frequency. And 50 % of input probability condition are assumed. In other words, input HIGH and input LOW occur alternately at each clock cycle to the input node. And other NMOS inputs of the AND-plane is GND for the worst case configuration. Actually, the input probability is higher than this due to the NOR type dynamic logic configuration of PLA designs. As shown in each figure, the power consumption and the PDP of the proposed PLA is smallest than any other designs. Moreover, the power consumption decreases linearly as the clock frequency decreases whereas the power consumption of Blair's PLA increases because the short circuit power consumption increases.

Figure 5 shows the simulated waveforms of the proposed PLA and Blair's PLA at 200MHz clock frequency. The dashed line shows that the voltage of the node 'a' for the proposed PLA and Blair's PLA. As shown in dashed line waveform, the proposed PLA consumes the short circuit power during on short interval whereas the Blair's PLA consumes the short circuit power during the whole evaluation phase. This is the reason why the proposed PLA consumed less active power at low clock frequency condition.

Table 1 shows the overall delay, power and PDP comparisons among the proposed PLA, conventional clock-delayed PLA, Blair's PLA, and Wang's PLA. The proposed PLA shows somewhat long operation delay time when it compared to Wang's PLA. However, the reduction in active power consumption overcomes this shortcoming of the proposed PLA. The proposed PLA reduces the active power consumption by 46% compared to the conventional clock-delayed PLA, by 30.5% compared to the Blair's PLA, and by 18.3% compared to the Wang's PLA at 200MHz clock frequency. Moreover, the proposed PLA reduces power consumption by 76.8% compared to the Blair's PLA at 50MHz clock frequency. Consequently, the overall PDP of the proposed PLA is smallest than any other PLA designs. The proposed PLA reduces PDP by 53.4%, 29.7% and 8.5% when it compared to the conventional clock-delayed PLA, Blair's PLA, and Wang's PLA respectively at 200MHz clock frequency.

Table 1: Overall power, delay and PDP at 200MHz Clock

PLA type	Power (mW)	Delay (ns)	PDP(pJ)
Clock-delayed PLA	0.334	1.067	0.356
Blair's PLA	0.259	0.912	0.236
Wang's PLA	0.221	0.825	0.182
Proposed PLA	0.180	0.926	0.166

Although the charge-sharing technique enhances the operation speed in Wang's PLA, it has design overhead to implement accurate charge-sharing capacitor at each dynamic node of AND-plane and OR-plane. If the charge-sharing capacitor is not implemented precisely, the wrong operation can be resulted in Wang's PLA. On the other hand, the proposed PLA is free from the implementation of the accurate charge-sharing capacitor.

5. CONCLUSION

A high performance and low power dynamic PLA with a conditional evaluation scheme is proposed. The proposed PLA not only reduces the power consumption but also eliminates the design overhead to implement the accurate charge-sharing capacitor. The proposed PLA reduces active power consumption using the conditional evaluation scheme by 46%, 30.5%, and 18.3% compared to the conventional clock-delayed PLA, Blair's PLA, and Wang's PLA respectively at 200MHz clock frequency. And the overall PDP is reduce by 53.4%, 29.7%, and 8.5% at the same clock frequency in a 0.25um CMOS process technology.

6. ACKNOWLEDGEMENTS

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7. REFERENCES

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