A LOW POWER CHARGE SHARING ROM USING DUMMY BIT LINES

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ABSTRACT

This paper proposes a shared-capacitor charge-sharing ROM (SCCS-ROM). The SCCS-ROM reduces the swing voltage using the charge-sharing technique of the charge-sharing ROM (CS-ROM) [4]. Although the CS-ROM needs three small capacitors per output, the SCCS-ROM shares the capacitors so that it needs only three capacitors. The SCCS-ROM implements the capacitors using dummy bit lines. This not only increases noise immunity but also reduces power. The simulation results show that the SCCS-ROM reduces 8.4% power compared to the CS-ROM.

1. INTRODUCTION

Due to the high demands on portable products, power consumption becomes a major concern in VLSI chip designs, especially for embedded memories. ROM (Read Only Memory) consumes lots of power because it is one of the busiest parts in chips and its size continues to be larger. The ROM core dissipates most of the power because bit lines and word lines have large capacitance. The bit lines dissipate most power because bit lines are high capacitive and many bit lines are selected for each access. The word lines also consume a large amount of power. Therefore, many techniques are proposed to reduce the power dissipation in these high capacitive lines of ROMs.

Some techniques focused to reduce the power consumption by decreasing the capacitances of bit lines and word lines [1]. They are achieved by the hierarchical word line, the selective precharge, and the minimization of non-zero terms. These techniques can save the power without losing performance.

Other techniques focused to reduce the power consumption by lowering the swing voltage of bit lines [1]-[4]. These techniques are independent of the ROM data and the power saving is in proportion to the swing voltage. Therefore, the low swing techniques can save lots of power. Recently, a charge-sharing ROM (CS-ROM) using charge-sharing bit line is proposed [4]. The CS-ROM saves lots of power but it requires small capacitors to reduce the swing voltage in bit lines. However, it is hard to implement the small capacitors precisely. The small capacitors decrease noise margin. To increase the noise margin, larger capacitors are required than we expect.

In this paper, a shared-capacitor charge-sharing ROM (SCCS-ROM) is proposed. The operation of the SCCS-ROM is exactly the same as the CS-ROM. However, the SCCS-ROM overcomes the problems of the CS-ROM by replacing the small capacitors with three large capacitors. In the SCCS-ROM, the capacitors are implemented precisely using dummy bit lines. This not only increases noise immunity but also reduces power.

2. CHARGE SHARING ROM

2.1 Charge-Sharing Bit Line

Figure 1. Concept of conventional charge-sharing bit line

Fig. 1 shows the concept of the conventional charge-sharing bit line (CSBL) [4]. The CSBL reduces the swing voltage of bit lines using three capacitors C_{CS} , C_H , and C_L . When the capacitance of the bit line is C_{BL} , the swing voltage becomes very small by the charge-sharing among C_{BL} , C_{CS} , and C_H .

All switches in Fig. 1 represent transistors and the numbers on the switches show the timing sequences when the transistors are turned on. A transistor connected to V_{DD} is a PMOS transistor and the other transistors are NMOS transistors. The operation of the CSBL is as follows. (1) C_{CS} and C_H are charged to V_{DD} and $V_{DD}-V_t$ respectively and C_L is discharged to ground. The total charge stored in C_{CS} and C_H is $C_{CS} \times V_{DD} + C_H \times (V_{DD} - V_t)$. The voltage of the bit line is at ground. (2) A bit line select transistor is turned on. C_{BL} , C_{CS} , and C_H are connected to share their charges. Their voltages become V_{CS} which is made by dividing the total charge stored in the capacitors by the total capacitance of the capacitors. The CSBL consumes P_{CSBL} where f is the switching frequency.

$$V_{CS} = \{C_{CS} \times V_{DD} + C_H \times (V_{DD} - V_t)\} / (C_{BL} + C_{CS} + C_H)$$

$$P_{CSBL} = f \times (C_{BL} + C_{CS} + C_H) \times V_{CS} \times V_{DD}$$

(3) A word line is selected. If ROM data is '1', the voltage of the bit line remains V_{CS} . If not, the voltage becomes ground. As a result, the voltage of C_{CS} becomes V_{CS} or ground according to the ROM data. Therefore, a sense amplifier is needed to detect the ROM data. Also, a reference voltage V_{REF} is required for the sense

amplifier. V_{REF} is made by the two small capacitors C_H and C_L . The voltages of C_H and C_L are V_{CS} and ground respectively. When C_H and C_L are connected, their voltages become $V_{CS}/2$. Therefore, V_{REF} becomes $V_{CS}/2$.

2.2 Charge-Sharing ROM

Figure 2. Concept of conventional charge-sharing bit line

Fig. 2 shows the charge-sharing ROM (CS-ROM) using the CSBL. The CS-ROM has M groups. Each group contains N bit lines and three small capacitors C_{CS} , C_H , and C_L . A bit line is selected among the N bit lines. The CS-ROM reduces the swing voltage in the selected bit line using the charge-sharing between C_{BL} and C_{CS} . The swing voltage is controlled by sizing C_{CS} . A small capacitor is used for C_{CS} to reduce power consumption. C_{CS} is much smaller than C_{BL} . Therefore, the power dissipation is significantly reduced.

The voltage of the selected bit line becomes V_{CS} after the charge-sharing between C_{BL} and C_{CS} . If ROM data is '1', the voltage remains V_{CS} . If not, the voltage becomes ground. Two small capacitors C_H and C_L are used to make the reference voltage V_{REF} . The voltages of C_H and C_L are V_{CS} and ground respectively. C_H and C_L are connected to make V_{REF} which is $V_{CS}/2$. The sense amplifier obtains data by comparing the voltage of the selected bit line and V_{REF} .

The CS-ROM requires two signals S0 and S1 except for precharge and sense amplifier enable (SAE). S0 and S1 are used for the charge-sharing operation.

We have to carefully select the size of C_{CS} . If the sense amplifier can detect small voltage difference, V_{CS} can be reduced to very small voltage to reduce power consumption. Therefore, C_{CS} becomes small. However, it is hard to implement the small capacitor precisely. Moreover, the size of C_{CS} varies due to interconnections and layout mismatches.

C_H and C_L must have exactly the same capacitance to increase noise margin. C_H and C_L are chosen in the range where V_{REF} can overcome external and internal noises and layout mismatches. However, it is hard to realize the exact size of C_H and C_L because their sizes are very small.

To make the input voltages of the sense amplifier robust from noises and layout mismatches, we can increase the sizes of C_{CS} , C_H , and C_L . Although the larger capacitors increase the noise margin, they cause more power dissipation by increasing swing voltage in the bit line.

3. PROPOSED CHARGE-SHARING ROM

3.1 Shared-Capacitor Charge-Sharing Bit Line

Figure 3. Concept of shared-capacitor charge-sharing bit line

Fig. 3 shows the shared-capacitor charge-sharing bit line (SCCSBL). The operation of the SCCSBL is exactly the same as the conventional CSBL. Although the CSBL uses three capacitors C_{CS} , C_H , and C_L per group, the SCCSBL shares the capacitors C_{CS} , C_H , and C_L for the charge-sharing operation. When the number of groups is M , the number of the capacitors is reduced to $1/M$. Moreover, the SCCSBL eliminates the control signals for the charge-sharing operation in each group. The control signals are only used for the shared capacitors.

All switches in Fig. 3 represent transistors and the numbers on the switches show the timing sequences when the transistors are turned on. Two transistors connected to V_{DD} are PMOS transistors and the other transistors are NMOS transistors. The operation of the SCCSBL is as follows. (1) C_{CS} and C_H are charged to V_{DD} and C_L is discharged to ground. The total charge stored in C_{CS} and C_H is $(C_{CS}+C_H) \times V_{DD}$. The voltage in the selected bit line is at ground. (2) A bit line is selected per group. M bit lines are selected in M groups. When the capacitance of the bit line is C_{BL} , the total capacitance of M bit lines becomes $M \times C_{BL}$. The bit lines are connected to C_{CS} and C_H for the charge sharing. Their voltages become V_{CS} . Each bit line in the SCCSBL consumes P_{SCCSBL} where f is the switching frequency.

$$V_{CS} = (C_{CS}+C_H) \times V_{DD} / (M \times C_{BL} + C_{CS} + C_H)$$

$$P_{SCCSBL} = f \times C_{BL} \times V_{CS} \times V_{DD}$$

(3) After all bit lines are disconnected from C_{CS} and C_H , a word line is selected. The voltages of the bit lines remain V_{CS} or become ground according to the ROM data. The voltages of C_H and C_L are V_{CS} and ground respectively. C_H and C_L are connected to make the reference voltage V_{REF} which is $V_{CS}/2$.

3.2 Shared-Capacitor Charge-Sharing ROM

Fig. 4 shows the shared-capacitor charge-sharing ROM (SCCS-ROM) using the SCCSBL. The SCCS-ROM uses dummy bit lines to implement the capacitors C_{CS} , C_H , and C_L . The SCCS-ROM

uses the diffusion programming ROM as shown in Fig. 7(b). Therefore, all bit lines have almost the same capacitance C_{BL} . The dummy bit lines also have C_{BL} . C_{CS} consists of $K-1$ dummy bit lines. C_H and C_L consist of only a dummy bit line. Thus, the size of C_{CS} becomes $(K-1) \times C_{BL}$. Also, the sizes of C_H and C_L are C_{BL} .

$$C_{CS} = (K-1) \times C_{BL}$$

$$C_H = C_{BL}$$

$$C_L = C_{BL}$$

When the SCCS-ROM has M groups, the charge-sharing voltage V_{CS} becomes independent of the size of C_{BL} . V_{CS} is easily adjusted by changing K . We do not need to consider the sizes of C_{BL} , C_{CS} , C_H , and C_L .

$$\begin{aligned} V_{CS} &= (C_{CS} + C_H) \times V_{DD} / (M \times C_{BL} + C_{CS} + C_H) \\ &= ((K-1) \times C_{BL} + C_{BL}) \times V_{DD} / (M \times C_{BL} + (K-1) \times C_{BL} + C_{BL}) \\ &= K \times C_{BL} \times V_{DD} / (M+K) \times C_{BL} \\ &= K / (M+K) \times V_{DD} \end{aligned}$$

Fig. 5 shows the detail structures of the SCCS-ROM. The SCCS-ROM has M groups and each group contains N bit lines. $K+1$ dummy bit lines are added to the original ROM core. $K-1$ dummy bit lines are used for C_{CS} . The other two dummy bit lines are used for C_H and C_L . The SCCS-ROM operates with four time sequences (precharge, charge sharing, evaluation, and sense amplifier enable) and four control signals (PCHG, CS, EVAL, and SAE).

The lines connecting all M groups increase the sizes of C_{CS} , C_H , and C_L because they have the capacitances due to the metal lines and the connected transistors. Also, they increase V_{CS} slightly. But, this does not affect the operation. If the additional capacitances are not small, they have to be considered. However, the additional capacitances are smaller than C_{BL} . Moreover, they are much smaller than C_{CS} which is $(K-1) \times C_{BL}$.

The sense amplifier in Fig. 6 has four inputs. Two inputs are connected to the selected bit line and the other two inputs are connected to V_H and V_L . If the sense amplifier with two inputs in Fig. 2 is used, C_H and C_L become the different size due to the gate capacitance of PMOS transistor of the sense amplifier. But, if the sense amplifier with four inputs is used, C_H and C_L become exactly the same. This improves noise margin.

Fig. 7(a) and 7(b) show the layouts of the dummy bit lines and bit lines respectively. The capacitance of the bit line depends on the programmed data. When all data connected to the bit line are '0', the bit line has the maximum capacitance. To guarantee that the swing voltage in the bit line is larger than V_{CS} , the dummy bit line has the maximum capacitance. All data connected to the dummy lines are '0'. The transistors in the dummy bit line are not turned on because the dummy bit lines are used for the capacitors C_{CS} , C_H , and C_L . The gates of the transistors are connected to ground.

The SCCS-ROM is smaller than the CS-ROM because the SCCS-ROM shares the capacitors C_{CS} , C_H , and C_L and the capacitors are compactly implemented using dummy bit lines. Also, the SCCS-ROM consumes less power than the CS-ROM because the SCCS-ROM consumes $f \times C_{BL} \times V_{CS} \times V_{DD}$ per group whereas the CS-ROM consumes $f \times (C_{BL} + C_{CS} + C_H) \times V_{CS} \times V_{DD}$. Moreover, the SCCS-ROM requires two control signals per group but the CS-ROM requires five control signals.

In the CS-ROM, we have to know the size of C_{BL} to choose the sizes of C_{CS} , C_H , and C_L . Moreover, it is hard to implement C_{CS} ,

C_H , and C_L exactly because the capacitors are so small that their sizes vary due to interconnections and layout mismatches. However, the SCCS-ROM shares C_{CS} , C_H , and C_L so that their sizes are large enough to overcome the effects of interconnections and layout mismatches. Therefore, the SCCS-ROM is more robust from noises.

Figure 4. Block diagram of shared-capacitor charge-sharing ROM

Figure 5. Shared-capacitor charge-sharing ROM

Figure 6. Sense amplifier

Figure 7. ROM cell layout (a) dummy bit lines (b) bit lines

4. SIMULATION RESULTS AND COMPARISONS

Table 1 shows the performance comparisons of various 32Kbit ROMs with 256 word lines, 128 bit lines, and 16bit output. The SCCS-ROM consumes 5.35mW at 100MHz clock frequency with $V_{DD} = 3.3V$. The area and delay of the SCCS-ROM are 0.18 mm² and 7.8ns. Circuit simulations are based on 0.35um CMOS technology and HSPICE models.

The compared conventional ROMs are a conventional ROM (CV-ROM) [1] and a charge-sharing ROM (CS-ROM) [4]. The CV-ROM uses the low power techniques; hierarchical word line, selective precharge, NMOS precharge, diffusion programming ROM core, and etc.

We assume that the voltage difference required for the sense amplifiers is 400mV. In the CV-ROM, the bit line swing voltage is $V_{DD}-V_t$ because NMOS transistors are used to precharge bit lines. In the CS-ROM and the SCCS-ROM, the bit line swing voltage is 800mV, which is twice the required voltage difference of the sense amplifier.

Power consumptions in each part of the ROMs are measured in Fig. 9. The results show that the bit lines and the control unit in the SCCS-ROM consume only 81% and 92% power compared to the CS-ROM respectively. The SCCS-ROM consumes 91.6% power compared to the CS-ROM. The area and speed of the SCCS-ROM are the same as the CS-ROM.

5. CONCLUSIONS

This paper proposes a shared-capacitor charge-sharing ROM (SCCS-ROM) using dummy bit lines. The SCCS-ROM reduces the swing voltage using the charge-sharing technique of the conventional charge-sharing ROM (CS-ROM) [4]. Although the CS-ROM needs three small capacitors per output, the SCCS-ROM shares the capacitors so that it needs only three capacitors. Moreover, the SCCS-ROM implements the capacitors using dummy bit lines. This not only increases noise immunity but also reduces power. The simulation results show that the SCCS-ROM reduces 8.4% power compared to the CS-ROM.

Figure 8. Simulated waveforms of the SCCS-ROM

Table 1. Comparisons of ROM (2K × 16 bits) performance

	Power [mW]	Area [mm ²]	Delay [ns]
Conventional ROM (CV-ROM) [1]	6.82	0.15	3.1
Charge-sharing ROM (CS-ROM) [4]	5.80	0.18	7.8
This work (SCCS-ROM)	5.35	0.18	7.8

Figure 9. Power consumptions in ROMs (2K x 16bits)

Figure 10. Layout

6. ACKNOWLEDGMENT

This work was supported by KOSEF through the MICROS at KAIST, Korea.

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