An OLED Display Driver IC Embedding -63dB CMR, 80mV/nA Sensitivity, 390pA Detectable, and Column-Parallel Pixel Current Readout for Real-Time Non-Uniformity Compensation

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Abstract

This paper presents a display driver IC that embeds column-parallel 11b pixel-current readouts to compensate for display non-uniformity. Leveraging the source-driven TFT pixel, the proposed techniques facilitate real-time current sensing, even while the display is active. Fabricated in 180nm, the chip achieves a -63dB rejection to common noise, a 390pA/LSB resolution, and an 80mV/nA sensitivity. Demonstrations with real LEDs effectively validated the pixel current sensing.

Introduction

Despite the rising prominence of OLED displays, the issue of non-uniformity, due to variations in the thin-film transistors (TFTs), remains a challenge (left of Fig. 1). In contrast to the current-mode drive [1] and the in-pixel compensation [2], external compensation [3-5], which directly measures the TFT pixel current (I_{pixel}), is proving particularly effective in OLED TVs for its superior capability to correct non-uniformities. However, I_{pixel}-sensing schemes still face challenges. Large common-mode noise (I_{CMn}), induced by supply ripples (V_{CMn}), hinders the accurate I_{pixel}-sense. This challenge intensifies in larger OLED panels due to increased parasitic capacitance (C_P), leading to higher I_{CMn} (right of Fig. 1). Although [4] and [5] employ differential analog front-ends (AFEs) to reject I_{CMn}, this approach results in doubled I_{pixel}-sensing time. Also, their common-mode rejection (CMR) to I_{CMn} remains insufficient for detecting sub-μA I_{pixel}. The non-real-time nature of their sensing, separated from display timing, may cause unwanted OLED emissions and user discomfort. Integrating AFEs into drive-column channels also demands a larger die area for the display driver IC. The channel size in [5] is too large, even without in-channel ADCs. In addition, the sensitivity of [5] is insufficient, increasing the burden on external ADCs. Although [4] occupies less space than [5] despite in-channel ADC, its resolution is limited to 39nA/LSB.

This paper presents an OLED driver IC that embeds column-parallel real-time I_{pixel} readouts, featuring high CMR and high sensitivity.

Proposed Readout and Source-Driver IC (RSIC)

Source-Driven TFT Pixel (Fig. 2)**:** In typical gate-driven pixels [3-5], a test voltage (V_{test}) is applied to the TFT gate, and I_{pixel} is measured via the drain when the OLED is deactivated. As a result, I_{pixel} differs from I_{OLED}, which directly determines the actual OLED luminance, thus making real-time sensing unfeasible. Beyond the data-lines, extra sensing-lines are required in the active-matrix. Moreover, apart from the gate-drive time, the gate-driven pixel must wait an extra duration for I_{pixel} to be delivered to the AFE. In the proposed source-driven pixel, I_{pixel} identical to I_{OLED} flows via the data-line when the actual display data (V_{data}) is programmed. This arrangement allows for real-time I_{pixel}-sensing even while the display is being driven. Fast I_{pixel}-sensing is also achievable, facilitated by the voltage-driven merits.

RSIC Channel (Fig. 3)**:** For display operation, V_{data} is driven to the OLED pixel by an AFE-combined amplifier (ACA) following the D/A conversion for the 10-bit data (D_{DAC}). While V_{data} settles, the ACA concurrently detects the current (I_{AFE}) flowing via the data-line. The I_{AFE} is then fed into a common-mode rejection filter (CMRF) to suppress I_{CMn}. The resulting filtered current (I_{filt}), which accurately represents I_{pixel}, is converted into an 11-bit digital output (D_{out}) through a folding-integrator (FI) and a residual SAR ADC. In the voltage-driving, a sample-and-hold (S/H) is utilized, enabling the R-DAC to be reused during the SAR A/D conversion, thereby saving channel area.

BW-Transitional ACA (Fig. 4)**:** The ACA design employs a class-AB amplifier at its core, featuring two output stages. The primary output stage is dedicated to drive V_{data}, while the corresponding replica stage concurrently replicates the data-line current into I_{AFE}. The dual functionality, in driving V_{data} and sensing I_{AFE}, necessitates meticulous optimization of the ACA's bandwidth (BW). A wider BW allows for rapid stabilization of V_{data} and I_{AFE} at the expense of decreased noise-filtering effect. Conversely, a narrower BW enhances noise filtration at I_{AFE} but results in slower driving and sensing speeds. To navigate this trade-off, the proposed ACA incorporates a BW-transitional design, enabled by a BW-control circuit (BCC). The BCC adaptively adjusts the ACA's transconductance (G_{mi}) in response to the amplifier's input difference, $|V_{INp} - V_{INn}|$. Initially, the BCC boosts the BW to expedite the settling of V_{data} and I_{AFE}. As $|V_{INp} - V_{INn}|$ approaches 0, it reduces the BW to bolster noise suppression. This strategy allows the ACA to obtain both rapid sensing and effective noise reduction.

Channel-Shared CMRF (Fig. 5)**:** This aims to filter out I_{CMn} (AC noise common to adjacent N channels) while allowing I_{pixel} (a unique DC readout signal) to be delivered to the I_{filt} output. To maximize the I_{CMn} rejection, the channel-sharing (CS) method is proposed, which involves aggregating the capacitive AC currents ($I_{AFi} = N \cdot I_{CF}$) from the adjacent N channels and feeding them back to the CMRF input (I_{FB}). This approach virtually boosts the filtering capacitance to $N \cdot C_F$, thus saving die area by obviating the need for large capacitance. Besides, the high-pass amplifier (HPA), working with a low-voltage supply, further amplifies the feedback signal as $I_{AFo} = A_F(s) \cdot I_{AFi}$, where $A_F(s)$ includes a zero at ω_z. This not only enhances the CMRF's feedback loop-gain but also elevates the order of the low-pass filtering for I_{CMn}. The combination of CS and HPA with $N = 8$ offers up to -63dB rejection within the supply-ripple frequency (f_{CMn}) range of 1.5 to 2MHz.

Folding Integrator & ADC (Fig. 6)**:** An integrator is utilized to convert the sensed current into a voltage-domain signal (V_{int}). To alleviate the burden on the ADC, high sensitivity (mV/nA) is essential. However, V_{int} is at risk of saturation, imposed by the supply voltage (V_{DD}) constraint. This work proposes a folding integrator (FI) able to drastically expand the dynamic range (DR) while achieving high sensitivity.

The proposed FI integrates I_{filt} and converts it into a digital output, as follows: When V_{int} reaches V_{ref} during integration with C_1 (or C_2), a comparator detects it, and V_{int} is folded back to V_{CM} by substitution with the empty C_2 (or C_1). Note that $|V_{ref} - V_{CM}|$ is half of the full-scale range (HFS). Whenever the folding occurs, the MSB 5-bit D_{FOLD} increments by +1. After the integration (T_{int}), a residue of V_{int} is then A/D converted to an LSB 7-bit D_{SAR} using the SAR ADC, which reuses R-DAC employed for the voltage driver. The final 11-bit output (D_{out}) is constructed by summing D_{FOLD} and D_{SAR}, with a 1-bit overlap. The FI offers 16× DR, as well as a high sensitivity of 80mV/nA.

This work also presents a novel technique to correct the FI's error (V_e) induced by the comparator's nonidealities. As shown at the bottom of Fig. 6, C_1 and C_2 swap roles during operation. Throughout this process, they compensate for V_e by transferring it between themselves each time they exchange roles. Thus, the residue of V_{int} is free from V_e.

Measurement Results

The RSIC was fabricated in a 180nm CMOS (Fig. 7). Fig. 8 shows the measured V_{data} for display inputs (D_{in}) and the current-sensing waveforms of V_{int} for $I_{pixel} = 0$ and 600nA, demonstrating up-folds for $I_{pixel} > 400$nA (I_{bias}) and down-folds for $I_{pixel} < I_{bias}$. The driver can support 60Hz 4K displays, but the real-time readout adaptively conforms to the variable refresh rate (VRR). The left of Fig. 9 shows the frequency response of CS-HPA CMRF, indicating -25dB improvement in AC common-noise suppression. The effectiveness of CMRF is reconfirmed in the mid-bottom of Fig. 9. The mid-top of Fig. 9 verifies the error correction within the FI, showing a deliberate V_e of ±150mV is canceled out. The right of Fig. 9 shows the I_{pixel} vs. D_{out} curve. Fig. 10 details the I_{pixel}-readout linearities (INL/DNL) and the SNR. Fig. 11 showcases a real demonstration using LEDs, clearly observing that the sensed I_{pixel} (D_{out}) correlates well with the actual LED luminance, thereby verifying the RSIC's efficacy in compensating for display non-uniformities. Fig. 12 tabulates the performance summary. This work outperforms prior works in terms of common-noise coverage (3.57μA$_{pp}$), resolution (390pA/LSB), SNR (60.3dB at C_P = 100pF), sensitivity (80mV/nA), and real-time functionality. Despite fully column-parallel, this work also achieves the smallest size per channel.

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References

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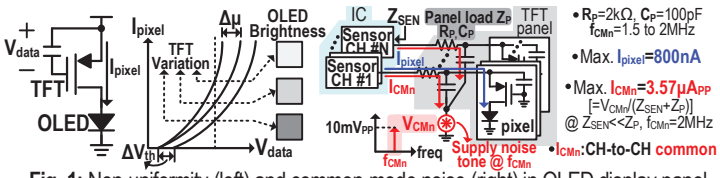

Fig. 1: Non-uniformity (left) and common-mode noise (right) in OLED display panel.

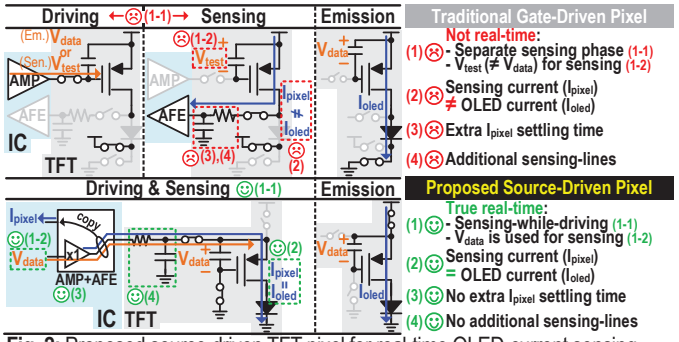

Fig. 2: Proposed source-driven TFT pixel for real-time OLED-current sensing.

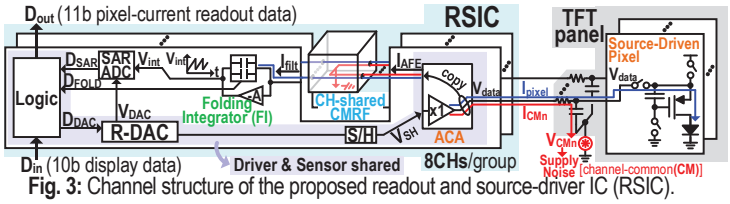

Fig. 3: Channel structure of the proposed readout and source-driver IC (RSIC).

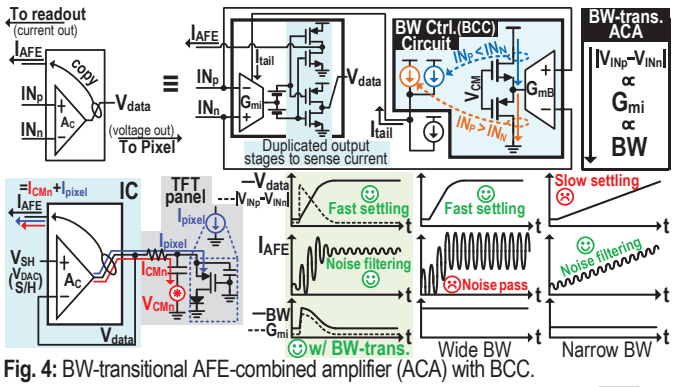

Fig. 4: BW-transitional AFE-combined amplifier (ACA) with BCC.

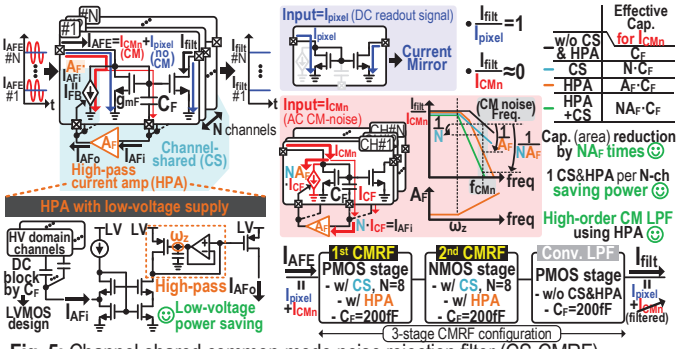

Fig. 5: Channel-shared common-mode noise rejection filter (CS-CMRF).

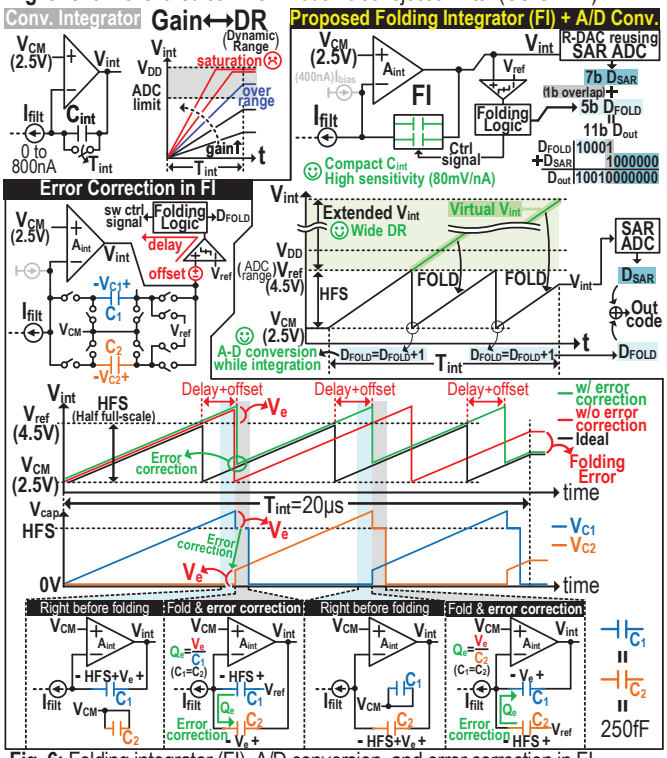

Fig. 6: Folding integrator (FI), A/D conversion, and error correction in FI.

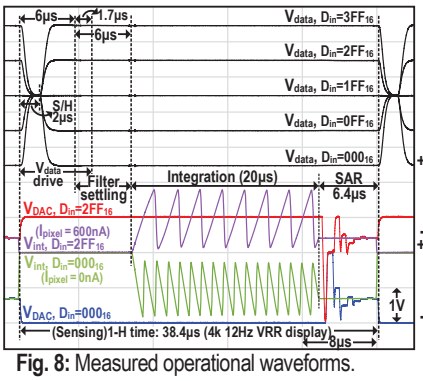

Fig. 8: Measured operational waveforms.

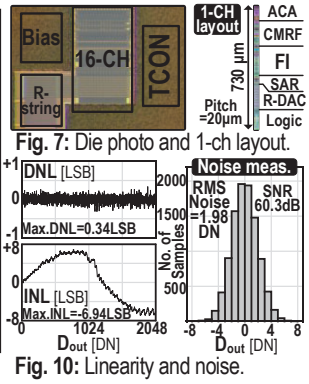

Fig. 10: Linearity and noise.

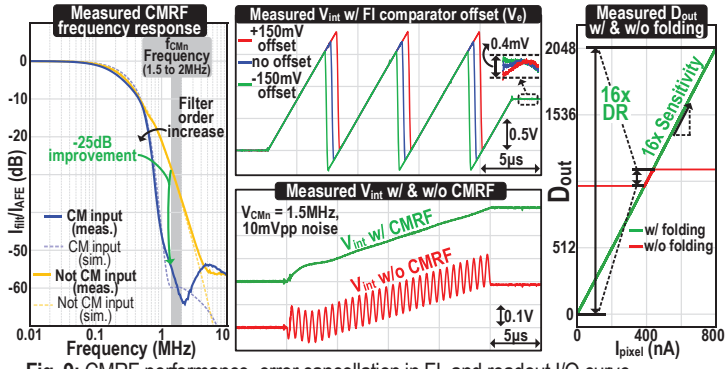

Fig. 9: CMRF performance, error cancellation in FI, and readout I/O curve.

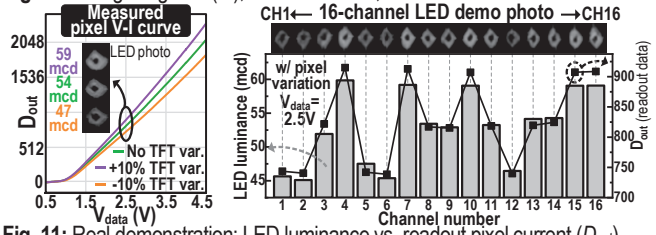

Fig. 11: Real demonstration: LED luminance vs. readout pixel current (D_{out}).

	JSSC'16 [4]	TCAS-I'23 [5]	This work
Technology	180nm CMOS	180nm CMOS	180nm CMOS
V_{data}-drive time	7.7 µs (4k 60Hz)	5.1 µs (QHD+ 60Hz)	7.7 µs (4k 60Hz VRR)
I_{pixel}-sense time	131* µs	40* µs	38.4 µs (4k 12Hz VRR)
Pixel structure	Gate-driven (3T1C)	Gate-driven (3T1C)	Source-driven (4T1C)
Sensing while display	X	X	O (real-time)
Data-line load (R_P / C_P)	30 kΩ / 30 pF	6.5 kΩ / 35 pF	2 kΩ / 100 pF
Max. coverable I_{CMn}**	0.25 µApp	0.7 µApp	3.57 µApp
I_{CMn} rejection (CMR)	-	-	-54 to -63 dB
ADC configuration	8b current-mode DAC + 1b comparator	- (No on-chip ADC)	5b folding integrator (FI) + 7b SAR ADC reusing R-DAC
Sensing resolution & Max. DNL	1-LSB = 39 nA (in 8bit) & 0.56 LSB (21.9 nA)	- (No on-chip ADC)	1-LSB = 390 pA (in 11bit) & 0.34 LSB (0.13 nA)
Current sensing sensitivity	-	6.88 mV/nA (0.55V/80nA)	80 mV/nA (64V/800nA)
SNR	-	62 dB (AFE only)	60.3 dB (end-to-end)
C_P-normalized SNR***	-	77.4 dB (AFE only)	80.3 dB (end-to-end)
Power per channel	Data Driver: 20 µW (2 drv.) + Sensing AFE: - + ADC: Comp. 8.5 µW CDAC 50 µW = 78.5 µW	Data Driver: 52 µW (2 drv.) + Sensing AFE: AFE 26 µW + ADC: - = 78 µW	Data Driver: ACA 21.2 µW + Sensing AFE: CMRF 21.5 µW + ADC: FI 37.5 µW SAR 1.2 µW = 81.4 µW
Channel configuration	2 drivers (10b) + 1 comp. & CDAC (8b)	2 drivers (10b) + 1 AFE	1 driver (10b) + 1 AFE + 1 ADC (11b)
	2 data-lines / 1 CH (time-interleaving*)		1 data-line / 1 CH (column-parallel)
1-channel area	38,906 µm²	67,500 µm²	14,600 µm²

* Doubled effective time due to differential sensing. ** $V_{CMn(pp)}/Z_P$ @ noise frequency of each work.
*** 20·log{ signal / (noise / $C_P^{1/2}$ [$pF^{1/2}$])} [dB], considering noise amplification effect of C_P [6].

Fig. 12: Performance summary in comparison with prior works.