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Solder reflow process induced residual warpage measurement and its influence on reliability of flip-chip electronic packages

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Abstract

To meet the future needs of high pin count and high performance, package size of flip-chip devices is constrained to become larger. In addition, to fulfill the environment issues, lead free solders will be replacing lead contained eutectic (Sn/37Pb) in near future. Thus, in this work, the effect of residual warpage and consequent residual stress on the reliability of large flip-chip using lead free solder is examined. Several effective experimental approaches to accurately measure residual warpage, using Moiré interferometry, shadow Moiré, and image processing schemes, are introduced. Moreover, geometric, process, and material parameters affecting the residual warpage during reflow process are discussed and some modifications are suggested. Finally, it is verified that it is crucial to accurately quantify and control the residual warpage in order to guarantee the overall reliability of flip-chip packages regardless of presence of underfill.
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1. Introduction

Flip-chip on board (FCOB) technology possesses the highest packaging density compared with other electronic packaging approaches, and is expected to become a mainstream technology in the near future [1]. It attracts increasing attention from the electronic packaging industry due to their good thermal performance, smaller size, lower profile, lighter weight, higher I/O density, high speed, low inductance, fine pitch, etc. [2–4]. However, the difference in the coefficient of thermal expansion (CTE) between the chip and the substrate makes flip-chip configurations vulnerable to thermally induced strains and often results in solder joint fatigue [5]. As an effective solution, filling the space between the silicon die and PCB with underfill encapsulant mechanically couples the severely CTE mismatched chip and substrate and provides a significant (at least one order of magnitude) enhancement in solder joints reliability [3,5–7,9–12]. This mechanical coupling between the die and the substrate reduces the strain in the solder connections by additional load transfer through the shear stresses, thus enhancing the thermomechanical reliability of flip-chip assembly [13]. Extensive studies have already made clear that the thermal fatigue life of the solder

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joints can be greatly improved when the underfill material has a low CTE, a high Young's modulus and a high glass transition temperature (T_g) [14–16].

However, even with underfill, the reliability of solder joints is still a serious concern in FCOB assembly [17,18]. The accurate failure prediction of solder joints may be hindered by factors such as underfill imperfection [10,12,19–22] or assembly process induced residual stresses [11,23,24]. In this study, the latter is focused for closer analysis, especially during solder reflow process which appears to be more severe when Sn/37Pb(SP) is replaced to Sn/3.0Ag/0.5Cu(SAC), lead free solders. This is ascribed to the inherent material behavior of SAC which tends to creep and relax less than SP at low stress levels [25–28] which will be discussed further in Section 2.2.

Most of existing works to predict effects of sequential processing steps on manufacturing stresses or deformations, are based on non-linear visco-plastic numerical analysis [23,24,28–32]. Although there exist some experimental works to directly measure residual warpage and stresses during fabrication process [3,11,33,34,59], not many of them have mainly focused on soldering process, neither have addressed a direct comparison between lead contained and lead free solders. Polsky et al. [35], Stiteler et al. [36], and Chien et al. [37] have investigated the warpage behavior of packages or PCBs during soldering processes, however, the works are primarily interested in the warpage of substrate or package themselves under reflow history rather than the warpage induced due to mechanical coupling of chip and substrate through solder.

There exist various techniques in order to accurately measure warpage of chip or substrates. Covering the recent works, geometric Moiré [38] methods, including shadow Moiré [35–37,39–42] and projection Moiré [41], in-plane Moiré interferometry [43–50], Twyman–Green (Michelson) interferometry [34,51,52], Fizeau interferometry [53,54], stylus scratch method [58], touch probe method [32] and laser profilometry [55,56] are well developed and frequently applied methods in electronic packaging field. Each technique comprises of both merits and demerits at the same time, thus, one should carefully decide considering effectiveness to one's own engineering application. Pioneer works of late 1980s and early 1990s, especially on optical methods, are well summarized by Suhling [57].

In this work, in-plane Moiré interferometry in company with newly developed image processing filter is applied to measure residual warpage of flip-chip after solder reflow process. The amount of warpage is relatively small, happening to occur between 0 and 10 μm, which is too little to apply conventional geometric Moiré methods. For verification, alternative experimental approaches are performed. Adopting in-plane Moiré interferometer and thermal optical chamber, residual warpage is estimated by in situ measurement of V-displacement field while heating the package up to its full relaxation. For SAC(Sn/3.0Ag/0.5Cu) which does not relax even up to 175 °C of heating, shadow Moiré technique with fine grating (5 μm pitch) is applied to evaluate its residual warpage. In addition, the effect of material property (SAC vs. SP(Sn/37Pb)) of solders on residual warpage is emphasized. It is discovered that residual warpage and stresses induced during solder reflow process significantly affects the entire reliability of flip-chip regardless of presence of underfill.

2. Experiments and results

2.1. Flip-chip assembly

The flip-chip package studied in this work is composed of silicon chip, C4 solder joints, and PCB substrate (Fig. 1). The chip has a side dimension and thickness of 10.0 mm and 0.685 mm, respectively. Single

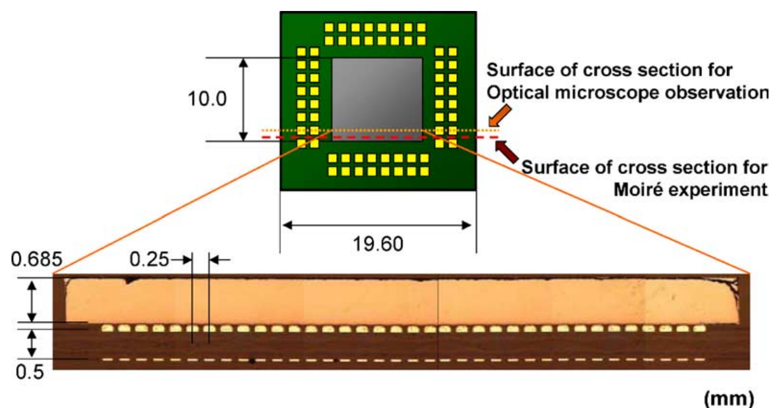


Fig. 1. Flip-chip assembly design.

row 144 I/Os are distributed at the peripheral of the chip with 0.25 mm pitch, 0.12 mm pad size, and 0.095 mm passivation openings. 19.6 mm^2 PCB substrate of 0.5 mm thickness is designed with four point probe daisy chains so that electrical connection of 16 solders located at each corners can be monitored. Electrical resistance of solder joints is measured at room temperature in between certain number of cycles. Solder pastes, SP and SAC alloys, are screen-printed on electroless Ni–P UBMs resolving low-cost and simple flip-chip bumping. Five microns of Ni–P layer and 0.08 μm of Au layer are plated on Al pads where solder bumps of 120 μm diameter are fabricated subsequently. The solder bumps on Si chip are dipped into a flux and then aligned to the substrate using flip-chip bonder. Soldering was performed using a reflow module on the flip-chip bonder with peak temperature of 230 °C and 280 °C for SP and SAC, respectively. Reflow of each solder was performed as followed processes:

1. Flux activation at 150 °C for 1 min.
2. Solder melting at peak temperature for 1 min.
3. Air cooling to room temperature.

Finally, flux cleaning is followed in DI (deionized) water at 60 °C.

2.2. Moiré experiment

Moiré interferometry is a whole-field in-plane displacement optical measurement technique with both high displacement sensitivity and high spatial resolution. It is especially effective for the non-uniform in-plane deformation measurements and has been used in the research and development of microelectronic packages to measure thermally induced displacement fields.

A thin cross-line diffraction grating is replicated onto the cross-section of interest and deforms with the sample. Interaction between two coherent laser beams with the deformed grating produces an interference pattern representative of the thermally induced displacement field. Based on a grating frequency, f of 1200 lines/mm, each interference fringe spacing represents 417 nm relative displacement difference which explains the definition of sensitivity [38]. Thermally induced deformations can be extracted from the displacement fields by the following relationship:

$$U(x,y) = \frac{1}{f} N_x(x,y) \quad (1)$$

$$V(x,y) = \frac{1}{f} N_y(x,y) \quad (2)$$

where N_x and N_y are the fringe orders in U and V fields, respectively.

In order to measure the residual warpage of chip and PCB after soldering process, bare chip and PCB are cross-sectioned and polished separately until the flat surface is guaranteed as in Fig. 2(a). They are polished in such a way that surface of cross-section is controlled to be shown in Fig. 1. The surface does not include solder bumps. Since warpage is a global deformation which occurs mainly due to chip and PCB CTE mismatch the presence of solder in the measured surface would not affect the value significantly. After polishing, a 1200 lines/mm cross-line diffraction grating is replicated on the cross-section of interest using TRA-BOND F114 epoxy as shown in Fig. 2(b). The epoxy has T_g of 128 °C and operation temperature range varies from (−)60 °C to (+)130 °C. The replication is performed at room temperature (23 °C) and cured for 24 h. The thickness of epoxy is extremely lower than the specimen. It is controlled to be below 5 μm. Its modulus is also an order lower than packaging materials. Thus the deformation of epoxy is thoroughly confined to that of the specimen. Situation is preferable if temperature exceeds the T_g of the epoxy since the modulus of epoxy is further decreased.

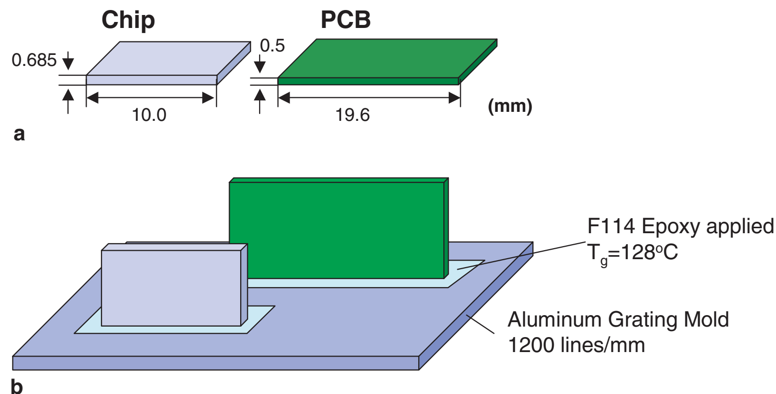


Fig. 2. Specimen preparation for Moiré experiment: (a) separate polishing for chip and PCB; (b) separate diffraction grating replication at room temperature (23 °C).

However, epoxy will not reflect the deformation of the specimen in case the adhesion is lost. The adhesion of the epoxy is guaranteed by several pretests. It lasted for 4000 cycles from (−)50 °C to (+)150 °C.

After confirming the null field of each adherends, the chip and PCB are bonded by solder reflow process as mentioned in previous section. Figs. 3 and 4 reveal the residual warpage ascribed to mechanical coupling of chip and substrate through soldering process measured by in-plane Moiré system. The convex type warpage, which can be calculated by counting the fringes from V field, is observed for both chip and PCB where severe warpage is apparent for SAC compared to SP. This is ascribed to the inherent material behavior of SAC which tends to creep and relax less than SP at low stress levels, which is well defined from quantitative studies of various works [25–28]. Sasaki et al. [28] has performed actual stress relaxation test which confirms this argument. In addition, Wiese et al. [25,26] and Amagai et al. [27] have found out with their well-controlled creep tests that SAC creeps less than SP. The fact that SAC experiences larger cooling ΔT excursion during reflow history also contributes to this existing state. The warpage of chip and substrate are acquired independently since the plane of incidence is slightly different due to separate polishing.

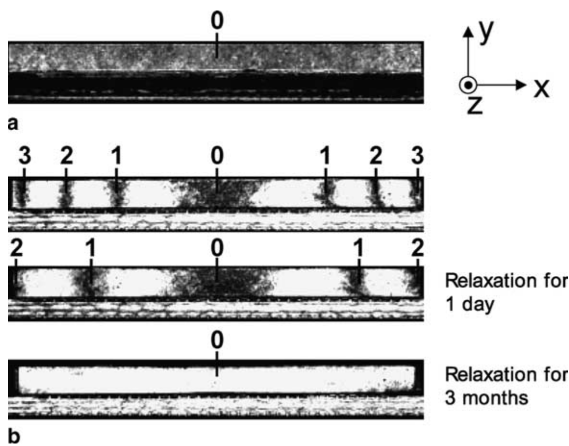


Fig. 3. Residual warpage measurement after solder reflow process: (a) SP (Sn/37Pb) chip; (b) SAC (Sn/3.0Ag/0.5Cu) chip.

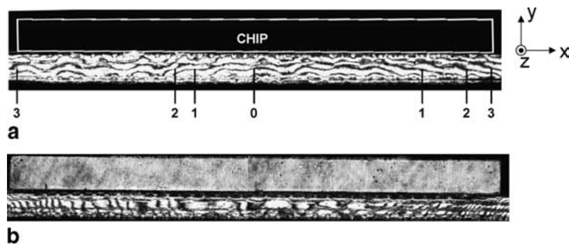


Fig. 4. Residual warpage measurement after solder reflow process: (a) SP (Sn/37Pb) PCB; (b) SAC (Sn/3.0Ag/0.5Cu) PCB.

In case of SP, chip is observed to have no warpage (Fig. 3(a)) while there exists slight amount of 1.251 μm for PCB (Fig. 4(a)). This reflects the fact that, as it was expected, chip is readily flattened back owing to its high bending stiffness originated in high Young's modulus and large thickness compared to PCB. In case of SAC (Fig. 3(b)), chip is slightly warped about 1.293 μm at the beginning of measurement (several hours after solder reflow). However, the warpage is gradually mitigated due to relaxation of residual stress at solder and finally disappears after 3 months of storage at room temperature.

The warpage of PCB for SAC, as shown in Fig. 4(b), contains many low frequency noises which may have arisen from higher temperature exposure during reflow process. Inspecting the dark noise region applying highly magnifying zoom lens (3.0 mm field of view with 640×480 pixel CCD camera) with higher NA (numerical aperture) and enhancing the illuminance, it is affirmed that the fringe connectivity is maintained. This implies that the noises are the result of local residual out-of-plane deformation (direction normal to the plane of cross-section, z-direction) of PCB rather than specimen grating deterioration. The out-of-plane deformation of substrate which is postulated to become abruptly accelerated between 230 °C and 280 °C, locally varies the incident plane angle from previous cross-sectioned plane and gives rise to low frequency noises.

2.3. Phase shifting filter

In order to accurately quantify the warpage amount for PCB of SAC an image processing filter is developed, namely, the phase shifting filter. The main concept of the proposed imaging filter is to classify the intensity value rather it is a noise or a data at (i,j)th pixel. Intensity of a Moiré fringe pattern can be expressed in following tensor equation:

$$I_{ij}^{k} = D_{ij} + A_{ij}\cos(\phi_{ij} - \delta_k) \quad (3)$$

where i and j are the indexes for x and y pixel in the image and k is for the phase shift. I_{ij} denotes the intensity value from the fringe pattern, ϕ_{ij} is the phase value at corresponding pixel, δ_k is the phase shifting amount, D_{ij} is the mean intensity or the background intensity, and A_{ij} is the visibility. The intensity value of (i,j)th pixel will follow Eq. (3) and alter when it is phase shifted due to change in δ_k (Fig. 5(b)). However, it will remain constant if the intensity value at (i,j)th pixel is a noise as in Fig. 5(a). A variance is defined which reflects the degree of difference between the original image and the phase shifted images.

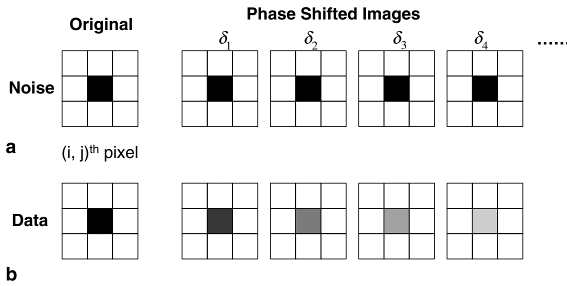


Fig. 5. Conceptual idea of phase shifting filter—intensity variation respect to consecutive phase shifts: (a) case when (i,j)th pixel is a noise; (b) case when (i,j)th pixel is a data.

The total variance at (i,j)th pixel, V_{ij} is defined to be the sum of variance at each phase shifted steps and can be expressed by the following:

$$V_{ij} = \sum_{k=1}^{N}((I_{ij}^{0} - I_{ij}^{k})^{2}) \tag{4}$$

where N refers to total number of phase shifts within a single phase travel, I_{ij}^{k} is the intensity of kth phase shift, and I_{ij}^{0} is the original image without any phase shift. Process algorithm is depicted in Fig. 6, where V_{thres} is the threshold variance determined arbitrarily by the user considering the noise level. Fig. 7 shows the residual warpage (V field) of PCB under the chip for SAC where the phase shifting filter is applied to enhance the accuracy in counting the fringe order. The total number of phase shifts, N is equal to 13 for current analysis. Reference grating is phase shifted with PZT driven actuator in in-plane interferometer system. The pixels which have V_{ij} lower than V_{thres} are defined as noises. They are flagged by designating the intensity value as 255 which is revealed as white dots in Fig. 7. From the original image where it is impossible to perform accurate fringe counting, feasible fringe counting is possible after the filtering. In some cases, multi-filtering with two different thresholds should be performed to increase the accuracy as in Fig. 7(a). The amount of warpage is estimated to be 7.089 μm which is about five times larger than that of SP. There exist warpage difference in right and left half of PCB. Usually, flexible substrates including thin PCB does not warp symmetrically. Especially, for such cases where solder is bonded peripherally without underfill, high asymmetric is expected.

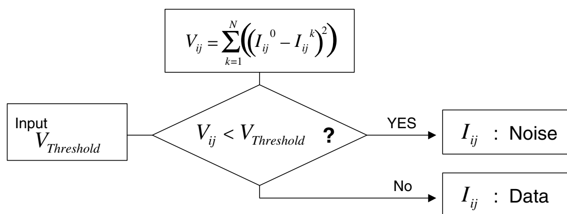


Fig. 6. Process algorithm (flow chart) for phase shifting filter.

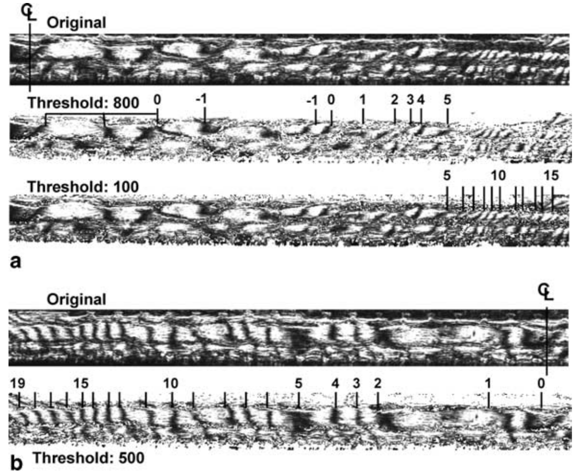


Fig. 7. Application of phase shifting filter in counting the fringes for residual warpage of SAC PCB: (a) right half of PCB; (b) left half of PCB.

2.4. Verification of warpage measurement through thermal relaxation

An alternative experiment with both SP and SAC is performed to verify the residual warpage measured in previous section. Different from the former experiment grating is replicated at room temperature after the chip and PCB are bonded through solder reflow process. Thus, the convexly warped state is set as reference as shown in Fig. 8(a). As the specimen is heated from room temperature to 125 °C, the warped chip and PCB will gradually relax and become flat due to relaxation behavior of solder. This flattening will appear as concave bending in Moiré fringes as in Fig. 8(b). Relaxation behavior of warpage is expected to saturate and converge to a certain value when it becomes completely flat upon full relaxation. Thermal relaxation procedure can also be achieved by imposing prolonged holding time at considerably high temperature. However, it also

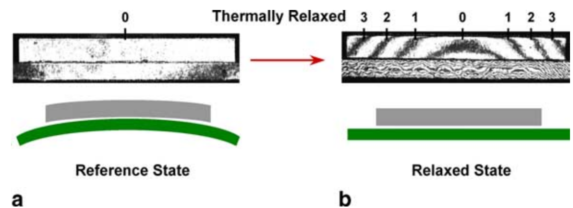


Fig. 8. Residual warpage measurement through thermal relaxation: (a) reference state: convexly warped state; (b) seemingly, concavely warped state: flattened state.

requires certain degree of bending stiffness of the adherends to become flat.

In order to resolve deformation behavior during high temperature condition the Moiré system is connected to the optical environmental chamber (EC1A, Sun Systems) as in Fig. 9. The air inside the chamber must be circulated vigorously to achieve the heating/cooling rate and maintain isothermal condition. Consequently, the environmental chamber experiences vibrations, which are normally transmitted to the specimen. However, vibrations can be tolerated if there is no relative motion, i.e., if the specimen and the optical system vibrate in unison. To fulfill this requirement, the specimen holder is connected directly to the interferometer and it is essentially free from the chamber [45].

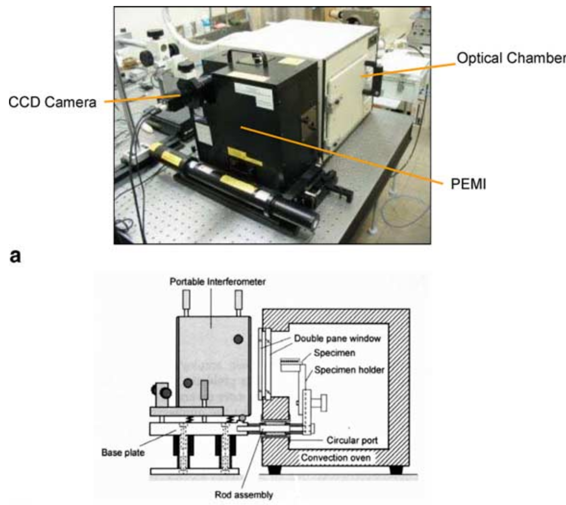


Fig. 9. Experimental setup for thermal relaxation test: (a) setup feature; (b) schematic design view (adapted from [45]).

In Fig. 10, results clearly reveal that the amount of residual warpage is in quite good agreement with the values obtained in previous section for SP chip, SP PCB, and SAC chip. However, for SAC PCB, low bending stiffness of PCB as well as low degree of relaxation behavior of SAC hinder the full relaxation. It failed to relax fully, even at 175 °C with 30 min holding time (Fig. 11). Accurate warpage above 175 °C was unattainable due to poor spatial resolution caused by high coefficient of thermal expansion (CTE), α_y of PCB which resulted in excessive thermal deformation in y-direction as shown in Fig. 11.

2.5. Fine pitch grating shadow Moiré

As an alternative solution to quantify the residual warpage of SAC PCB, a shadow Moiré setup is developed. This, non-contact, simple, and relatively low cost setup provides whole-field fringe pattern of out-of-plane displacement. A Moiré pattern is a visual pattern produced by the superposition of two regularly spaced gratings that geometrically interfere to create light and dark fringes [35]. The shadow Moiré method uses a reference grating which is placed directly in front of a test object or specimen. The shadow of reference grating on the specimen, generated from transmitting a collimated beam of light through the grating, produces a virtual grating, termed specimen grating [17]. When the surface under investigation is inclined or curved, shadow Moiré fringes are formed by interaction between these two

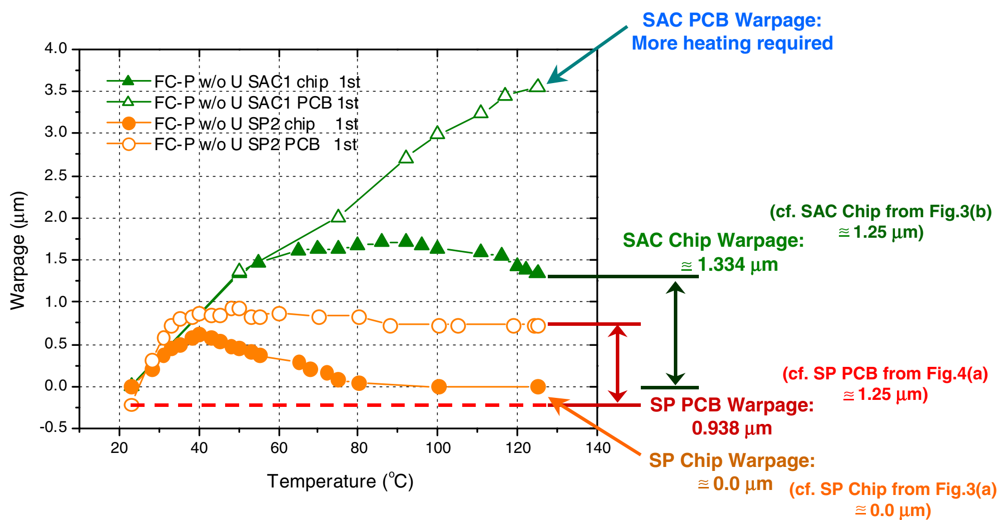


Fig. 10. Residual warpage measured by thermal relaxation test.

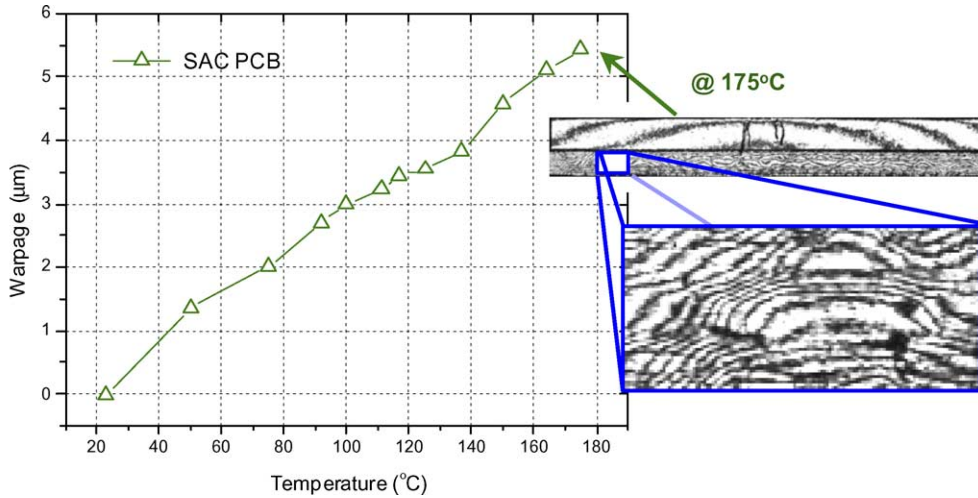


Fig. 11. Warpage variation measured by thermal relaxation test for SAC PCB up to 175 °C.

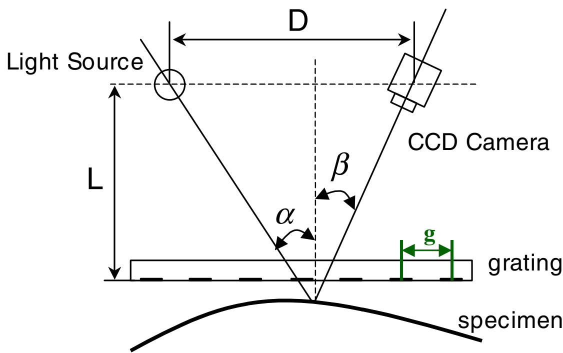


Fig. 12. Typical schematic design for shadow Moiré system.

gratings. Fig. 12 is a typical schematic design for shadow Moiré system. The governing equation of the out-of-plane displacement can be expressed as the following:

$$W = \frac{g}{\tan\alpha + \tan\beta} N_z \quad (5)$$

where g is the grating pitch, N_z is the fringe order, α is the incident angle, and β is the viewing angle. If the CCD camera and light source are separated by the distance D and located at the identical distance L from the grating, by the following relation:

$$\tan\alpha + \tan\beta = \frac{D}{L} \quad (6)$$

Eq. (5) is simplified to

$$W = \frac{gL}{D} N_z \quad (7)$$

Basic sensitivity,

$$\eta = \frac{gL}{D} \quad (8)$$

which refers to the minimum relative displacement the system can optically resolve, is usually set to be 10–100 μm/fringe for shadow Moiré. Sensitivity can be enhanced up to sub-micron level by adopting phase shifting module and imposing related image processing schemes. However, intrinsic non-linearity of phase shifters and dependence of image processing on test conditions may cause adverse affects to the accuracy and repeatability of the system. Thus, in this work, optical sensitivity is elevated by introducing 200 lines/mm (5 μm pitch) quartz glass grating so that the warpage of SAC PCB can be measured which is expected to be around 7 μm. Fig. 13 shows the shadow Moiré setup. Collimated, monochromatic ($\lambda = 632.8$ nm) laser source

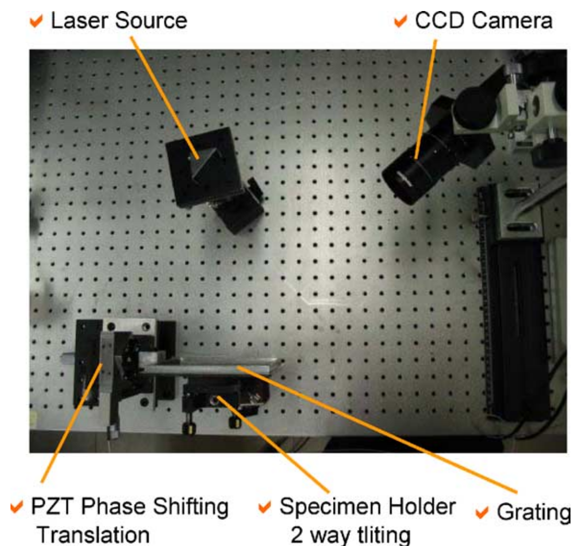


Fig. 13. Feature of shadow Moiré setup for this study.

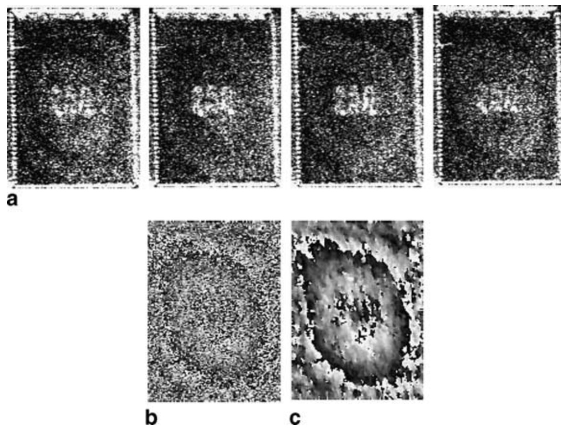


Fig. 14. Residual warpage of SAC PCB measured by fine pitch shadow Moiré method: (a) phase shifted images; (b) phase map; (c) filtered phase map.

is applied for the light source and the sensitivity is fixed to be 5 μm/fringe by selecting the incident angle, $\alpha = 0°$ and viewing angle, $\beta = 45°$.

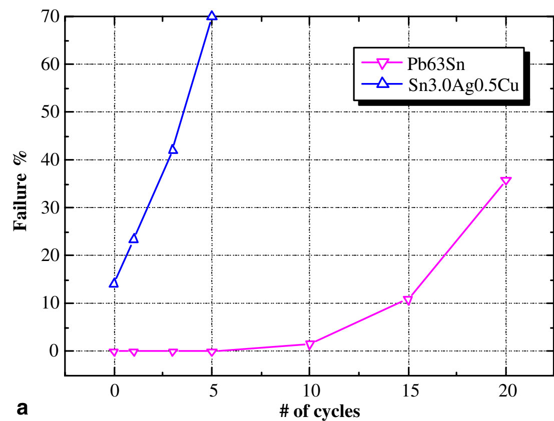
The shadow Moiré fringe shown in Fig. 14(a) revealed poor contrast or visibility, thus, it is phase shifted to obtain the phase map for clear fringe counting (Fig. 14(b) and (c)). The estimated amount of warpage, 7.0 ± 0.3 μm, is in good agreement with the previous data.

3. Discussion

It is found that different amount of residual warpage of chip and PCB is developed for different solder alloys after the solder reflow process (Table 1). In either solders, SAC or SP, chip and PCB are obliged to warpage due to CTE mismatch during cooling process. During their warped state, solder joints are in mixed mode stress condition, normal tensile (=peel) and shear existing at the same time. However, in SP, warpage is easily

Table 1
Residual warpage measurement results (μm)

	Testing methods			Error (%)
	Moiré interferometry with phase shifting filter	Thermal relaxation	Fine pitch shadow Moiré	
SP				
Chip	0.0	0.0	–	0
PCB	1.251	0.938	–	25.0
SAC				
Chip	1.293	1.334	–	3.1
PCB	7.089	–	7.0 ± 0.3	± 4.2



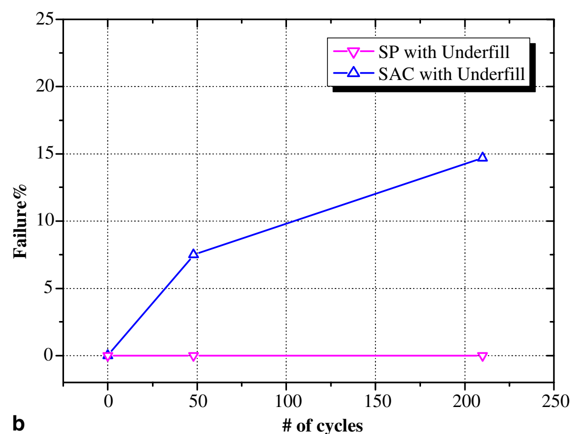


Fig. 15. Thermal cycling life data for SAC vs. SP (−55 °C to +125 °C): (a) Without underfill case; (b) With underfill case.

decreased due to relaxation of stresses (both normal and shear) and creep deformation in shear, leading the package to nearly pure shear state. For SAC which relatively relax and creep less than SP, remains in warped state, still carrying significant amount of stresses. Normal stress can be identified as the main cause of early fracture failure of flip-chips without underfill. It acts normal to the crack fronts and the resulting opening mode crack propagation conditions are mostly responsible for the failure [10]. Even if solder bump failure due to board warpage is not immediate, weakened bumps can pose a serious reliability risk [8].

According to thermal cycling test results of Fig. 15, non-underfilled SAC which has about five times larger warpage difference than SP, starts to fail from the first cycle with much faster failure rate. The typical failure mode for SAC is observed to be the brittle failure at Al/Ni interface while for SP is found to be solder fatigue near UBM (Fig. 16).

As it was mentioned earlier underfill provides a significant (at least one order of magnitude) enhancement in solder joints reliability [3,5–7,9–12]. However, the

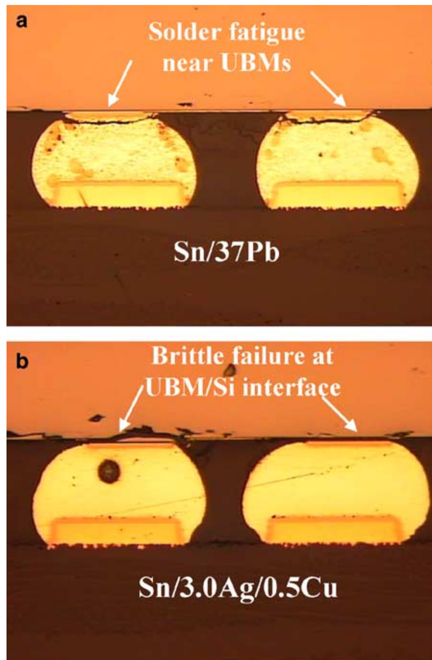


Fig. 16. Failure analysis with optical microscope after several thermal cycles (without underfill case): (a) SP after 20 cycles; (b) SAC after 3 cycles.

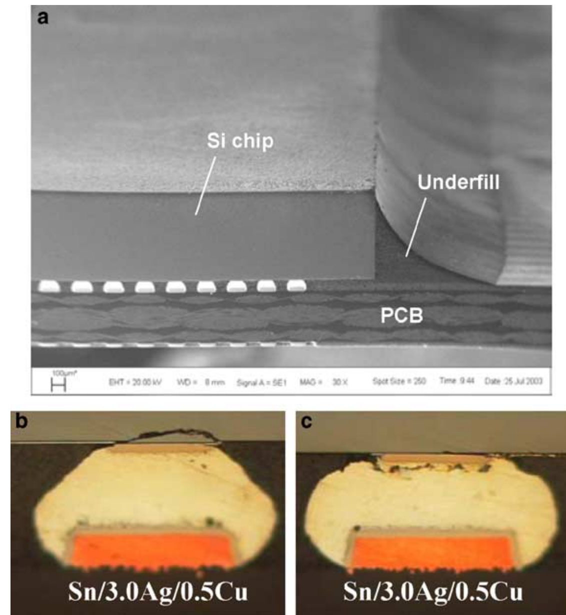


Fig. 17. Flip-chip with underfill case: (a) SEM image of underfilled flip-chip before thermal cycling; (b) optical microscope inspection for SAC after 100 cycles—Si cratering and UBM/Al failure; (c) crack along IMC.

reliability of SAC is still poor even with underfill. Dissimilar to underfilled SP which lasts for 1000 thermal cycles without any failure, 30% of the specimens are failed after 100 cycles through crack propagation at UBM/Al interface and IMC region for SAC (Fig. 17). It can be surmised that high normal strain/stress may have caused crack to propagate readily through brittle interface and material in SAC. This mechanism is revealed as high failure rate for SAC either it is underfilled or not.

To meet the future needs of high pin count and high performance, the LSI die and package size of flip-chip devices is constrained to become larger [3]. Besides, many of the products that use flip-chips use relatively thin substrate (0.5–1.0 mm), which increases board flexure during manufacturing process [8]. Moreover, to fulfill the environment issues SAC will be replacing SP in near future. In order to guarantee the reliability of solder joints for flip-chip using SAC, it is crucial to accurately quantify and control the residual warpage, as it is discussed in this work. There exists several parameters affecting the residual warpage during reflow process. Residual stress is expected to diminish if the bending stiffness or compliance of chip and PCB are matched. This can be achieved by varying the thickness of the two adherends at the early design stage. A solder alloy with superior stress relaxation nature is preferred to reduce the residual stress, such as SP. Moreover, subsequent relaxation through thermal aging process is anticipated to decrease the residual stress effectively. Besides, lowering the peak temperature and reducing the cooling rates during solder reflow process can also contribute to mitigate the residual stresses.

4. Conclusions

Several experimental techniques to measure small residual warpages (0–10 μm range) are suggested and its significance on reliability of entire flip-chip package is discussed.

1. Residual warpage of chip and PCB are measured for both Sn/37Pb and Sn/3.0Ag/0.5Cu by Moiré interferometry. The gratings are replicated on the chip and PCB separately and the V field is observed after the solder reflow.
2. A phase shifting filter is developed which enables accurate fringe counting in spite of high level of noises. The algorithm is effectively applied by discriminating the data from low and high frequency noises.
3. A new approach to measure residual warpage is proposed by thermally relaxing the specimen. The result is mutually verified with that of other methods.
4. Shadow Moiré setup which can resolve 5 μm/fringe sensitivity is developed by adopting fine pitch grating (200 lines/mm) with collimated laser beam.

5. Residual warpage values measured in this study are summarized in Table 1. The amount of residual warpage and stress induced during reflow process should be considered at early design stage. Proper control of residual warpage and stress through geometry, material, and process modification mentioned in this work can remarkably increase the reliability of flip-chip packages.

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