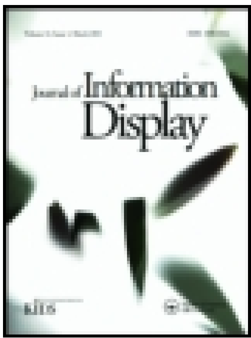

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Passivation layer effect on the positive bias temperature instability of molybdenum disulfide thin film transistors

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ABSTRACT

As two-dimensional (2D) materials have a large surface to volume ratio, the stability of thin film transistors (TFTs) is likely to be lowered with air exposure. Therefore, we study the positive bias temperature instability (PBTI) of chemical vapor deposition (CVD) grown molybdenum disulfide (MoS_2) TFTs before and after deposition of a passivation layer. The results of the PBTI study demonstrate that the fabricated devices adjust to the stretched-exponential model, which shows a threshold voltage shift attributed to the charge trapping mechanism. However, by depositing the passivation layer (Al_2O_3) that physically blocks the charge transfer process with O_2 and H_2O adsorbed to the surface of the MoS_2 channel, the threshold voltage shifted reduces from 10 V to 7.4 V under stress condition. The quantitative value of tau (τ), one of the fitting parameters of the stretched-exponential model, also decreases from 6453 s to 5153 s, resulting in improved device stability.

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Chemical vapor deposition; CVD-grown MoS_2; positive bias temperature instability; passivation layer effect; stretched-exponential model

1. Introduction

As emerging and commercial soft electronics with highly flexible property, two-dimensional (2D) materials such as graphene, transition metal dichalcogenides (TMDs), and hexagonal boron nitride (h-BN) have been considered as excellent materials for soft electronics. This is mainly due to their flexible physical properties as a consequence of their atomically thin and layer-by-layer stacked characteristics [1–3]. TMDs with the chemical formula of MX_2 (M = transition metal (e.g. Mo and W), X = chalcogen (e.g. S, Se, and Te)) have been in the spotlight for their superior electrical properties with appropriate bandgap size [4,5], high on/off current ratio [6,7], and high mobility [8–10]. When looking at the periodic table, several combinations of transition metals and chalcogens are possible, and various electrical properties such as semi metallic, superconducting, and semiconducting can be obtained based on proper combinations of transition metal and chalcogen [11]. Consequently, TMDs can be selected according to the purpose of their application. Among several combinations of transition metal and chalcogen, TMDs consisting of a transition metal in group 6 exhibit significant switching operations due to semiconducting properties with proper bandgap ($1 \sim 2$ eV). This composition makes them excellent channel materials for the next-generation display field. Various attempts have been performed to apply TMDs to next-generation displays. Mechanically exfoliated flakes were initially integrated with OLED, which showed potential as a display application [12,13]. A study on driving circuits for operating flexible OLED displays was also reported using MoS_2 thin films grown through powder-based chemical vapor deposition (CVD) [14]. More recently, a report demonstrating flexible OLEDs using a large-area thin film synthesized by metal–organic chemical vapor deposition (MOCVD) was reported [15]. The above studies proved that TMDs possess the electrical and mechanical properties required for OLED displays application, but the reliable performance of TMDs-based TFTs should also be considered for long-term operation. As a method for improving the stability of TFTs, research on gate insulator (GI) [16–18], passivation layer [19,20], and post-treatment processes [21–23] have been conducted. In the case of 2D materials, the ratio of surface to volume is extremely large, indicating that the interface property with the insulating film has a significant influence on the device properties. Particularly, when O_2 or H_2O contained in the air are adsorbed on the surface of

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TMDs, hysteresis occurs in the transfer curve due to the charge transfer phenomenon [24–26]. Therefore, in order to improve the stability of the TFTs, it is crucial to control the interface characteristics formed between the channel and insulator so various attempts have been performed to find an insulator suitable for TMDs. As is widely known, the use of high-k dielectric as a gate insulator (GI) is essential in boosting the electrical performance of MoS_2 TFTs (and other 2D materials using TFTs) due to its great gate modulation and effective charge screening [27,28]. Moreover, high-κ dielectrics deposited via atomic layer deposition (ALD) are also advantageous in industrial application compared with other passivation layer candidates such as a polymer. In this study, we sought to improve not only the electrical performance by suppressing the charged impurity scattering but also the stability by protecting the MoS_2 channel from O_2 or H_2O by adopting Al_2O_3 as the passivation layer [29–32]. After depositing Al_2O_3 as the passivation layer on the as-fabricated MoS_2 TFTs, the results confirm that stability in terms of the threshold voltage shift improves under the positive bias stress of 30 V at 60°C.

2. Results and discussion

In order to test the stability of TFTs with the MoS_2 channel, MoS_2 was synthesized using CVD based on powder precursors vaporization [33]. Sulfur (Sigma Aldrich, 99.98%) and MoO_3 (Sigma Aldrich, $\geq$ 99.5%) powders were loaded into alumina crucibles, and growth substrates were placed face down on a crucible containing MoO_3 powders. Crucibles containing sulfur and MoO_3 powders were separately placed up-stream and down-stream in a tube furnace, and the vaporization temperature was set to 320°C and 830°C, respectively. Ar gas measuring 100 sccm with inert property was introduced into the tube furnace as a carrier gas. The CVD process pressure was performed in an atmospheric environment of 750 torr to precisely control the vaporized pressure of the solid powders. The optical microscopy (OM) image in Figure 1(a) shows the as-grown MoS_2 domain and thin film. From the domain evolution point of view, the shape evolution of MoS_2 proceeds from a hexagonal shape to triangular shape under the chemical potential for the edge formation [34,35]. Finally, the synthesized MoS_2 domain shows a triangular shape of tens of micrometers in length on each side, indicating that high-quality MoS_2 was synthesized. The number of layers of MoS_2 with a layer stacked structure can be determined easily through spectroscopic analysis such as Raman spectroscopy [36]. Raman spectroscopy using a laser with 532 nm wavelength was used to characterize the number of layers of MoS_2 film. As shown in Figure 1(b), the vibration peak (E^1_{2g}) in the in-plane direction appears

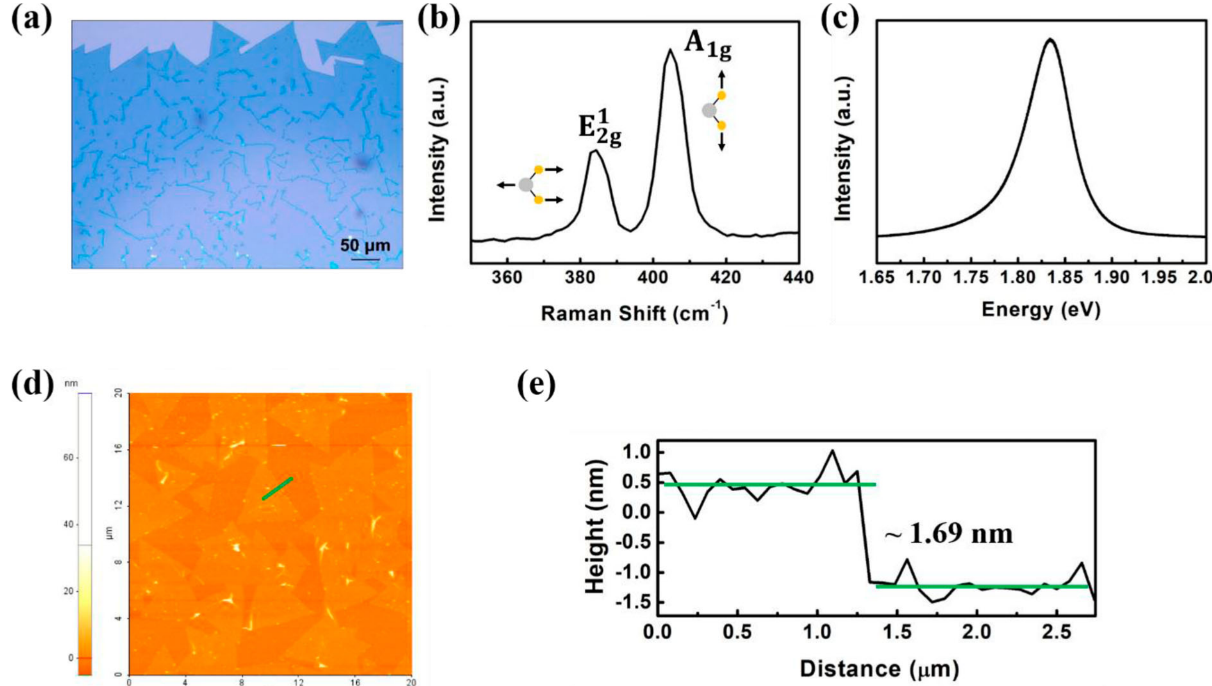

Figure 1. (a) Optical microscopy (OM) images of powder vaporization based CVD-grown MoS_2 thin film. (b) Raman and (c) photoluminescence (PL) spectrum acquired from the MoS_2 thin film region. (d) Atomic force microscopy (AFM) image of a single crystalline MoS_2 domain with a triangular shape in the region of 20 by 20 µm^2. (e) Height profile of the crystalline MoS_2 domain marked by a green line in (d).

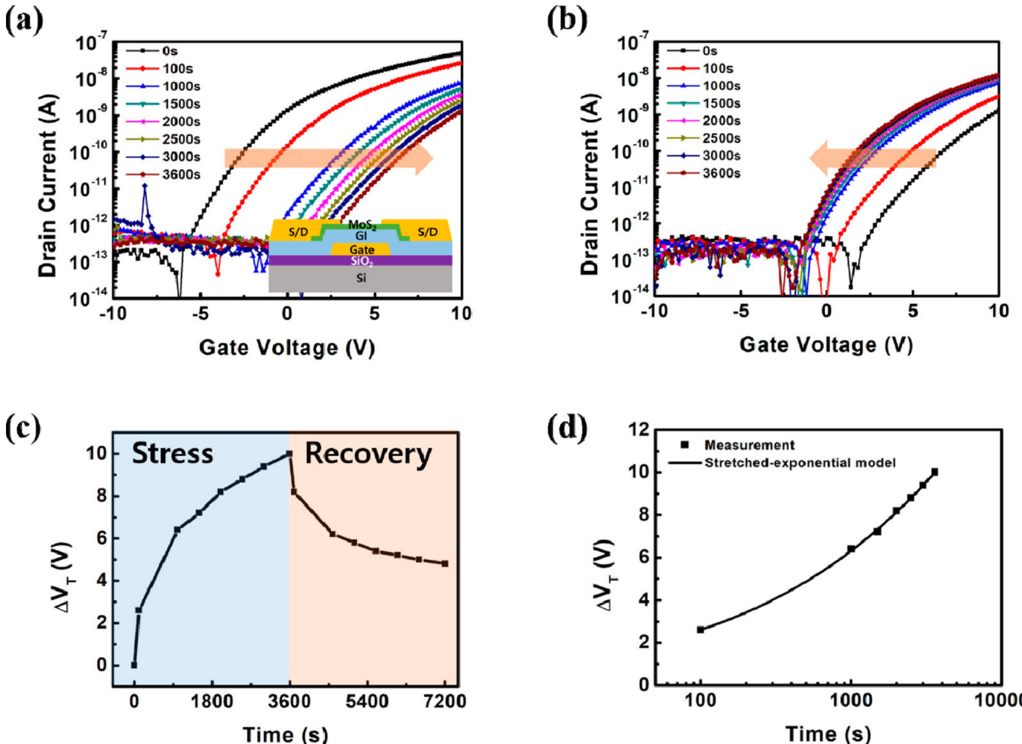

Figure 2. (a, b) Transfer curves of MoS_2 TFTs without passivation layer as a function of (a) stress time and (b) recovery time. (c) Time-dependent threshold voltage shift in stress and recovery phases. (d) Measured data of threshold voltage depending on the stress time suitable with the fitting line of the stretched-exponential model.

in the 384.4 cm^{-1}, and another vibration peak (A_{1g}) in the out-of-plane direction appears in the 404.7 cm^{-1}. As the distance between two characteristic Raman peaks is 20.3 cm^{-1}, the number of layers of MoS_2 thin film is expected to be approximately two. The bandgap of the as-grown MoS_2 thin film can be also identified by photoluminescence (PL) spectroscopic analysis. The result of PL measurement shows that the as-grown MoS_2 thin film has a bandgap of approximately 1.83 eV. In addition to spectroscopic analysis, atomic force microscopy (AFM) can provide more accurate information about the number of layers (Figure 1(d)). AFM measurement was performed over a wide area of $20 \times 20\ \mu m^2$, and the measured thickness of MoS_2 was about 1.69 nm as shown in Figure 1(e). It can be seen that the thickness information is exactly the same as that obtained through the Raman spectroscopic analysis.

Although MoS_2 is successfully synthesized and characterized, one-step is required to enable MoS_2 film to be used in device applications. As the MoS_2 synthesized using powder precursors is prepared at relatively high temperatures, the as-grown MoS_2 has a tensile strain after completion of growth due to the difference in the thermal expansion coefficient with the substrate [37,38]. Therefore, to obtain an improved device performance, the tensile strain must be eliminated, which can be achieved through the transfer process. In this study, a polystyrene (PS) solution was spin-coated on the as-grown MoS_2 as a supporting film, followed by separating PS/MoS_2 stack from the substrate using the surface energy difference [39]. In order to fabricate MoS_2 TFTs with a bottom-gate staggered structure, Cr/Au/Pd with thickness of 10/50/40 nm was thermally deposited onto SiO_2/Si substrate as a gate electrode. Subsequently, the plasma enhanced chemical vapor deposition (PECVD) was used to deposit SiO_2 with thickness of 200 nm as a GI. Transfer of the PS-coated MoS_2 onto the prepared substrate was followed by PS removal using toluene. In order to obtain ohmic contact property, Ti/Au (15/35 nm) was chosen as a source/drain electrode (Inset of Figure 1(a)). Under $V_{DS} = 0.1$ V condition, the MoS_2 TFTs with a bottom-gate staggered structure showed a high on/off current ratio of $\sim 10^6$ and field effect mobility of 5.6 $cm^2V^{-1}s^{-1}$ in the linear regime, which was calculated using Equation (1).

$$\mu = g_m \frac{L}{C_{ox} \cdot W \cdot V_{DS}} \tag{1}$$

Considering the gate bias sweep range of −20 to 20V and the temperature range for OLED operation, the stress conditions of gate bias and temperature were set to severe at 30 V and 60°C for 3600 s. As shown in Figure 2(a),

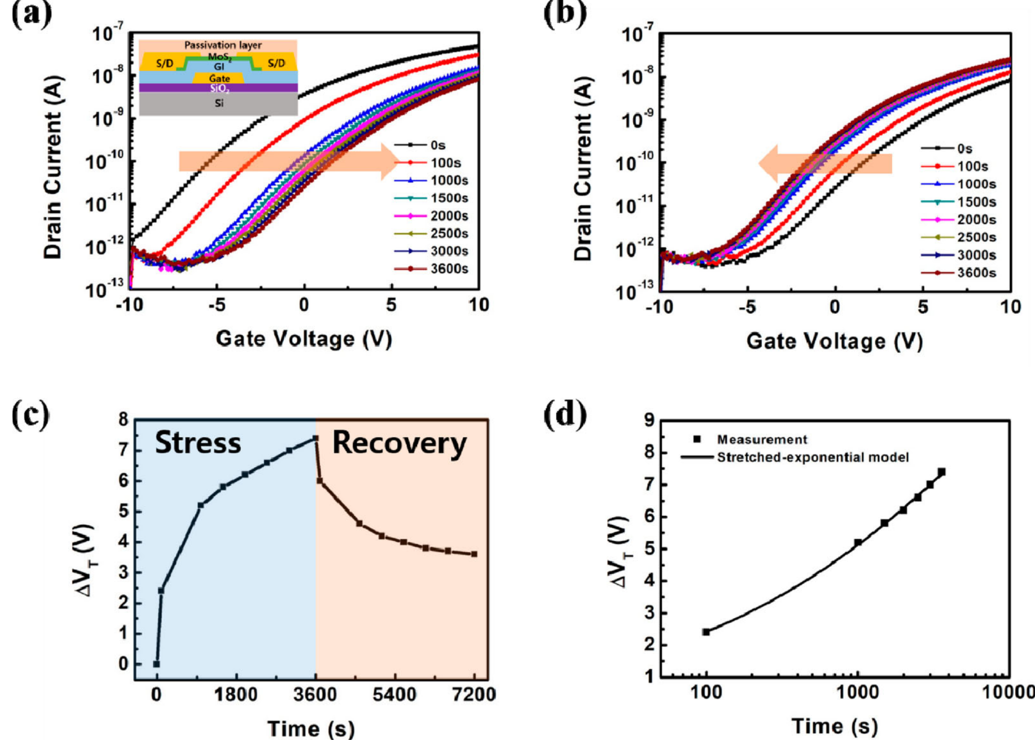

Figure 3. (a, b) Transfer curves of MoS_2 TFTs with passivation layer as a function of (a) stress time and (b) recovery time. (c) Time dependent threshold voltage shift in stress and recovery phases. (d) Measured data of the threshold voltage depending on the stress time suitable with the fitting line of the stretched-exponential model.

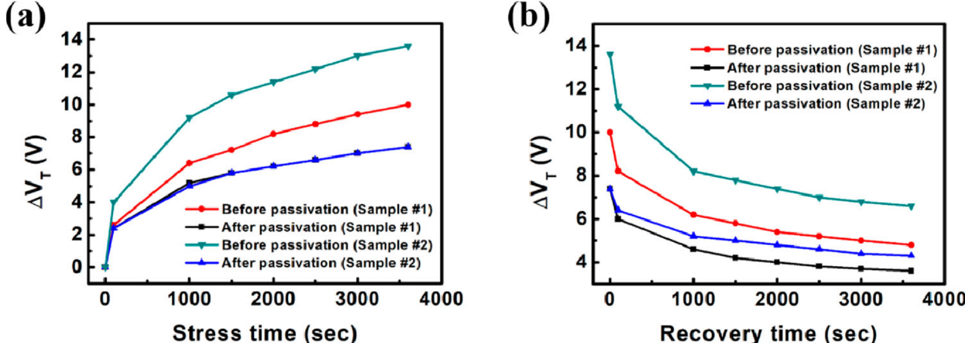

Figure 4. (a, b) Threshold voltage shift of different MoS_2 device samples as a function of (a) stress time and (b) recovery time.

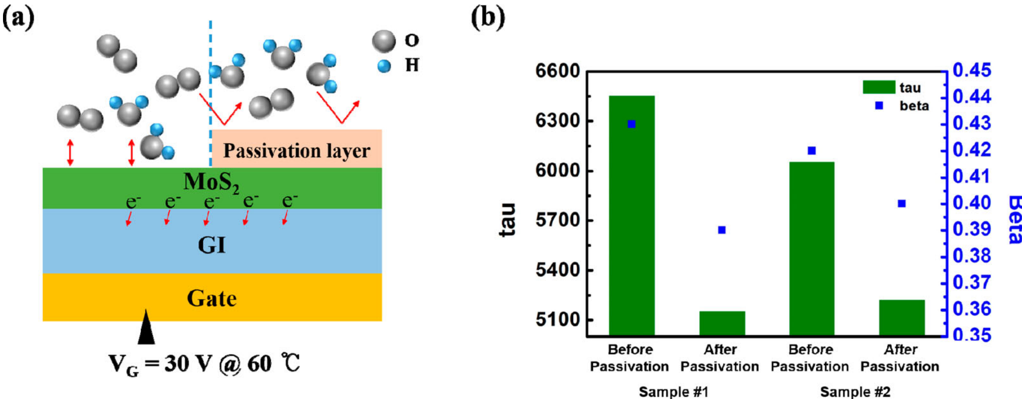

Figure 5. (a) Schematic illustration of the effect of passivation layer against O_2 and H_2O. (b) Quantitative comparison of the characteristic fitting parameters of MoS_2 TFTs before and after passivation layer deposition.

under the gate bias stress of 30 V at 60°C, the transfer curves were measured at $V_{DS} = 0.1$ V when 0, 100, 1000, 1500, 2000, 2500, 3000, and 3600 s, and threshold voltages were extracted from each transfer curves at a constant current level of 10^{-9} A. As the stress time increases, the threshold voltage positively shifts from −0.4 V to 9.6 V because electrons are trapped into the GI or interface between the GI and MoS_2 when a positive bias stress is applied. If the bias stress applied to the gate is stopped, the recovery response wherein the threshold voltage negatively shifts can be measured. In this study, the recovery time was set to 3600 s in the same manner as in the stress situation, and temperature was also maintained at 60°C under the gate bias stress of 0 V. As the recovery time increases to 3600 s, threshold voltage negatively shifts from 9.6 V to 4.4 V due to the electron de-trapping mechanism from GI or interface (Figure 2(b)). During the same time scale of 3600 s, the threshold voltage shifts are not consistent during the stress and recovery phases as shown in Figure 2(c). When bias stress of 30 V at 60°C was applied for 3600 s, the threshold voltage shifted by 10 V, and only a −5.2 V shift was exhibited during the recovery phase. According to these results, a difference in time when the electron is trapped and de-trapped exists. The time dependence of the relative value of the shifted threshold voltage was usually used to confirm which mechanism is dominant under a bias stress situation. It can be seen that the relative value of the shifted threshold voltage derived from the applied stress for 3600 s agrees with the following stretched-exponential model.

$$\Delta V_T = \Delta V_{T0}\left\{1 - \exp\left[-\left(\frac{t}{\tau}\right)\right]^{\beta}\right\} \tag{2}$$

where ΔV_{T0} is ΔV_T at infinite time, τ is the carriers characteristic trapping time, β represents the stretched-exponential exponent, and t is the bias stress time duration. The stretched-exponential model was used to represent the charge trapping mechanism of a-Si TFTs [40]. In the case of MoS_2 TFTs, the measured values fit well with the fitting line of the model, as shown in Figure 2(d), indicating that the trapped carrier in the GI or interface causes the instability measured in the positive bias of 30 V at 60°C.

2D materials such as MoS_2 have a large surface to volume ratio due to their atomically thin property. Because of this property, the treatment of basal plane plays an important role in the TFTs performance as the surface properties usually determine the overall properties of the 2D materials. In the case of MoS_2 TFTs, hysteresis in the transfer curve is usually observed due to the charge transfer process between the adsorbed O_2/H_2O and the MoS_2 channel [26,41], which also results in degradation of the subthreshold swing. The charge transfer occurring on the surface of the MoS_2 channel can also affect the stability of the device. Therefore, in order to block the contact between the MoS_2 channel and the air, Al_2O_3 with thickness of 30 nm was deposited as a passivation layer by atomic layer deposition (ALD) (inset of Figure 3 (a)), and PBTI test was conducted under the same conditions. As shown in Figure 3(a) and (b), the threshold voltage positively shifts from −2.2 V to 5.2 V in the stress phase and recovers to 1.4 V after another 3600 s. Relative shifts in threshold voltage during the stress and recovery phases are 7.4 V and −3.8 V, respectively (Figure 3 (c)). In the stress phase, measured values of the shifted threshold voltage match with the fitting line of the stretched-exponential model as Figure 3(d), indicating that the instability characteristic is also due to electron trapping in the GI or interface in the case of the passivation layer deposited MoS_2 TFTs.

Although the threshold voltage shift trend shows the same dependence on the presence or absence of the passivation layer, a difference in degree is seen as shown in Figure 4(a). In the case of Sample #1, the threshold voltage has a shift of 10 V during the bias stress of 30 V at 60°C for 3600 s, but the threshold voltage has a shift of 7.4 V after passivation. Similarly, in the case of Sample #2, a threshold voltage shift of 13.6 V is observed for the device without passivation during the applied stress period, and a threshold voltage shift of 7.4 V is observed after passivation. Although the degree of shift in the threshold voltage varies from device to device, it is common that the threshold voltage shift caused by positive bias temperature (PBT) stress is reduced after passivation. In terms of threshold voltage recovery, in the case of Sample #1, the threshold voltage recovery is of 5.2 V for the device without passivation, whereas a threshold voltage recovery of 3.8 V is observed after passivation. In the case of Sample #2, the threshold voltage recovery before and after passivation is 7 and 3.1 V, respectively (Figure 4(b)). When stress is applied to MoS_2 TFTs, the threshold voltage shift in the positive direction is reduced when the passivation layer is deposited. However, in the recovery phase, there is little or no passivation layer effect due to the electron de-trapping mechanism from the GI or interface.

O_2 and H_2O adsorbed on MoS_2 channel act as an electron acceptor [42], consequently affecting the electrical properties of MoS_2. In the absence of a passivation layer, as shown in Figure 5(a), O_2 and H_2O are easily adsorbed on the surface of the MoS_2 due to a positive gate bias of 60 V. These field-induced absorbents are

negatively charged by electrons acceptation from MoS_2 channel. In the absence of a passivation layer under positive bias stress at 60°C, negatively charged O_2 and H_2O on the surface of MoS_2 channel tend to make a positive threshold voltage shift more pronounced. If a passivation layer is present, it acts as a barrier that physically prevents O_2 and H_2O from adsorbing to the surface of MoS_2, resulting in a relatively reduced shift in the threshold voltage under stress conditions. This passivation layer effect can also be analyzed through quantitative numerical comparisons. In the stretched-exponential model of Equation (1), τ representing the characteristic trapping time of the carriers specifically refers to the time required to reach the equilibrium for the trapping and de-trapping process [43]. As shown in Figure 5(b), τ decreases after passivation layer deposition, because when the MoS_2 channel is exposed to air, the equilibrium rate of the trap and de-trap process is delayed due to O_2 and H_2O adsorbed on the MoS_2 surface. In the case of β, which stands for the width of the involved trap distribution, the value decreases after the passivation layer is deposited. However, since the variation of β is within 10%, the distribution of traps in the GI or interface is considered almost constant.

3. Conclusion

In summary, we synthesized MoS_2 thin film using the powder vaporization-based CVD method and fabricated TFTs with a bottom-gate staggered structure using PECVD SiO_2, which is widely used in the actual display industry as a GI. The instability behavior of the MoS_2 TFTs was measured before and after passivation layer deposition at the positive gate bias stress of 30 V at 60°C. In both cases, the charge trapping mechanism was shown to primarily cause instability because the shift in the threshold voltage over time was consistent with the stretched-exponential model fitting line. As the passivation layer physically blocks the MoS_2 channel from O_2 and H_2O, the stability of TFTs is improved, which can be confirmed through the behavior of the threshold voltage shift under stress situations. Moreover, the quantitative comparison of the fitting parameters used in the stretched-exponential model showed better stability after passivation layer deposition. Due to the characteristics of the 2D materials with a large surface to volume ratio, when exposed to the external environment, the electrical characteristics of the device are degraded upon contact with O_2 and H_2O, as these adversely affect the stability of the device. Therefore, it can be concluded that the use of passivation layer is essential in improving the stability of MoS_2 TFT.

4. Methods

4.1. MoS_2 synthesis and transfer

MoS_2 was synthesized in a four-inch tube furnace with two separate and independently controlled heating systems. MoO_3 (Sigma Aldrich, $\geq 99.5\%$) and sulfur (Sigma Aldrich, 99.98%) powders were used as precursors for MoS_2 and were loaded in alumina crucibles. MoO_3 and sulfur were vaporized at 830°C and 320°C for 30 min, respectively. Inert Ar gas measuring 100 sccm was introduced in the tube furnace as a carrier gas in order to transport the vaporized precursors. After finishing the synthesis of MoS_2 thin film using the CVD method, MoS_2 coated with PS supporting layer was transferred onto the prepared substrate, as described elsewhere and cited in 'Results and Discussion'

4.2. Electrical property characterization

All devices were annealed at 150–200°C for 2 h under vacuum ($\sim 10^{-2}$ Torr) to remove O_2 and H_2O adsorbed on the MoS_2 channel. A parameter analyzer (4200 SCS, Keithley Instruments) and probe station (MS-TECH) were used for PBTI, and all measurements were conducted under dark conditions.

Disclosure statement

No potential conflict of interest was reported by the author(s).

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References

[1] D. Akinwande, N. Petrone, and J. Hone, Nat. Commun. **5**, 5678 (2014).
[2] S. Das, R. Gulotty, A.V. Sumant, and A. Roelofs, Nano Lett. **14**, 2861–2866 (2014).
[3] L. Gao, Small **13**, 1603994 (2017).
[4] L. Debbichi, O. Eriksson, and S. Lebègue, Phys. Rev. B **89**, 205311 (2014).
[5] J. Jadczak, J. Kutrowska-Girzycka, P. Kapuściński, Y. Huang, A. Wójs, and L. Bryja, Nanotechnology **28**, 395702 (2017).
[6] H. Wang, L. Yu, Y.-H. Lee, Y. Shi, A. Hsu, M.L. Chin, L.-J. Li, M. Dubey, J. Kong, and T. Palacios, Nano Lett. **12**, 4674–4680 (2012).
[7] X. Liu, Y. Chai, and Z. Liu, Nanotechnology **28**, 164004 (2017).
[8] H.-J. Chuang, X. Tan, N.J. Ghimire, M.M. Perera, B. Chamlagain, M.M.-C. Cheng, J. Yan, D. Mandrus, D. Tománek, and Z. Zhou, Nano Lett. **14**, 3594–3601 (2014).
[9] D. Ovchinnikov, A. Allain, Y.-S. Huang, D. Dumcenco, and A. Kis, ACS Nano **8**, 8174–8181 (2014).
[10] H. Yang, C. Li, L. Yue, C. Wen, J. Zhang, and D. Wu, IEEE Electron Device Lett. **40**, 1116–1119 (2019).
[11] M. Chhowalla, H.S. Shin, G. Eda, L.-J. Li, K.P. Loh, and H. Zhang, Nat. Chem. **5**, 263 (2013).
[12] J.S. Kim, P.J. Jeon, J. Lee, K. Choi, H.S. Lee, Y. Cho, Y.T. Lee, D.K. Hwang, and S. Im, Nano Lett. **15**, 5778–5783 (2015).
[13] S. Yu, J.S. Kim, P.J. Jeon, J. Ahn, J.C. Park, and S. Im, Adv. Funct. Mater. **27**, 1603682 (2017).
[14] Y. Woo, W. Hong, S.Y. Yang, H.J. Kim, J.H. Cha, J.E. Lee, K.J. Lee, T. Kang, and S.-Y. Choi, Adv. Electron. Mater. **4**, 1800251 (2018).
[15] M. Choi, Y.J. Park, B.K. Sharma, S.-R. Bae, S.Y. Kim, and J.-H. Ahn, Sci. Adv. **4**, eaas8721 (2018).
[16] K.H. Ji, J.-I. Kim, Y.-G. Mo, J.H. Jeong, S. Yang, C.-S. Hwang, S.-H.K. Park, M.-K. Ryu, S.-Y. Lee, and J.K. Jeong, IEEE Electron Device Lett. **31**, 1404–1406 (2010).
[17] R. Cross, M.M. De Souza, S.C. Deane, and N.D. Young, IEEE Trans. Electron Devices **55**, 1109–1115 (2008).
[18] H.H. Hsieh, C.H. Wu, C.W. Chien, C.K. Chen, C.S. Yang, and C.C. Wu, J. Soc. Inf. Disp. **18**, 796–801 (2010).
[19] J.K. Jeong, H. Won Yang, J.H. Jeong, Y.-G. Mo, and H.D. Kim, Appl. Phys. Lett. **93**, 123508 (2008).
[20] P.-T. Liu, C.-H. Chang, and C.-S. Fuh, RSC Adv. **6**, 106374–106379 (2016).
[21] J.H. Song, N. Oh, B. Du Anh, H.D. Kim, and J.K. Jeong, IEEE Trans. Electron Devices **63**, 1054–1058 (2016).
[22] M.-H. Kim, M.-J. Choi, K. Kimura, H. Kobayashi, and D.-K. Choi, Solid-State Electron. **126**, 87–91 (2016).
[23] C.-L. Fan, F.-P. Tseng, and C.-Y. Tseng, Materials **11**, 824 (2018).
[24] F. Urban, F. Giubileo, A. Grillo, L. Iemmo, G. Luongo, M. Passacantando, T. Foller, L. Madauß, E. Pollmann, and M.P. Geller, 2D Mater. **6**, 045049 (2019).
[25] C. Lee, S. Rathi, M.A. Khan, D. Lim, Y. Kim, S.J. Yun, D.-H. Youn, K. Watanabe, T. Taniguchi, and G.-H. Kim, Nanotechnology **29**, 335202 (2018).
[26] A. Di Bartolomeo, L. Genovese, F. Giubileo, L. Iemmo, G. Luongo, T. Foller, and M. Schleberger, 2D Mater. **5**, 015014 (2017).
[27] H.-Y. Chang, S. Yang, J. Lee, L. Tao, W.-S. Hwang, D. Jena, N. Lu, and D. Akinwande, ACS Nano **7**, 5446–5452 (2013).
[28] K.L. Ganapathi, S. Bhattacharjee, S. Mohan, and N. Bhat, IEEE Electron Device Lett. **37**, 797–800 (2016).
[29] S.Y. Kim, S. Park, and W. Choi, Appl. Phys. Lett. **109**, 152101 (2016).
[30] H.A. Lee, S.Y. Kim, J. Kim, and W. Choi, J. Phys. D: Appl. Phys. **50**, 094001 (2017).
[31] S.-P. Ko, J.M. Shin, H.K. Jang, M.Y. You, J.-E. Jin, M. Choi, J. Cho, and G.-T. Kim, Nanotechnology **29**, 065703 (2018).
[32] J.H. Ryu, Y.G. You, S.W. Kim, J.H. Hong, J.H. Na, and S.H. Jhang, Curr. Appl. Phys. **20**, 363–365 (2020).
[33] Y.H. Lee, X.Q. Zhang, W. Zhang, M.T. Chang, C.T. Lin, K.D. Chang, Y.C. Yu, J.T.W. Wang, C.S. Chang, and L.J. Li, Adv. Mater. **24**, 2320–2325 (2012).
[34] S. Wang, Y. Rong, Y. Fan, M. Pacios, H. Bhaskaran, K. He, and J.H. Warner, Chem. Mater. **26**, 6371–6379 (2014).
[35] D. Cao, T. Shen, P. Liang, X. Chen, and H. Shu, J. Phys. Chem. C **119**, 4294–4301 (2015).
[36] H. Li, Q. Zhang, C.C.R. Yap, B.K. Tay, T.H.T. Edwin, A. Olivier, and D. Baillargeat, Adv. Funct. Mater. **22**, 1385–1390 (2012).
[37] Z. Liu, M. Amani, S. Najmaei, Q. Xu, X. Zou, W. Zhou, T. Yu, C. Qiu, A.G. Birdwell, and F.J. Crowne, Nat. Commun. **5**, 5246 (2014).
[38] M. Amani, M.L. Chin, A.L. Mazzoni, R.A. Burke, S. Najmaei, P.M. Ajayan, J. Lou, and M. Dubey, Appl. Phys. Lett. **104**, 203506 (2014).
[39] A. Gurarslan, Y. Yu, L. Su, Y. Yu, F. Suarez, S. Yao, Y. Zhu, M. Ozturk, Y. Zhang, and L. Cao, ACS Nano **8**, 11522–11528 (2014).
[40] F. Libsch and J. Kanicki, Appl. Phys. Lett. **62**, 1286–1288 (1993).
[41] D.J. Late, B. Liu, H.R. Matte, V.P. Dravid, and C. Rao, ACS Nano **6**, 5635–5641 (2012).
[42] Q. Yue, Z. Shao, S. Chang, and J. Li, Nanoscale Res. Lett. **8**, 425 (2013).
[43] H. Park, I.-J. Park, D.Y. Jung, K.J. Lee, S.Y. Yang, and S.-Y. Choi, 2D Mater. **3**, 021003 (2016).