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Noise analysis of replica driving technique and its verification to 12-bit 200 MS/s pipelined ADC

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Abstract: This study demonstrates the noise analysis of a replica driving MDAC architecture, which is verified by implementing a 12-bit 200 MS/s replica driving pipelined analogue-to-digital converter (ADC). Based on the noise design strategy with the target effective number of bits = 10.5-bit, the overall dynamic performance degradation by KT/C noise and thermal noise by an amplifier is alleviated by removing the front-end sample-and-hold (S/H) circuit, and the transconductance (g_m) of the inner source follower is maximised by increasing the current and threshold voltage (V_T) reduction. Replica input sampling networks are designed for the first-stage sub-ADC and the first-stage MDAC with different aspect ratios to minimise the sampling skew for the S/H-less architecture. A prototype 12-bit 200 MS/s ADC is fabricated in a 65 nm complementary metal oxide semiconductor. The measured spurious-free dynamic range (SFDR) and signal-to-noise distortion ratio (SNDR) at a 1.0 MHz input signal is 82.6 and 65.6 dB, respectively, and SFDR and SNDR at the Nyquist (=99.0 MHz) input are 77.3 and 58.6 dB, respectively. The ADC core and the reference driver consume 53.9 and 13.2 mW, respectively, at a 1.2 V supply voltage.

1 Introduction

The significance of a high-resolution, high-speed data converter for signal processing is increasing as various mobile applications emerge. Pipelined analogue-to-digital converters (ADCs) conduct analogue/digital conversion at high speed with low complexity by splitting the target resolution into multi-stages with sampling capability in each stage. Although the performance of traditional pipelined ADCs (resolution and speed) relies much on the performance of the operational amplifier (opamp) used for residue amplification, static power consumption becomes a major drawback in mobile applications. The majority of the reported studies so far have tried to save opamp power consumption with various strategies: switched opamp [1], opamp sharing [2], current reuse [3], comparator-based opamp replacement (comparator-based switched-capacitor, zero-crossing-based circuits) [4, 5], an open-loop amplifier [6], a ring amplifier [7], and load reduction [8]. The replica driving technique [9], which drives a heavy load in a power-efficient manner, has been proposed to alleviate the bandwidth limitation and the gain error by using an amplifier. As the load capacitor (C_L) of residue amplifiers increases for higher resolution, the effect of power saving by the load separation becomes dominant. Thus, applying the replica driving technique to high-resolution pipelined ADCs is an efficient solution. However, the noise of the amplifier, including the source follower (SF) in the replica driving scheme, may be a limitation for high-resolution applications. In this study, we quantitatively estimate the noise contribution by the SF in the replica driving technique and demonstrate a low-noise design strategy for the replica driving technique.

2 Noise analysis of the replica driving technique

The replica driving technique achieves high-speed operation with low-power consumption by separating accuracy and the C_L from the design point of view. Unlike in the conventional complementary metal oxide semiconductor (CMOS) amplifier, the SF in the replica driving technique is used as the output stage to replicate the output voltage of the amplifier. The signal swing limit due to the V_{GS} drop in the SF is resolved by a switched capacitor (SC) level shifter, i.e. the inner SF drives only the internal parasitic with high accuracy by the closed loop, while the open-loop replica SF drives a heavy real load fast. Although adopting an amplifier-based MDAC including the replica SF can achieve high resolution and high-speed operation, the thermal noise by the transistors including the SF and KT/C noise by the switches should be cautiously considered for the SC circuits. Especially the thermal noise can be an intrinsic limitation in design architecture and also causes rapid dynamic performance drop in high-precision applications.

In this study, a 12-bit 200 MS/s pipelined ADC which is one of the SC applications is determined to check the design validity of noise-analysis based replica driving technique. The specific design architecture of the pipelined ADC is firstly determined considering the design target [effective number of bits (ENOB) > 10.5-bit], which is calculated and verified by periodic NOISE (PNOISE) simulation. Based on the ADC architecture, sampling network related schemes are proposed (replicated sampling network, capacitor-splitting sampling network in sub-flash ADC and clock generator).

2.1 Noise analysis of replica driving MDAC

The analysis of the noise contribution is indispensable to achieve high signal-to-noise ratio performance for high-resolution ADCs. The noise of the replica driving technique is analysed based on a replica driving 12-bit pipelined ADC with a 3.5-bit/stage MDAC with the residue gain (G_{res}): 8 as the first stage, where the sample-and-hold (S/H) ($G_{res} = 1$) can be analysed in the same manner as the S/H-included architecture. To simplify the calculation in this study, the overall noise is analysed based on a 3.5-bit/stage MDAC as a representative. As the replica driving MDAC is controlled by two non-overlap clock phases (Q_1, Q_2), the input-referred first MDAC noise ($N_{1st\_MDAC,in}$) can be described as the sum of the noise power during the sampling phase (Q_1) and the amplifying phase (Q_2). Fig. 1*a* shows the noise sources during the sampling phase (Q_1). The power spectrum density (PSD) of the top switch and the bottom switch is expressed as $S_{n,top}(f)$ (=4kTR$_{sn,top}$) and $S_{n,bot}(f)$(=4kTR$_{sn,bot}$), respectively. The noise charge (Q_{vp}), which is frozen at the summing node (V_p), can be calculated resistance of

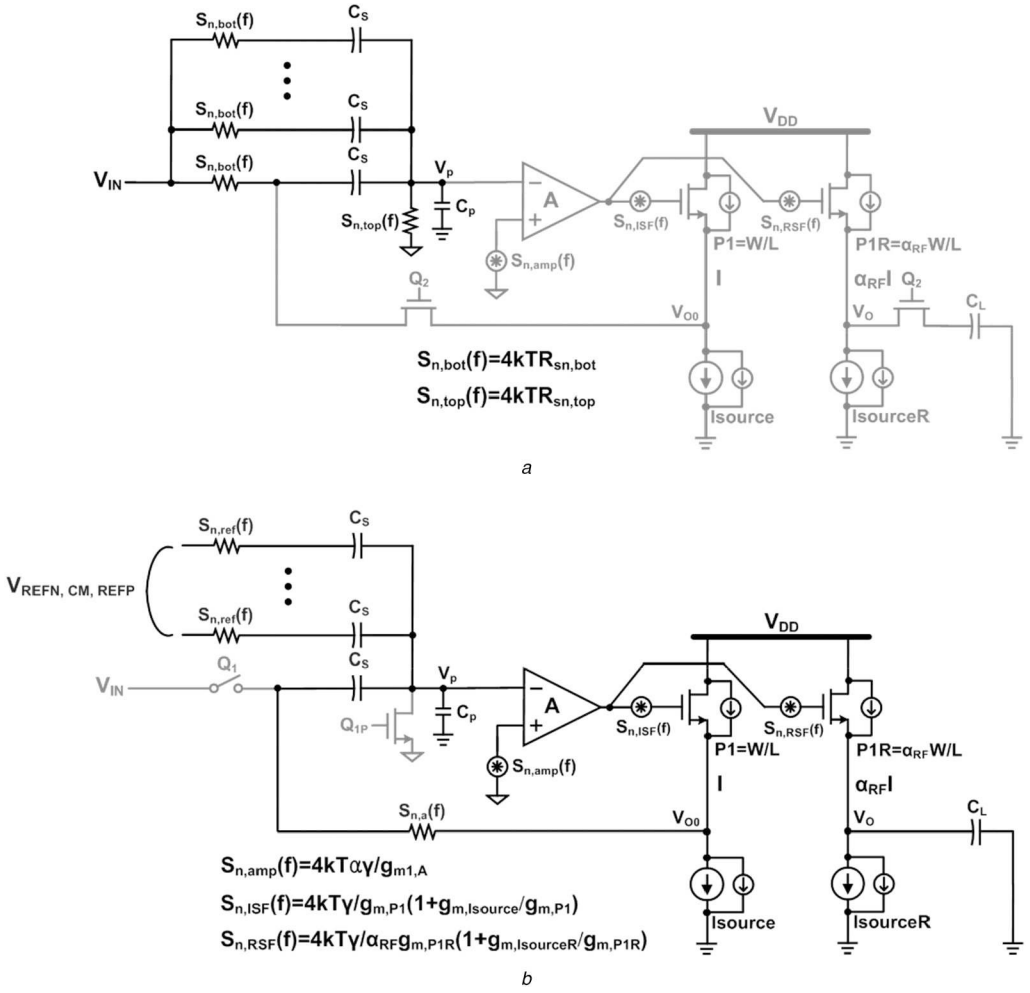

Fig. 1 *Noise of replica driving MDAC depending on sampling period (Q_1) and amplifying period (Q_2)*
(a) Sampling period: Q_1 = high, Q_2 = low, ***(b)*** Amplifying period: Q_1 = low, Q_2 = high

top (bottom) switch). $N_{\text{out,Q1}}$ is calculated by the equi-partition theorem for simplicity as shown in (1) [10] through the transfer function from each noise source (k: Boltzmann constant (=1.38 × 10^{-23}), T = 300 K, $R_{\text{sn,top(bot)}}$:

$$N_{\text{out,Q1}} = \left(\frac{8C_s + C_p}{C_s}\right)\frac{kT}{C_s} = \frac{1}{\beta_f}\frac{kT}{C_s}, \quad \beta_f = \frac{C_s}{8C_s + C_p} \tag{1}$$

Fig. 1*b* shows that the noise sources during the amplification phase (Q_2) can be expressed using the PSD of the reference switch (=4kT$R_{\text{sn,ref}}(f)$), the PSD of the amplifying switch (=4kT$R_{\text{sn,amp}}(f)$), the PSD of the amplifier noise (=$S_{\text{n,amp}}(f)$), the PSD of the inner SF (=$S_{\text{n,ISF}}(f)$) and the PSD of the replica SF (=$S_{\text{n,RSF}}(f)$). Note that the PSDs of the amplifying switch and that of the reference switch are not dominant sources compared to the other noise sources because the resistance of those switches generally has a much lower resistance than the limit of the resistor–capacitor (RC) time requirement for the fast reference settling. Thus, $N_{\text{out,Q2}}$ can be simplified as the sum of the noise power of the amplifier ($N_{\text{out,amp}}$) and that of the SFs ($N_{\text{out,SF}} = N_{\text{out,ISF}} + N_{\text{out,RSF}}$), as shown in (2), i.e. the replica driving design has additional noise contribution terms ($N_{\text{out,ISF}}$, $N_{\text{out,RSF}}$) compared to the conventional design. The ($g_{\text{m1,A(P1,Isource(IsourceR)}}$: g_m of the input transistor of two-stage amplifier (A), M_{P1}, the current source of the inner SF (replica SF)), α: the input referred noise ratio (=6.2 in the folded cascade amplifier), γ: the process coefficient (=1.6 in this process), α_{RF}: the replica factor)

$$N_{\text{out,Q2}} = N_{\text{out,amp}} + N_{\text{out,SF}} \cong \frac{1}{\beta_f}\frac{kT\gamma\alpha}{C_c} + \left\{\frac{kT\gamma}{g_{m,P1}}\frac{\beta_f g_{m1,A}}{C_c} + \frac{kT\gamma}{C_L}\right\} \tag{2}$$

$N_{\text{1st\_MDAC,out}}$ is expressed as the sum of $N_{\text{out,Q1}}$ and $N_{\text{out,Q2}}$ as shown in (3). $N_{\text{1st\_MDADC,in}}$ is expressed by dividing the $N_{\text{1st\_MDAC,output}}$ with the square of $G_{\text{1st\_MDAC}}$ (=8) as shown in (4). The $\alpha/(\beta_f C_c)$ in $N_{\text{out,amp}}$ is dominant compared to both $\beta_f g_{m1,A}/(g_{m,P1}C_c)$ in $N_{\text{out,ISF}}$ and $1/C_L$ in $N_{\text{out,RSF}}$, and the additional noise by the SFs can be further mitigated by increasing the g_m of the SFs. In the S/H design, the output-referred noise by hand-calculation is 907 μVrms and its value can be also verified by the PNOISE simulation, where the output-referred noise with a two-stage amplifier is 890 μVrms and that without a two-stage amplifier is 133 μVrms, respectively. In addition, as g_m of the two-stage amplifier increases maintaining the design target (loop-bandwidth and stability), the output-referred noise level gradually decreases as shown in Fig. 2, where the g_m ratio is defined as the normalised g_m with respect to the determined g_m considering the design target. Thus, the replica driving technique follows the same low-noise strategy as for the conventional amplifier design. It should be noted that the $N_{\text{1st\_MDADC,in}}$ in (4) cannot be reduced through a large C_S because the C_c and α also contribute to $N_{\text{1st\_MDADC,in}}$. Therefore, the noise of the amplifier can be minimised by increasing the g_m of the input transistor while reducing the g_m of the power rail transistors when C_c is determined considering power consumption and loop bandwidth

$$N_{\text{1st}_{\text{MDAC, out}}} = \frac{1}{\beta_f}\frac{kT}{C_s} + \left[\frac{1}{\beta_f}\frac{kT\gamma\alpha}{C_c} + \left\{\frac{kT\gamma}{g_{m,P1}}\frac{\beta_f g_{m1,A}}{C_c} + \frac{kT\gamma}{C_L}\right\}\right] \tag{3}$$

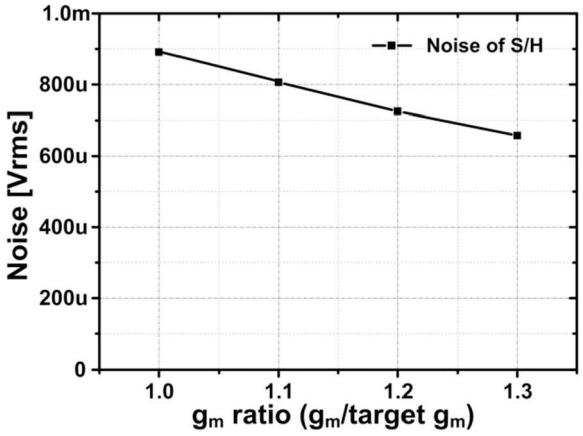

Fig. 2 *Output-referred noise of S/H depending on g_m ratio*

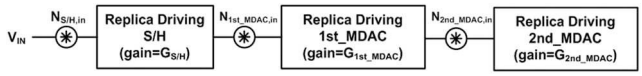

Fig. 3 *Noise modelling of replica driving pipelined ADC*

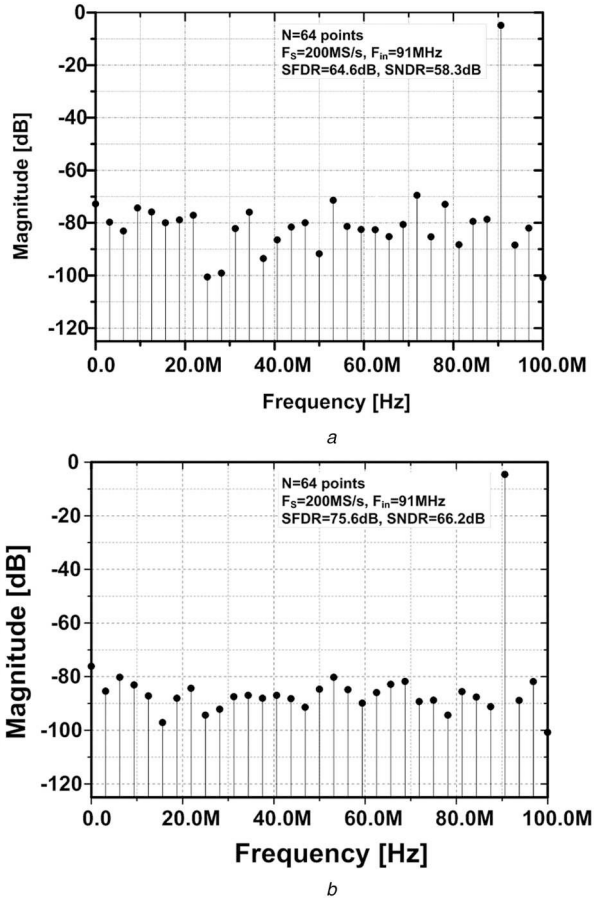

Fig. 4 *FFT results of 12-bit 200 MS/s replica driving pipelined ADC based on transient noise simulation*
(a) With S/H, ***(b)*** Without S/H

$$N_{1\text{st\_MDAC,in}} = \left(\frac{1}{\beta_f}\frac{kT}{C_s} + \left[\frac{1}{\beta_f}\frac{kT\gamma\alpha}{C_c} + \left\{\frac{kT\gamma}{g_{m,P1}}\frac{\beta_f g_{m1,A}}{C_c} + \frac{kT\gamma}{C_L}\right\}\right]\right) / \left(\frac{8C_s}{C_s}\right)^2 \quad (4)$$

2.2 Overall noise in replica driving pipelined ADC

Based on the above noise analysis, the noise effect is estimated from the overall configuration of the pipelined ADC with three stages (S/H, first MDAC, and second MDAC). The total noise of the ADC in [9] is represented by Fig. 3. $N_{S/H,in}$, $N_{1st\_MDAC,in}$, and $N_{2nd\_MDAC,in}$ are the input referred noise power of S/H, first MDAC, and second MDAC, respectively, while $G_{S/H}$ and $G_{1st/2nd\_MDAC}$ are the signal gain of S/H and the MDACs, respectively. The total input-referred noise power ($N_{total,in}$) of the proposed replica driving pipelined ADC is expressed as the following equation, which is known as the Friis formula for noise:

$$N_{total,in} = N_{S/H,in} + N_{1st_{MDAC},in}/(G_{S/H})^2 + N_{2nd_{MDAC},in}/(G_{S/H}G_{1st_{MDAC}})^2 \quad (5)$$

The input-referred noise of the second MDAC ($N_{2nd\_MDAC,in}$) is divided by the square of the signal gains (($G_{S/H}$ G_{1st_MDAC})^2), while that of the first MDAC ($N_{1st\_MDAC,in}$) is almost directly transferred to the input ($G_{S/H} = 1$). Therefore, the effect of $N_{2nd\_MDAC,in}$ is relatively small compared to $N_{S/H,in}$ and $N_{1st\_MDAC,in}$. Thus, we consider only $N_{S/H,in}$ and $N_{1st\_MDAC,in}$ to calculate the total input-referred noise ($N_{total,in}$). As the $N_{S/H,in}$ is higher than $N_{1st\_MDAC,in}$, the dominant noise is caused by the S/H, and this can also be verified by the transient noise simulation depending on S/H as shown in Fig. 4.

3 Circuit implementation

3.1 ADC architecture

We designed a prototype 12-bit 200 MS/s replica driving pipelined ADC on the basis of our study as described in the previous section. The prototype ADC has a 4-bit–5-bit–5-bit configuration with a heavy C_L as shown in Fig. 5, including the reference driver which does not include the external decoupling capacitor and the large internal capacitor for bias stabilisation to prevent ringing by the bond-wire inductance. Each sampling capacitor of the MDAC stages was determined considering KT/C noise and the capacitor mismatch of the process. In addition, when all parasitic capacitances were counted, including the input capacitor of the sub-ADCs, the net load capacitance (C_{Leff}) from each amplifier in the MDAC point of view was quite large ($C_{Leff\_1st\ MDAC} = 3.2$ pF and $C_{Leff\_2nd\ MDAC} = 1.2$ pF). Note that the power reduction capability of the proposed structure compared to the conventional amplifier became prominent as C_L increased. Moreover, as the S/H was removed based on the noise analysis, the signal-to-noise distortion ratio (SNDR) of the replica driving pipelined ADC was increased by ∼8 dB as shown in Fig. 4.

3.2 Sampling network design

Assume that the performance degradation by the timing skew between the MDAC and sub-flash ADC is negligible. The S/H-less design [11] that was applied to the prototype ADC has advantages in terms of the power efficiency and noise performance as the S/H causes the static current, non-linearity, and thermal noise. However, as the fast moving input signal is sampled at the same time in both the MDAC and the flash ADC in the conventional S/H-less design, the actual signal difference (ΔV) between the two input paths may be worse. Moreover, trimming the RC to match the RC delay can cause additional delay and design complexity. To minimise the sampling difference by the RC delay, the acceptable maximum RC delay mismatch (t_d), which is inversely proportional to the signal frequency, is 50 ps from (6). Thus, the RC delay is the dominant error source with a fast moving input signal

$$\Delta V \cong (dV_{in}/dt) \times t_d = A\omega_{in}t_d \le \frac{1}{2}\text{LSB} = \frac{1}{2}\frac{A}{2^4} \quad (6)$$

In most of the previous designs [12, 13], to minimise the sampling difference by the RC delay, the RC delay is controlled by trimming. However, the matching between two input paths can be degraded by the RC trimming as the signal frequency increases. Moreover, additional calibration circuitries [11] to compensate the

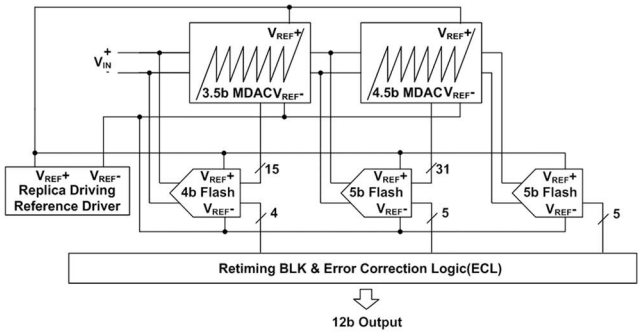

Fig. 5 *Overall configuration of 12-bit 200 MS/s replica driving pipelined ADC*

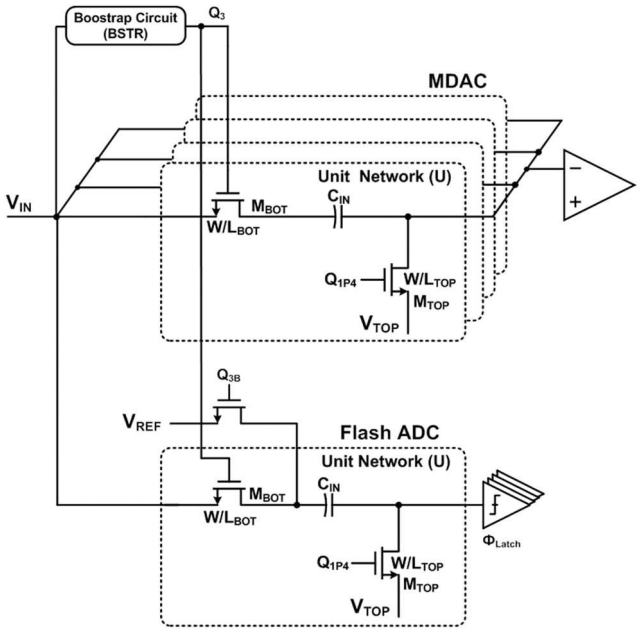

Fig. 6 *Replicated sampling network of first stage MDAC and flash ADC*

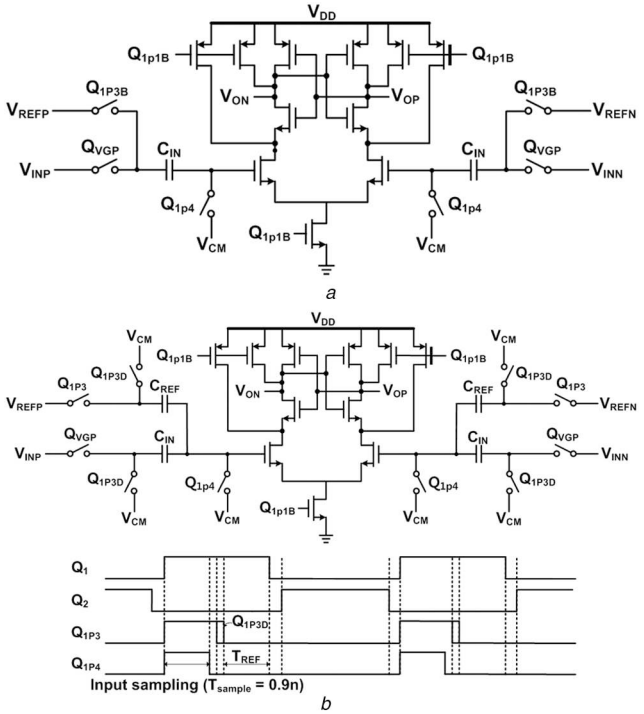

Fig. 7 *Sampling network of sub-flash ADC*
(a) Conventional scheme, ***(b)*** Capacitor-splitting scheme

RC delay difference between the MDAC and sub-flash ADC can cause hardware overhead and its efficiency is limited to specific conditions. Thereby, applying the S/H-less design in high-resolution ADCs is limited. To match the input sampling path in this design, a replica sampling network composed of the unit sampling capacitor C_{IN}, the top switch transistor (M_{TOP}) and the bottom switch transistor (M_{BOT}) was newly implemented as the basic cell shown in Fig. 6, while the dedicated sampling networks for the flash ADC and the MDAC were assigned in the conventional design. The input sampling network of the MDAC is composed of four replica unit sampling networks (U), and that of the flash ADC is composed of one replica unit sampling network (U). The bottom switch transistor (M_{BOT}) and the top switch transistor (M_{TOP}) in both the MDAC and the flash ADC are shared by the bootstrap circuit (BSTR) [14] and sampling clock (Q_{1P4}), respectively. Thus, the effect of the RC delay in both the sampling networks is almost the same without additional RC trimming circuits. As the estimated RC delay from the post-layout simulation is 4 ps, which is much lower that the requirement (=50 ps), the mismatch between the two input sampling networks is negligible.

3.3 Capacitor-splitting sampling network

The proposed front end of the flash ADC is composed of a strong-arm typed dynamic comparator with a proposed capacitor-splitting sampling network as shown in Fig. 7, where the dynamic compactor without a pre-amplifier is for low-power consumption and the capacitor-splitting sampling network is for alleviating the kick-back effect. In conventional sampling network with a dynamic comparator, a sampling capacitor (C_{IN}) is shared for both input signal and reference sampling. Thereby, the kick-back effect by the un-balanced impedance in the sampling network causes additional offset (3-σ: 21 mV in this design) [15], which limits the resolution assign in the pipelined ADC. To remove the additional offset in the proposed design, the additional capacitor (C_{REF}) for reference voltage is newly assigned. During the sampling phase (T_{sample}), the input signal ($V_{INP(N)}$) and the reference signal ($V_{REFP(N)}$) are sampled in C_{IN} and C_{REF}, respectively. When Q_{1P3D} is enabled, as both C_{IN} and C_{REF} are connected to V_{CM}, which means each effective impedance from the input pair to V_{CM} is the same, the kick-back effect due to the impedance mismatch is removed. Thus, the only offset of the dynamic comparator is considered for determining the resolution in the sub-flash ADC. The loading increase by the additional C_{REF} can be negligible. In addition, to secure the sampling clock which requires low jitter, faster (×2) external clock signal [16] is adopted instead of a complex phase generator which causes hardware complexity and additional power consumption.

3.4 Amplifier

The bandwidth of the amplifier increases as the CMOS process advances but the gain decreases due to the lowered output impedance. Thus, many circuit techniques based on amplifiers, such as correlated double sampling (CDS) [17], correlated level shifting (CLS) [18] and the three-stage amplifier, have been proposed to increase the gain. However, the increased number of phases and the complexity of the frequency compensation still limit the bandwidth. The proposed two-stage amplifier for high gain, as shown in Fig. 8, is composed of a gain-boosting folded-cascode amplifier as the first stage and a common-source amplifier as the second stage. The loop gain of the first stage MDAC ($G_{LP,replica}$) is 78 dB, which is 35 dB boosted by the gain-booster and is sufficiently higher than the required loop gain (=60.2 dB). As the input common level of the second stage amplifier is decreased to maximise the output swing range of the amplifier (A), the gate voltage of the cascade transistor ($M_{7(8)}$) and the V_{dsat} (V_{GS}–V_T) of the $M_{9(10)}$ are lowered. To mitigate the thermal noise effect by lowering the α in the amplifier, the V_{dsat} (V_{GS}–V_T) of the $M_{9(10)}$ and $M_{3(4)}$ are maximised within the allowable swing range and the g_m of the input pairs (M_1 and M_2) are maximised.

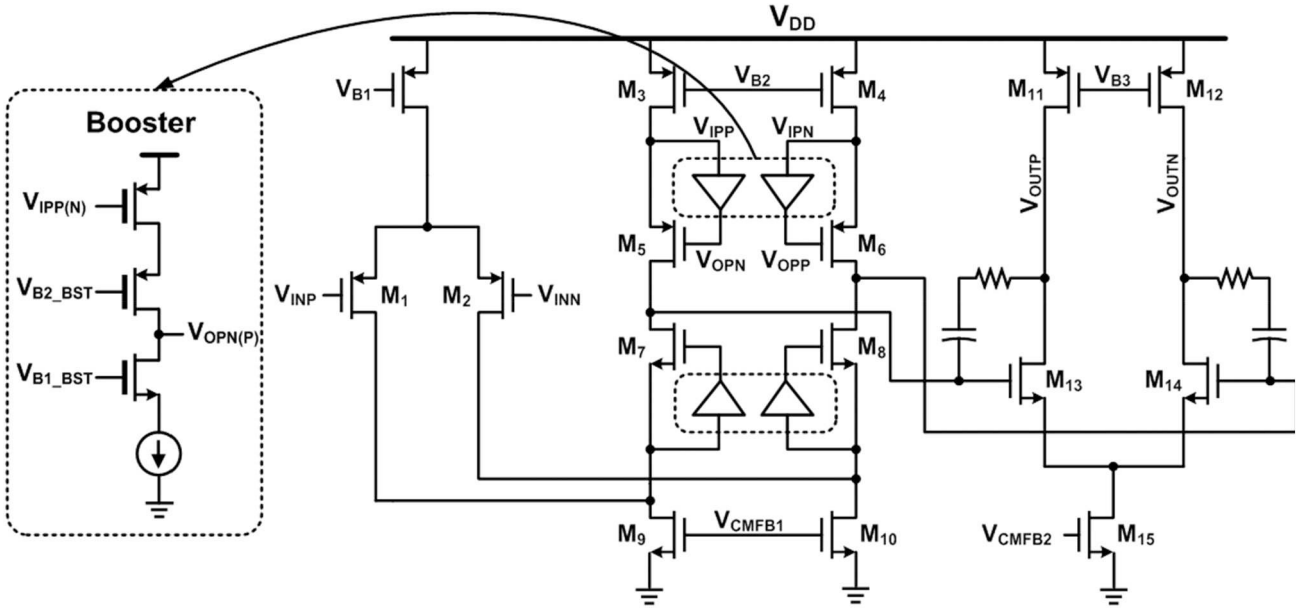

Fig. 8 *Two-stage amplifier (A) in replica driving MDAC with booster*

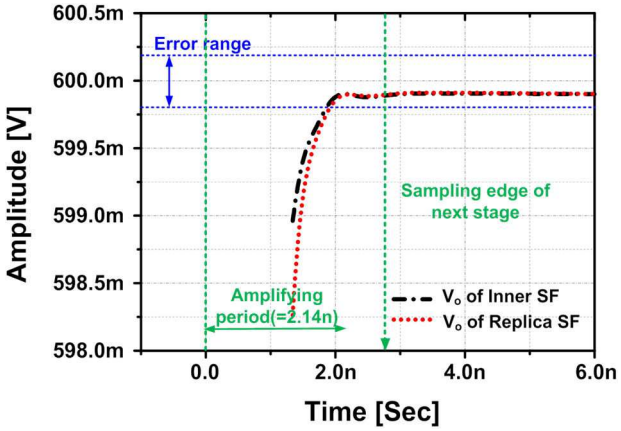

Fig. 9 *Settling of inner SF output (V_{O0}) and replica SF (V_O)*

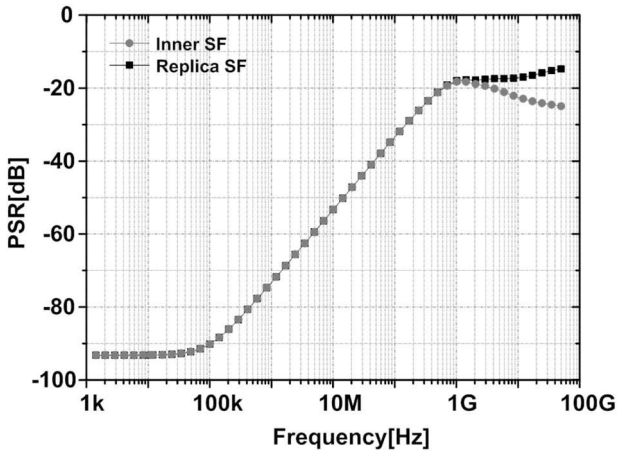

Fig. 10 *PSR of inner SF output (V_{O0}) and replica SF (V_O)*

3.5 Mismatch error of SFs

Here we discuss the settling behaviour, the offset and the linearity, which are caused by the mismatch in the implemented SFs: The output of the inner SF (V_{O0}) shows a fast settling behaviour with a parasitic load by the closed-loop manner as shown in Fig. 9, and the output of the replica SF (V_O) by the open-loop manner with the heavy C_L faithfully follows V_{O0}. The replica SF drives V_O with C_L (=3.2 pF) by $\alpha_{RF} = 2$ within the allowable error (=0.5 least

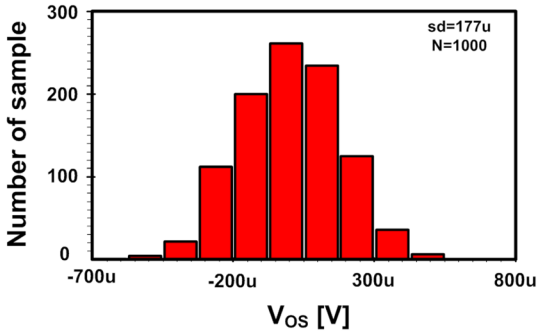

Fig. 11 *V_{OS} between inner SF output (V_{O0}) and replica SF (V_O)*

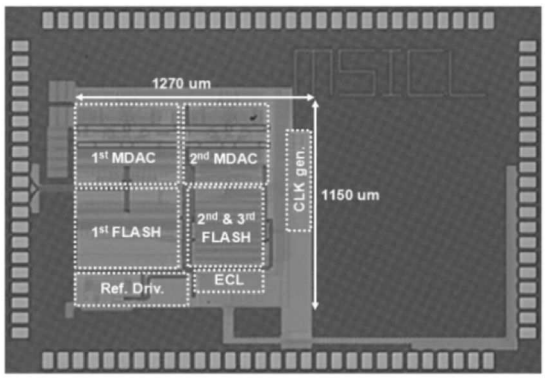

Fig. 12 *Chip photo*

significant bit (LSB) for 9-bit resolution in this case) before the amplifying period finishes (<2.14 ns for 200 MS/s). Indeed, as the simulated output of the replica SF (V_O) settles down to a 0.5 LSB error within 1.8 ns, the settling error is negligible. Moreover, the power supply rejection (PSR) simulations were conducted for both the inner (V_{O0}) and the replica (V_O) SFs as shown in Fig. 10. The two cases show identical behaviour up to 1 GHz. Thus, the difference between the two SFs caused by the disturbance from the external noise is negligible. In addition, the effect of the offset between SFs is negligible as both the SFs were designed to have a large transistor ($W/L = 200u/0.06u$) for high transconductance ($g_{m,Mn1}$), which guarantees that the pole ($=C_{p,1}/g_{m,Mn1}$) at the output of the inner SF (V_{O0}) is higher than the loop bandwidth ($=\beta_f C_c/g_{m,A1}$). Fig. 11 shows the offset result using a Monte–Carlo simulation between the inner SF (V_{O0}) and the replica SF (V_O). The

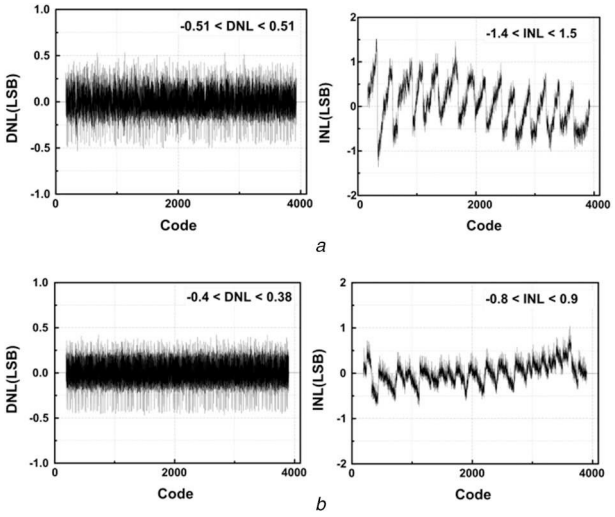

Fig. 13 *Measured differential non-linearity (DNL) and integral non-linearity (INL)*
(a) 200 MS/s, ***(b)*** 20 MS/s

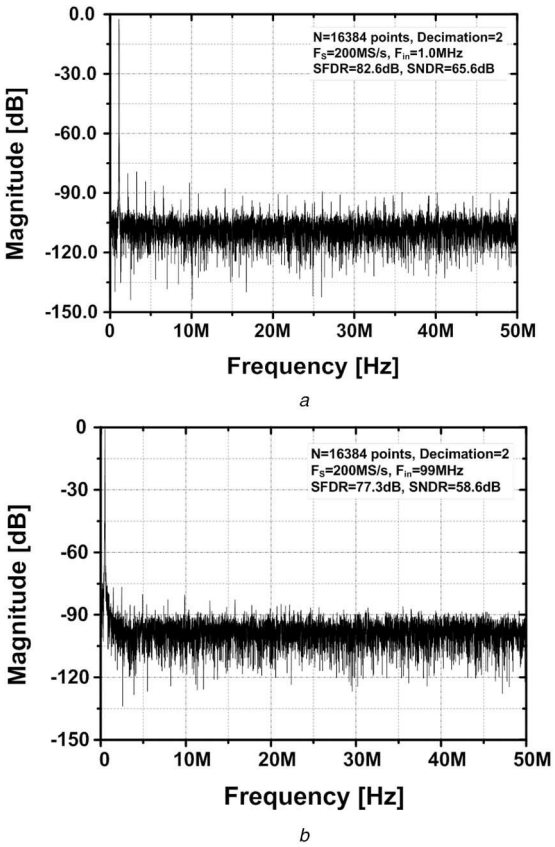

Fig. 14 *Measured FFT result at 200 MS/s with*
(a) 1.0 MHz input signal, ***(b)*** 99.0 MHz input signal

offsets of the dynamic latch, the first MDAC and the replica driving SF are 0.54, 8.07 and 16.5 mV (3-σ), which are corrected by the over-range (=38.5 mV) in the proposed design. Thus, the chance of the non-linearity is negligible.

3.6 Noise of S/H-less 12-bit 200 MS/s replica driving pipelined ADC

The total input-referred noise power ($N_{\text{total,in}}$) in this S/H-less replica driving pipelined ADC is expressed as (7). As the input-referred noise of the second MDAC ($N_{\text{2nd\_MDAC,in}}$) is divided by the square of the signal gains (($G_{\text{1st\_MDAC}}$)^2), the effect of $N_{\text{2nd\_MDAC,in}}$ is relatively small compared to $N_{\text{1st\_MDAC,in}}$. Thus, $N_{\text{total,in}}$ is dominantly determined by $N_{\text{1st\_MDAC,in}}$. To secure the

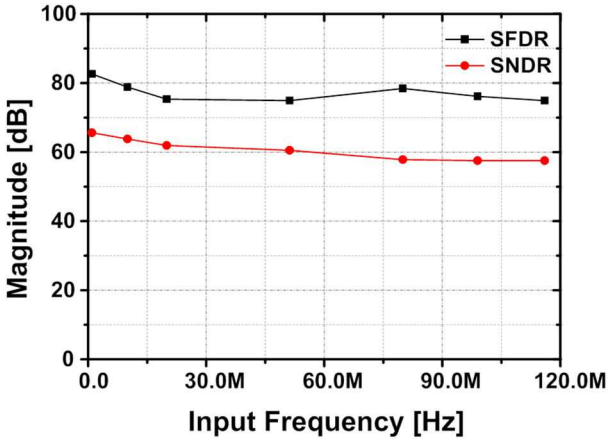

Fig. 15 *SNDR, SFDR versus input frequencies at 200 MS/s*

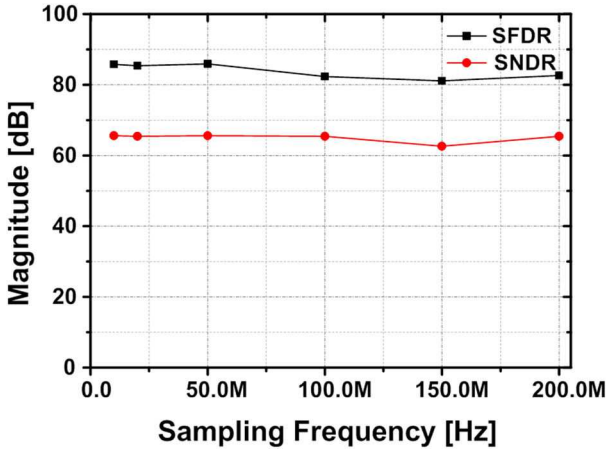

Fig. 16 *SNDR, SFDR versus sampling frequencies at 1 MHz input signal*

effective bits beyond 10.5 in this design, the total noise voltage (= $\sqrt{N_{\text{total,in}}}$) should be below 350 μVrms

$$N_{\text{total,in}} = N_{\text{1st\_MDAC,in}} + N_{\text{2nd\_MDAC,in}}/(G_{\text{1st\_MDAC}})^2 \quad (7)$$

The dynamic performance of the replica driving pipelined ADC can be estimated using the noise performance of the replica driving MDAC. The ADC calculated noise voltage (=125 μVrms) is similar to the PNOISE simulation result (=134 μVrms) and the most noise comes from the amplifier (A). The noises from the SF with an increased g_m in the replica technique do not cause a fundamental noise limit, and the low noise design strategy for the amplifier is quite the same as the conventional amplifier design. The noise power of the second MDAC can also be calculated by the same method, and its noise voltage (=$\sqrt{N_{\text{2nd\_MDAC,in}}}$) is 128.6 μVrms, which is also similar to the simulation result (=131.3 μVrms). The transient noise simulation was 66.2 dB SNDR and the noise analysis result was 68.5 dB SNDR.

4 Experimental results

The prototype 12-bit 200 MS/s replica driving S/H-less pipelined ADC was implemented in a CMOS 65 nm low power (LP) process. The ADC, including the reference drivers, occupied a 1.27 × 1.15 mm^2 active area; a chip photo is shown in Fig. 12. Figs. 13*a* and *b* show the measured DNL/INL at 200 and 20 MS/s, respectively. The saw-tooth shape in the INL (at 200 MS/s) was caused by the insufficient settling of the replica driving reference driver, while the measured INL of 20 MS/s, which is bilateral symmetry to that of 200 MS/s, was caused by the capacitor. The fast Fourier transform (FFT) spectra for low-frequency input (F_{IN} = 1.0 MHz) and Nyquist input (F_{IN} = 99 MHz) at 200 MS/s sampling-rate are shown in Fig. 14. The measured spurious-free dynamic range (SFDR) and SNDR at 1.0 MHz input signal are 82.6 and 65.6 dB,

	[19] Lin VLSI '14	[20] N. Dolev VLSI '13	[21] Shin JSSC '14	[22] Sehgal JSSC '15	[23] Sahoo JSSC '09	This Work
Architecture	Pipelined-SAR	Pipelined	ZCBC	Pipelined	Pipelined	Pipelined
Technology	65nm CMOS	65nm CMOS	55nm CMOS	45nm CMOS	90nm CMOS	65nm CMOS
Resolution	12b	12b	12b	12b	12b	12b
fs	210MS/s	200MS/s	200MS/s	195MS/s	200MS/s	200MS/s
Op-amp. based	X	X	X	O	O	O
Sampling cap.	2pF	N/A	N/A	4.4pF	4pF	4pF
Power Supply	1.0V	1.0V	1.1V	1.0V	1.2V	1.2V
SNDR	63.4dB	65dB	64.6dB	64.8dB	64dB	65.6dB
Size	0.48mm^2	0.26mm^2	0.282mm^2	0.81mm^2	1.36mm^2	1.52mm^2
Power	5.3mW	*11.5mW	28.5mW	*53mW	*348mW	67.1mW
FoM	30.3fJ/step	*92.8fJ/step	111fJ/step	*191.6fJ/step	*1.34pJ/step	216fJ/step

*excludes power consumption in reference buffers

Fig. 17 *Performance comparison (12-bit, 200 MS/s ADCs)*

Table 1 Performance summary of prototype ADC

process		65 nm CMOS
supply		1.2 V
resolution		12-bit
sampling rate		200 MS/s
negative reference voltage (VREFN)/ positive reference voltage (VREFP)		0.3 V/0.9 V
power	analogue	46.9 mW
	digital	7.0 mW
	ref. driv.	13.2 mW
total (w/o ref. driv.)		67.1 mW(53.9 mW)
DNL		−0.51–0.51 LSB
INL		−1.4–1.5 LSB
SFDR		82.6 dB@F_{IN} = 1.0 MHz
SNDR		65.6 dB@F_{IN} = 1.0 MHz
ENOB		10.6-bit (9.44-bit@Nyquist)
core area		1.52 mm^2
FoM		216 fJ/Conv-step

respectively, and the measured SFDR and SNDR at 99.0 MHz input signal are 77.3 and 58.6 dB, respectively. The measured SNDR and SFDR with respect to the input frequency at 200 MS/s are shown in Fig. 15. The rapid dynamic performance drop (SFDR/SNDR) was caused by the slow setting through the coupling effect by the layout pattern between the input signals to the summing node of the amplifier. The measured SNDR and SFDR with respect to the sampling frequency at F_{IN} = 1.0 MHz are shown in Fig. 16. The dynamic performance maintains an almost constant value irrespective of the sampling frequency. The ADC core and the reference driver consume 53.9 and 13.2 mW, respectively, under a 1.2 V supply voltage. The figure-of-merit (FoM) of the prototype ADC is 483 fJ/conv-step at a Nyquist signal frequency and 216 fJ/conv-step at a 1.0 MHz signal frequency. Fig. 17 shows the performance comparison (12-bit, 200 MS/s ADCs). Although the FoM of this design is somewhat higher than that of recently published ADCs, it shows the efficiency of the replica driving scheme in the opamp-based designs. The ADC performance is summarised in Table 1.

5 Conclusion

The noise of the replica driving technique was analysed and then the 12-bit 200 MS/s replica pipelined ADC was implemented based on the noise analysis to verify the feasibility of high resolution, high speed, and lower power consumption. The noise that was increased by the additional SFs in the replica driving technique was alleviated by increasing the g_m of the SF and its contribution to total noise was negligible compared to the amplifier. Thus, the replica driving technique followed the low noise design methodology for the conventional amplifier. Considering the feasibility of the high-resolution pipelined ADC, the amplifier is still an efficient method for accuracy, and the measured results show that the replica driving technique is applicable to high-precision SC applications with power efficient manner.

6 References

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