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A Comparative Study of the Curing Effects of Local and Global Thermal Annealing on a FinFET

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ABSTRACT Recently, localized thermal annealing has been spotlighted as an effective method to cure aged devices. The degraded gate oxide can be successfully cured by local annealing, which utilizes Joule heat inherently generated in the device. But, despite this advantage, there has been no study comparing the curing effects with various other annealing methods. In this study, the curing effects of local annealing and a conventional global annealing method applied to SOI FinFETs are compared. The measured electrical characteristics are discussed to evaluate the damage curing with respect to curing level and variability.

INDEX TERMS Damage curing, degradation, electrothermal annealing (ETA), FinFET, forming gas annealing (FGA), global annealing, hot-carrier injection (HCI), Joule heat, local annealing, reliability, SOI FinFET.

I. INTRODUCTION

Controlling gate oxide quality has been one of the most important challenges to improving device performance, reliability and yield. In particular, process-induced damages during device fabrication, such as plasma based deposition and etching, as well as the gate stacking process, can degrade the gate oxide quality [1]. To mitigate the abovementioned damages, thermal annealing with the aid of a forming gas such as hydrogen (H_2) or deuterium (D_2) diluted with nitrogen (N_2), which is called wafer-level (global) forming gas annealing (FGA), has been widely used. During annealing, the forming gas passivates the trap sites at the interface of the Si-SiO_2, reduces the trap density, and cures pre-existing damage. Such trap reduction and damage curing depends on the FGA process conditions, including the gas species (*e.g.*, H_2 or D_2), annealing temperature (T_{ANNL}) and annealing time (t_{ANNL}).

Recently, a transistor-level (local) annealing method known as electrothermal annealing (ETA), has emerged as an alternative to the conventional global annealing. The ETA mechanism is based on locally generated Joule heat induced by current flowing through a FET.

For example, the word-line current in a FET for flash memory [2], the current via dual-gate pads in a gate-all-around FET [3], the source-to-body current in a conventional 2-D planar FET [4]–[6] and punchthrough current in a floating body FET [7]–[8], have been utilized to generate the Joule heat to cure the gate oxide damage.

Compared to FGA, the speed of the ETA is very fast (less than ms), and the induced temperature can increase to over 900 °C. Moreover, the local ETA, simply abbreviated as ETA, has excellent annealing selectivity and can cure a targeted damaged FET which has experienced harsh operational stress. The curing effects depend on (i) current density as well as the time of Joule heat generation, (ii) a geometric structure used as the heatsink, and (iii) the material used to constitute the FET. The ETA is applicable to various devices, not just silicon based transistors [2]–[8], but also for thin-film transistors (TFTs) [9] and even 2-dimensional (2-D) transistors [10]–[12].

However, even though the ETA has advantages to improve the device performance and the reliability, there are two concerns. First, a comparison study between the emerging ETA and conventional thermal annealing with well-controlled experiments is necessary to understand the curing mechanism. For example, in our previous works [7], [13]–[15], we could not elucidate where the hydrogen comes from, i.e., whether it came from the atmosphere or diffused out from

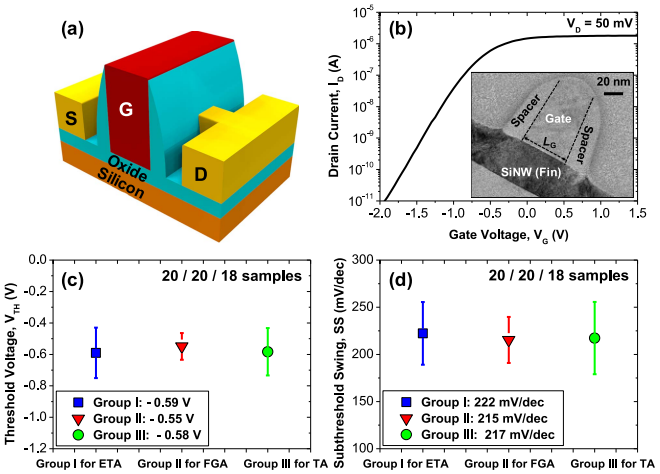

FIGURE 1. (a) A schematic of the FinFET. (b) Measured I_D-V_G characteristic of the pristine FinFET before the application of annealing and the HCI. (c)-(d) Extracted V_{TH} and *SS* of the initial FinFETs from each group. The values in the inset indicates the average V_{TH} and *SS* from each group.

the inside of the FETs. Second, the feasibility of ETA as an annealing method has been reported many times for various device structures such as gate-all-around (GAA) FET, FinFET, and planar FET [7]–[8], [13]–[15]. But, a quantitative study for fair comparison has not been done yet. Hence it is very timely to address the abovementioned concerns.

In this work, for the first time, we fairly compare the curing effects of ETA, FGA with H_2, and thermal annealing (TA) without H_2, which uses the same conditions but without H_2. Prior to comparing the characteristics of the FinFETs, pristine FinFETs were intentionally aged by hot-carrier injection (HCI). Then the aforementioned three annealing methods were applied to the aged FinFETs. Through this comparative study, the relative curing effects were quantitatively evaluated.

II. EXPERIMENTAL DETAILS

Tri-gate FinFETs were fabricated on a p-type (100) SOI wafer. The thickness of the buried oxide (BOX) was 400 nm, and the height of the fin (H_{Fin}) was 50 nm. After delineation of the silicon nanowire (SiNW), 5 nm of SiO_2 was thermally grown as a gate oxide, and n^+ poly-Si was deposited and patterned as a gate electrode. Finally, the conventional furnace based 1st FGA with H_2 was applied to all the devices before evaluating the three annealing methods. Details of the fabrication process flow, and additional transmission electron microscope (TEM) images for along the gate as well as along the channel and gate oxide thickness, have already been reported in our previous works [7], [16].

The nominal channel width (W_{Fin}) of the FinFET was 60 nm, the gate length (L_G) was 60 nm, and the gate spacer width (W_{Spacer}) was 30 nm. Fig. 1(a)-(b) shows the schematic and measured *I-V* characteristics of the fabricated FinFET. For fair comparison of the curing effects, 58 FinFETs were used to obtain similar device characteristics, specifically, the threshold voltage (V_{TH}) and

TABLE 1. Annealing conditions for curing of the gate oxide damage.

	Group I (ETA)	Group II (FGA with H_2)	Group III (TA without H_2)
V_G	Ground	Floating	
V_S	Ground		
V_D (V_{ETA})	4.2 V		
t_{ANNL}	0.1 ms	30 min	
T_{ANNL}	23 °C	410 °C	
Ambient	Air	$H_2 : N_2 = 1 : 9$	$H_2 : N_2 = 0 : 10$

subthreshold swing (*SS*), and were categorized into three groups. The first 20 devices were designated group I for the ETA, the second 20 devices were group II for the FGA with H_2, and the remaining 18 devices were group III for the thermal-only annealing without H_2, as shown in Fig. 1(c)-(d). The V_{TH} was extracted using the constant current method [17] at a low V_D of 50 mV, and the *SS* was extracted between the drain current at V_{TH} and that below two orders. All electrical measurements were performed with a parameter analyzer (HP 4156C) under air ambient at room temperature. HCI stress was applied to intentionally create the gate oxide damage at the condition of $V_G = 2$ V and $V_D = 4$ V for 100 sec. After that, the three abovementioned annealing methods were applied to each group. All annealing methods were immediately applied after the HCI without time delay. The detailed annealing conditions are summarized in Table 1.

We used the punchthrough current-induced Joule heat for the ETA [7]. At the optimal voltage (V_{ETA}) range for the ETA, the current was 83 μA, and the calculated power was 0.35 mW. The V_{ETA} of 4.2 V was an approximately optimal value, as was previously reported in our work [7], and corresponded to the range of 400 °C to 500 °C according to the simulations with the aid of TCAD (not shown). In more detail, when the V_{ETA} was increased, the device parameters such as V_{TH} and *SS* were cured to nearly the initial state. But, when it was above a critical V_{ETA} of 4.2 V, i.e., the induced temperature was too high, the cured V_{TH} and the *SS* became even worse than the initial value. Hence, a V_{ETA} of 4.2 V was used as an optimal value, which maximized the curing effects without device degradation. In the same vein, the optimal V_{ETA} is more closely associated with the generated temperature than the annealing time during the ETA. If the temperature is too high, the dopants in the source and drain are diffused out of the channel, and short-channel effects were worsened [18]. Additional, unwanted device degradations were found. This will be discussed later in the manuscript.

On the other hand, the longer t_{ANNL} was applied, the better curing effects to restore V_{TH} and *SS* were

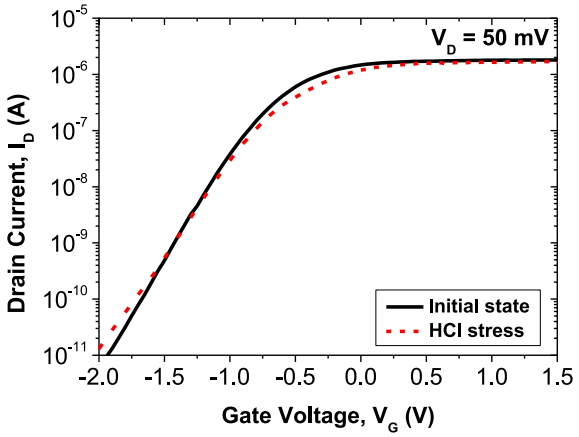

FIGURE 2. Measured $I_D - V_G$ characteristic of the FinFET before and after the HCI stress.

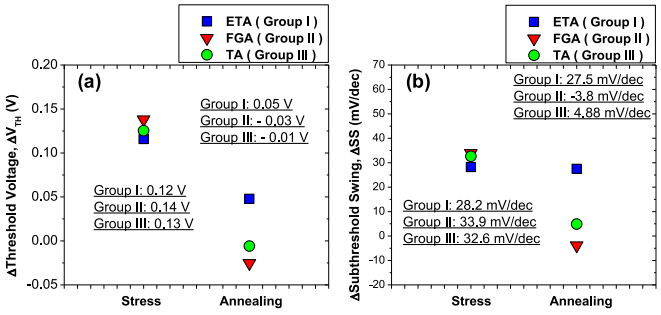

FIGURE 3. (a) Extracted average ΔV_{TH} and (b) ΔSS after the HCI ($V_{TH,HCI} - V_{TH,INT}$, SS_{HCI}- SS_{INT}) and after the annealing ($V_{TH,ANNL}$-$V_{TH,INT}$, SS_{ANNL}-SS_{INT}) by ETA, FGA and TA.

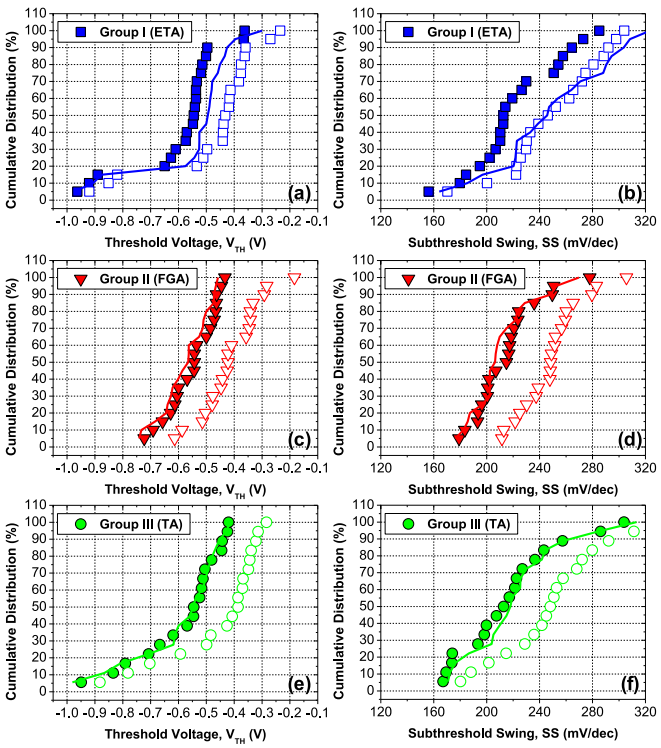

FIGURE 4. Statistical variation in V_{TH} and SS before the HCI (filled symbol), after the HCI (hollow symbol) and after annealing (line). (a)-(b) Group I with the ETA, (c)-(d) group II with the FGA and (e)-(f) group III with the TA, respectively.

observed [13], [19]. It should be noted that this work utilized the punchthrough current for Joule heating. Most of the I_D is not inversion current via the surface, but punchthrough current through the core of the fin-shaped channel. During the ETA, the measured fraction of inversion current compared to the total I_D at the V_{ETA} of 4.2 V is approximately 3 %. It is inferred that V_G dependency is negligibly small because the current for the ETA is dominated by V_D rather than by V_G. The annealing conditions for Group III, the furnace equipment and the detailed recipe were the same as those used for Group II, except without the use of H_2.

III. RESULTS AND DISCUSSION

Fig. 2 shows the measured *I-V* characteristics of the fabricated FinFET after the HCI stress. Fig. 3 shows the extracted average device parameters of the FinFET after the applied HCI stress and each corresponding annealing. After the applied stress, the V_{TH} and the SS increased due to gate oxide damage. The level of the degradations was nearly the same for all devices, as shown in Fig. 3(a)-(b). Note $\Delta V_{TH} = V_{TH,HCI} - V_{TH,INIT}$ and $\Delta SS = SS_{HCI} - SS_{INIT}$. After the stress, the extracted ΔV_{TH} and ΔSS were in a range of 0.12 V to 0.14 V and 28 mV/dec to 34 mV/dec, respectively, as shown in Fig. 3(a)-(b). In order to quantify the trap density (N_T), low-frequency noise (LFN) characteristics were analyzed (not shown), as discussed in our previous paper [15], [20]. After the stress, the 2.83×10^{18} cm^{-3} eV^{-1} of N_T was increased up to 9.51×10^{18} cm^{-3} eV^{-1}, and gate leakage (I_G) current of 200 fA was increased to 240 fA.

The curing effect for FGA, TA and ETA were in descending order. The FGA was the best, the TA was the second and the ETA was the worst, as shown in Fig. 3(a)-(b). The reason that the FGA exhibited better curing effect is due to the H_2 introduced during the 2nd FGA, in addition to the pre-existing H_2, which was applied in the aforementioned 1st FGA in the EXPERIMENTAL DETAILS. The reason that the TA even without H_2 is inferior to the FGA is that there was no introduction of new H_2. Regardless of N_2 ambient, the H_2 at the grain boundary of the poly-Si gate is dehydrogenated and diffuses out above 400 °C [21]. A similar result was reported by Fishbein *et al.* for the dehydrogenation of poly-Si above 500 °C [22]. It is noteworthy that the temperature for the dehydrogenation can be varied by device structure as well as dimension, dissimilar fabrication as well as different constituent material, and different annealing time as well as temperature. Even though the reported temperature for each dehydrogenation is not the same, they are reasonably similar [7], [21]–[22].

Fig. 4 shows the statistical variation in V_{TH} and SS prior to the HCI stress, after the HCI and after each annealing. Each curing trend in Fig. 4(a)-(f) is consistent with the average

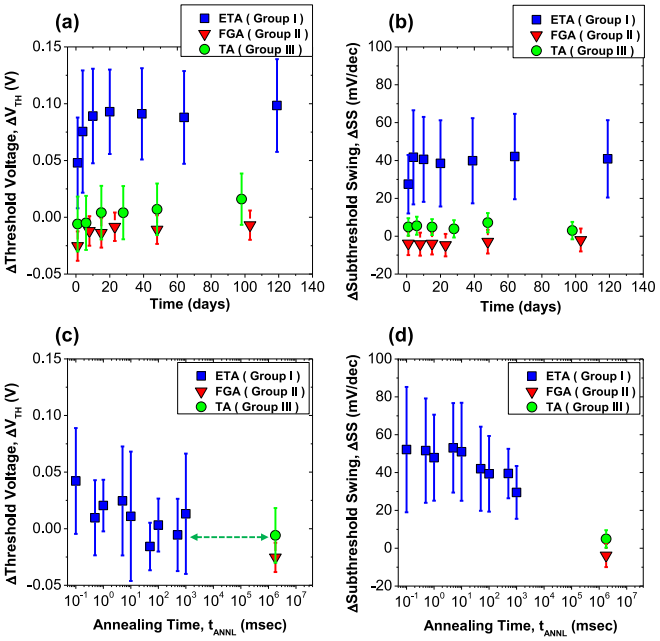

FIGURE 5. Elapsed time dependent characteristics of the FinFETs after annealing. (a) Extracted ΔV_{TH} and (b) ΔSS. (c)-(d) Curing characteristics versus t_{ANNL} from 0.1 ms to 1 sec.

values of ΔV_{TH} and ΔSS in Fig. 3(a)-(b). Fig. 5(a)-(b) show elapsed time dependent characteristics after each annealing. The ETA showed large variability compared with the FGA and the TA, because even though an identical V_{ETA} of 4.2 V was applied to Group I, there were probing variations during the measurements.

Note that metallization was not applied to make the metallic probing pads, for process simplicity. In addition, while the curing effects remained for longer than 100 days after the FGA and the TA, they remained for only a few days after the ETA. This suggests that the curing effect was weak and insufficient compared with the other methods.

The reason that the TA exhibited better curing effect than the ETA can be explained in two ways. First, it should be noted that the t_{ANNL} was 0.1 ms in the ETA and the t_{ANNL} was 30 min in the FGA and TA, hence the reaction for passivating the traps cannot be sufficiently enabled in such a short t_{ANNL}. The second reason is due to the different amounts of hydrogen. In the case of the TA, since the wafer enclosing the FinFETs was entirely annealed under 410 °C ambient, the amount of hydrogen obtained from grain boundary of the poly-Si gate is sufficient. However, in the case of ETA, hot-spots locally exist near the source/drain extension and the poly-Si gate acts as a heat sink [7]. Hence the amount of hydrogen for device curing is relatively insufficient. This fact is supported by the data shown in Fig. 5(c)-(d). When a longer t_{ANNL} of 50 ms was applied for the ETA, the curing of V_{TH} and SS was enhanced. Hence, prolonged annealing time is preferred to maximize the curing effects by ETA.

The curing mechanism of ETA can be summarized as follows. Device curing was initially observed near 210 °C to 280 °C [7], [13]. The temperature of 230 °C to 260 °C was consistent with the experimental results reported by Stesmans [23]. Hence, the curing mechanism is considered to be related to the passivation of dangling bonds by hydrogen which exists near the Si/SiO_2 interface [23]–[24]. However, when an ETA voltage, corresponding to the temperature range of 400 °C to 500 °C is applied, the hydrogen can be supplied from the gate grain boundary, as mentioned above. At the temperature of 400 °C to 500 °C, the concentration of hydrogen tends be to highly activated, hence the curing effect is maximized. The voltage corresponding to this temperature range is optimal for ETA [7], [13], [20]. However, when a voltage resulting in a temperature exceeding 600 °C is applied for ETA, secondary extra damage, which cannot be cured by thermal annealing, is generated [7], [13], [20]. This reasoning is supported by Stesmans's reports that the cured Si-H bonding at the Si/SiO_2 interface can be re-broken at higher temperature above 600 °C [25]. In this work, the HCI was used for the intentional stress and for fair comparison with our previous work [7]. However, it is also confirmed that damage stemmed from bias-temperature instability (BTI) is also curable by the ETA (not shown), and this observation is consistent with the other studies [26]–[29].

IV. CONCLUSION

The curing characteristics of damaged FinFETs were analyzed and fairly compared for three types of annealing method: FGA with H_2, TA without H_2 and ETA. Prior to annealing, a harsh HCI was applied to 58 FinFETs for intentional device aging. After each annealing, the representative device parameters were extracted and quantitatively compared. The ETA showed larger variability and lower sustainability than the other methods. This was caused by the relatively very short annealing time of 0.1 ms. The curing effect can be further improved by prolonging the annealing time from 0.1 ms to 1 s. Moreover, it can be inferred that incorporating hydrogen gas during the ETA is much preferred to maximize the curing effect.

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