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Experiments and 2D-Simulations for Quasi-saturation Effect in Power VDMOS Transistors

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Abstract

Quasi-saturation phenomena in power VDMOS transistors have been studied extensively by experiments and also by two dimensional device simulation. It has been found that the quasi-saturation current is proportional to the effective cell-to-cell spacing, and beyond the critical point, carrier drift velocity in JFET region is saturated and carrier modulation occurs under the gate region. The results of this work shows that a power VDMOS transistor should be designed to keep the operating current smaller than one half of the critical current (I^*) rather than I^* reported previously. This is obtained from the detailed analysis of the severe non-linearity of the on-resistance due to mobility degradation as well as to the channel length modulation in the JFET region.

1. Introduction

Recently vertical DMOS (VDMOS) has drawn much attention due to its inherent high speed capability as a power device [1]. However, the on-resistance area product, R_{on}·A, of a VDMOS is higher than that of bipolar devices for the same breakdown voltage. Therefore it is extremely important to determine cell-to-cell spacing optimally to minimize R_{on}·A [2]. But later it was found that the cell-to-cell spacing (a) must sometimes be wider than the optimal spacing to keep the operating current smaller than the critical current (I^*), because beyond quasi-saturation, the transconductance decreases very sharply [3].

In this paper, from experiments and numerical device simulation, we found that I^* is determined by the effective cell-to-cell spacing (a_{eff}) which is basically the same as the distance between two metallurgical p-body to n-substrate junctions. Moreover, the cell-to-cell spacing (a) should be determined such that the operating current should be less than $I^*/2$ rather than I^* [4]. This is obtained from the detailed analysis of the non-linearity in R_{on}·A due to the mobility degradation as well as to the channel length modulation in the JFET region, which was not considered before.

2. Fabrication of test devices

Power VDMOS transistors shown in Fig. 1 with various cell-to-cell spacings are fabricated and the I-V characteristics are measured. The silicon wafer has the n^- epitaxial layer grown on n^+ substrate. The resistivity of epitaxial layer is 13 ~ 15 Ω·cm and the thickness is 49±4 μm.

We followed typical DMOS fabrication process steps as reported in ref. [5]. They start from the boron implantation and the drive-in for p^+ region, and the gate oxide of 1000 Å is thermally grown. LPCVD n^+ doped poly-silicon is deposited and etched using RIE. After implantation of boron ions and drive-in for p-body phosphorus ions are implanted for n^+ source region. The vertical junction depths of p^+, p-body and n^+ regions are 6 μm, 4 μm and 1 μm, respectively. Aluminum metalization is performed to make both front and back-side ohmic contacts.

The transistors have 12 rectangular cells with common source size(s) of 25×25 μm^2 in mask dimension. The test VDMOS devices have different cell-to-cell spacings of a = 10 μm, 12 μm, 14 μm, 17 μm, 20 μm and 25 μm in mask dimension.

3. Experimental results

As a typical example, the measured I-V characteristics for VDMOS with a = 14 μm is shown in Fig. 2. From this figure, we can see that the quasi-saturation phenomenon occurs above V_{GS} = 5V for this device. Fig. 3 shows measured transfer characteristics at drain-to-source voltage (V_{DS}) of 20V, for devices with different cell-to-cell spacings. It is very clear from this figure that the current becomes saturated at high gate bias and the saturated current levels (quasi-saturation) are very sensitive to the cell spacing, a.

To see the drain-to-source voltage dependences of the quasi-saturation current, we plot quasi-saturated I_{DS} versus V_{DS} for various devices in a log-log scale as shown in Fig. 4. From this figure, we can make following arguments. Firstly, the values of on-resistances (R_{on}'s) show severe non-linearity for V_{DS} larger than 2V. Secondly, the I-V curves for various devices are almost parallel to each other. These observations imply that the quasi-saturation current is a very strong function of a and non-linearity is caused by some physical mechanism independent of a. To extract the relationship between the quasi-saturation current and cell-to-cell spacing, we plotted the quasi-saturation current versus cell-to-cell spacing for various drain-to-source voltages in Fig. 5. From this figure, we can see that the quasi-saturation current is proportional to the effective cell-to-cell spacing which is smaller than cell-to-cell spacing (mask dimension) by 6.4 μm. It is interesting to note that this coincides with the cell-to-cell spacing formed between two p-body to n-substrate metallurgical junctions. However, it shows that the linearity is not good for the case of a = 20μm and 25μm in Fig. 5. This deviation from linear I_{DS} versus a is caused by the finite epi-resistance, R_{epi}, which was shown in Fig. 1.

The critical current I^* [6], at which the electron drift velocity is saturated, can be written by

$$I^* = qfN_D N_{cell} \cdot (2s+a) \cdot a_{eff} v_{sat} \cdot \qquad (1)$$

Here f (=n/N_D) which is larger than 1 is the ra modulated carrier density(n) in the JFET regi (doping density of the epi-layer). v_{sat} is the s velocity and N_{cell} is the number of unit cell. Th I^*, which is calculated from Eq. (1), is shown and Fig. 4. From these figures, we can see characteristics shows severe non-linearity n The R_{on} estimated at $I=I^*$ is about twice larger measured at low V_{DS} as illustrated in Therefore, as a worst case design we recomme f=1/2 instead of 1 which was suggested in refs [6].

4. Discussion

To investigate the internal behavior of transistor, two dimensional device simulat carried out. The structure of the simulated shown in Fig. 6. Because our devices are com rectangular cells, 3D device simulation should However, we used 2D simulator to red computation time. But we used s/2 = 7μm ir 12.5μm to treat this 3D problem by an equiv simulation. Fig. 7(a) shows the contour plc electron concentration at high gate bias be quasi-saturation (V_{GS} = 14V). This figure sh severe carrier modulation occurs below the ga (f>1) as was reported before [4]. In addition see that the channel length of the JFET r severely modulated as the drain voltage increas

The linearity of on-resistance R_{on} n drain-to-source voltage is very important beca size is determined from thermal dissipation c [7]. However, as shown in Fig. 2 and Fig experimental data shows severe non-linearity o $V_{DS} \geq 2V$. To see whether this non-linearity i either by mobility degradation at high or by length modulation of JFET region, simulations using constant mobility and velocity saturatio The results are compared in Fig.7(b). This figu that about one half of the non-linearity is ca channel length modulation and the other

contributed by velocity saturation. This non-linearity due to channel length modulation is caused by the increase of the depletion region depth, X_D, as the drain-to-source voltage increases. The channel length of JFET region can be written by

$$X_J+X_D \cong X_J + \sqrt{\frac{2\varepsilon(V_{bi}+V_1)}{qN_D}}. \qquad (2)$$

The channel length of JFET in VDMOS transistors increases as a 1st order function of potential V_1 where V_1 is the effective voltage across JFET as shown in Fig. 1. But the mobility decreases as a 2nd order function of V_1. Therefore, the initial derivation of I-V characteristics from linearity is caused by channel length modulation. This is exactly observed in Fig. 7(b). Our simulation results for a wider spacing device are illustrated in Fig. 8, which show qualitatively the same tendency as those of Fig. 7.

If we look at our experimental data shown in Fig. 2, we can see that the power dissipation at $I_{DS} = I^*/2$ is about 20% higher than that calculated assuming low field R_{on}.This 20% can easily be considered by increasing chip size by 20%, for example. Therefore, we recommend to decide the cell spacing such that the operating current be smaller than $I^*/2$ instead of I^* as reported previously [4].One important thing to notice here is that although I^* can be increased by doping JFET region higher than the epi-region, the non-linearity due to channel length modulation cannot be improved. Moreover, this should be properly considered for the optimum doping profile of the epitaxial layer, because lower doping near the junction area to get higher breakdown voltage [8] can seriously increase the non-linarity of R_{on} due to channel length modulation.

5. Conclusions

We studied quasi-saturation phenomena in power VDMOS transistors extensively by experiments and also by two dimensional device simulation. We found that the quasi-saturation current is proportional to t effective cell-to-cell spacing which is almost same as t distance between two p-body to n-substrate junctior and beyond the critical point, carrier drift velocity JFET region is saturated and carrier modulation occu under the gate region. From the results, we recomme to design a power VDMOS such that the operati current should be smaller than one half of the critic current (I^*) rather than I^* reported previously. This obtained from the detailed analysis of the severe no linearity of the on-resistance due to mobility degradati as well as to the channel length modulation in the JFI region.

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References

[1] Y.Tarui, Y.Hayashi and T.Sekigawa, "Diffusi Self-aligned MOST: A New Approach for Hi Speed Device," J. Japan Soc. of Appl. Phys., V 39, pp. 105-110, 1970.

[2] P.L.Hower, T.M.S.Heng and C.Huang, "Optimu Design of Power MOSFETs," IEDM Tech. Di pp. 87-90, 1983.

[3] J.L.Sanchez et. al., "Quasi-saturation Effect in Hi voltage VDMOS Transistors," IEEE Proceedin Vol. 132(1), pp. 42-46, 1985.

[4] M.N.Darwish, "Study of the Quasi-saturation eff in VDMOS Transistors," IEEE Trans. Electr Devices, Vol. ED-33(11), pp. 1710-1716, 1986.

[5] H.J.Sigg, G.D.Vendlin, T.P.Cauge and J.Kocsis, "D-MOS Transistors for Microwave Applications," IEEE Trans. Electron Devices, Vol. ED-19(1), pp. 45-53, 1972.

[6] M.N.Darwish, "VDMOS Transistors with Improved On-resistance and Quasi-saturation Characteristics," IEDM. Tech. Dig., pp. 634-637, 1986.

[7] See for example, "HEXFET Data Book," International Rectifier Co., 1983.

[8] X.B.Chen and C.Hu, "Optimum Doping Profile of Power MOSFET Epitaxial Layer," IEEE Trans. on Elect. Dev., pp. 985-987, 1982.

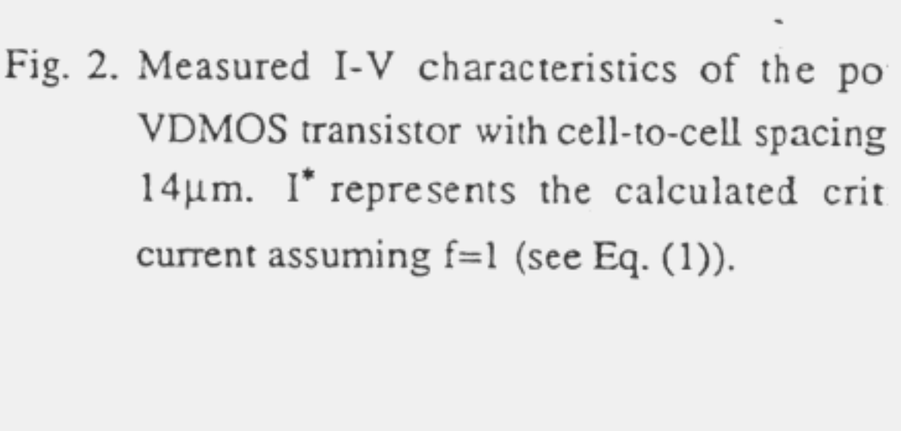


Fig. 2. Measured I-V characteristics of the po VDMOS transistor with cell-to-cell spacing 14μm. I^* represents the calculated crit current assuming f=1 (see Eq. (1)).

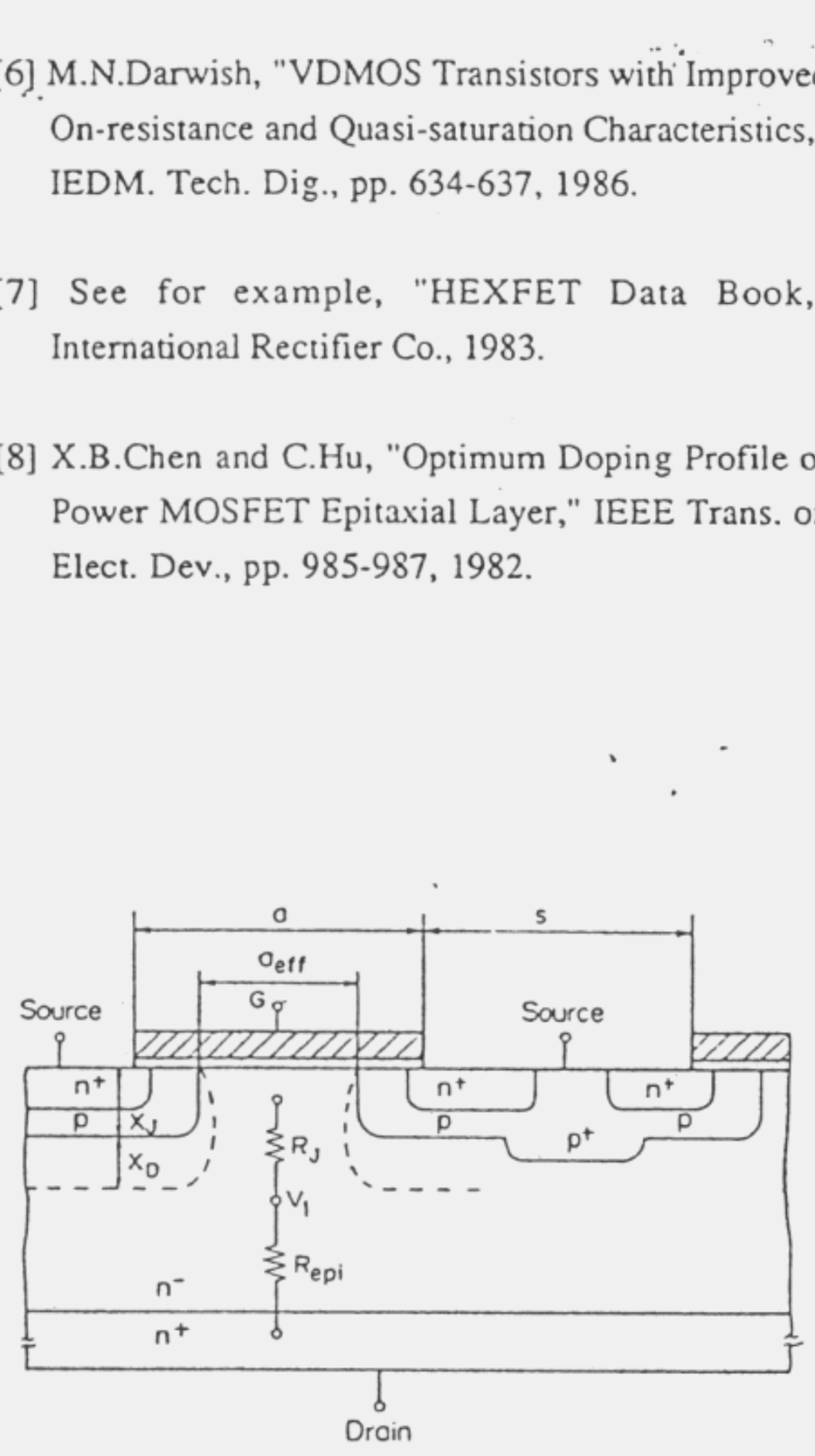


Fig. 1. The crosssection of power VDMOS transistors. R_J represents the non-linear resistance of the JFET region formed between two p-body regions. V_1 is the effective voltage across the JFET region.

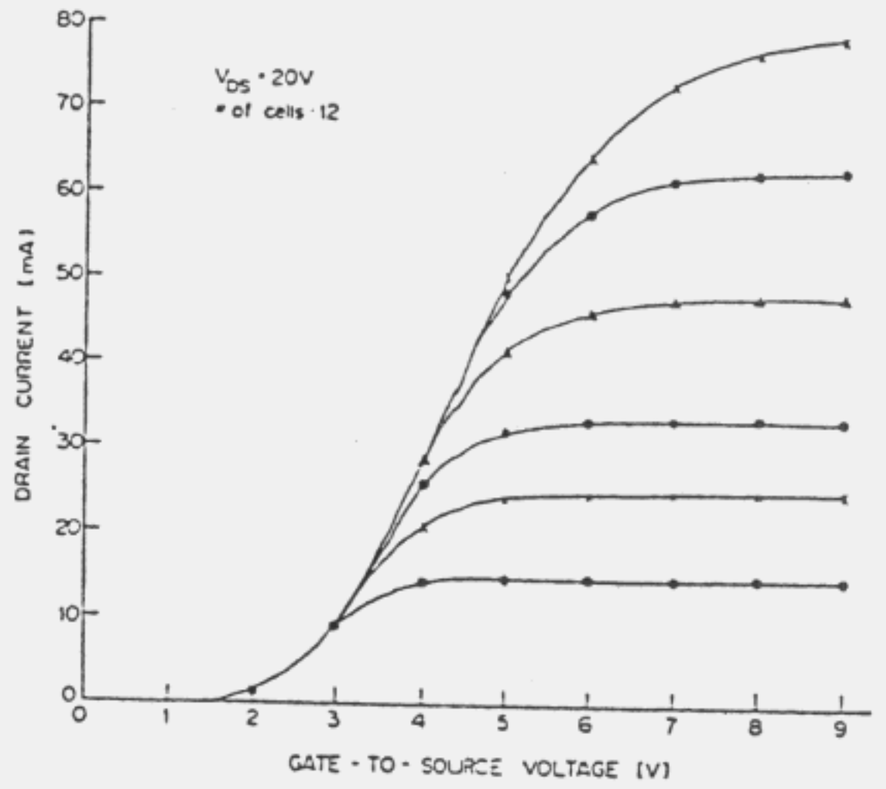


Fig. 3. Measured transfer characteristics for vari devices with different cell-to-cell spacings, a V_{DS} = 20V. The points represent the measu values.

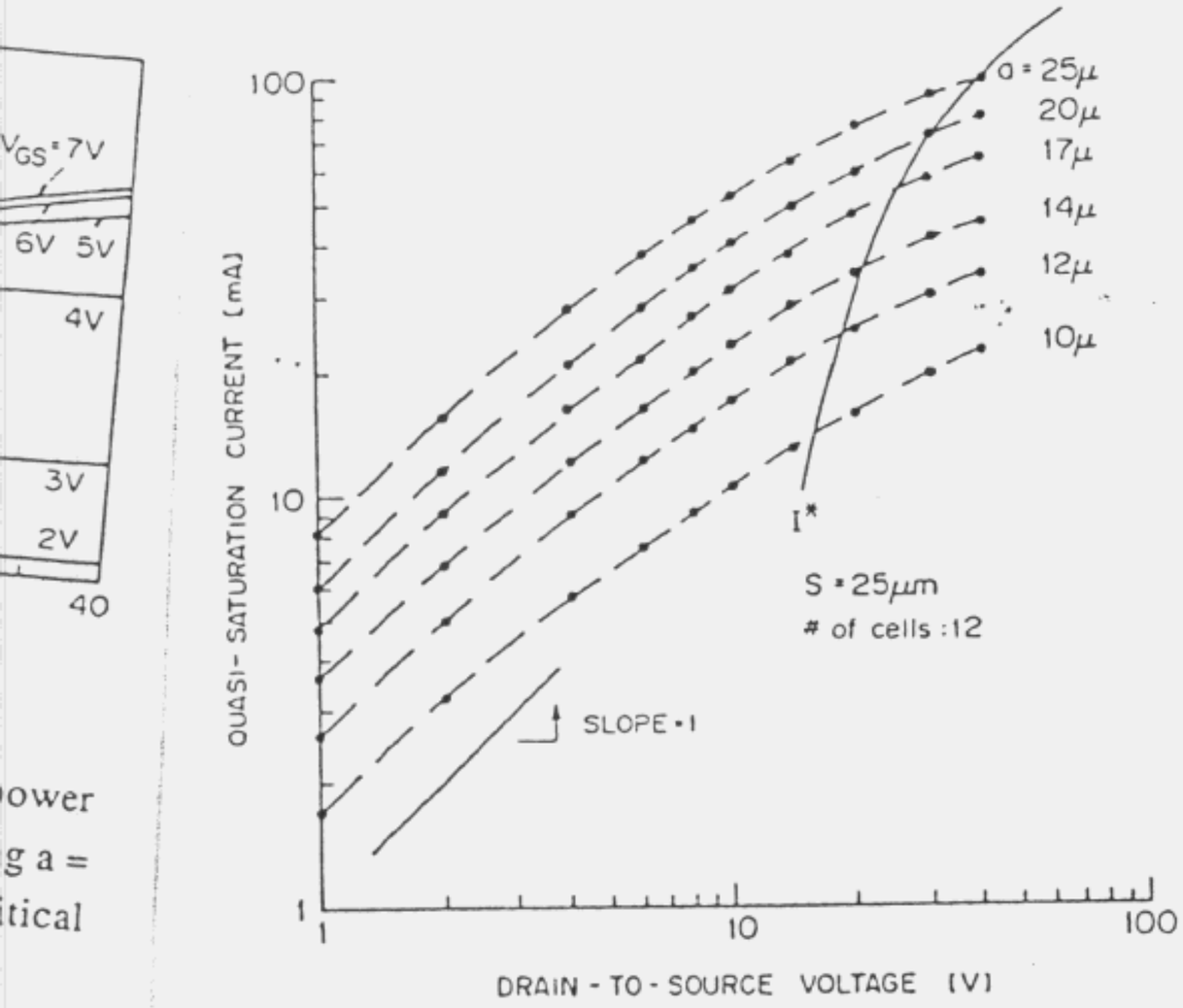


Fig. 4. Measured quasi-saturation current vs. drain-to-source voltage for various devices in log-log scale. The curves are almost parallel to each other. However, strong non-linearity is observed for $V_{DS} \geq 2V$. I^* represents the values of the critical current defined by Eq. (1) assuming f=1.

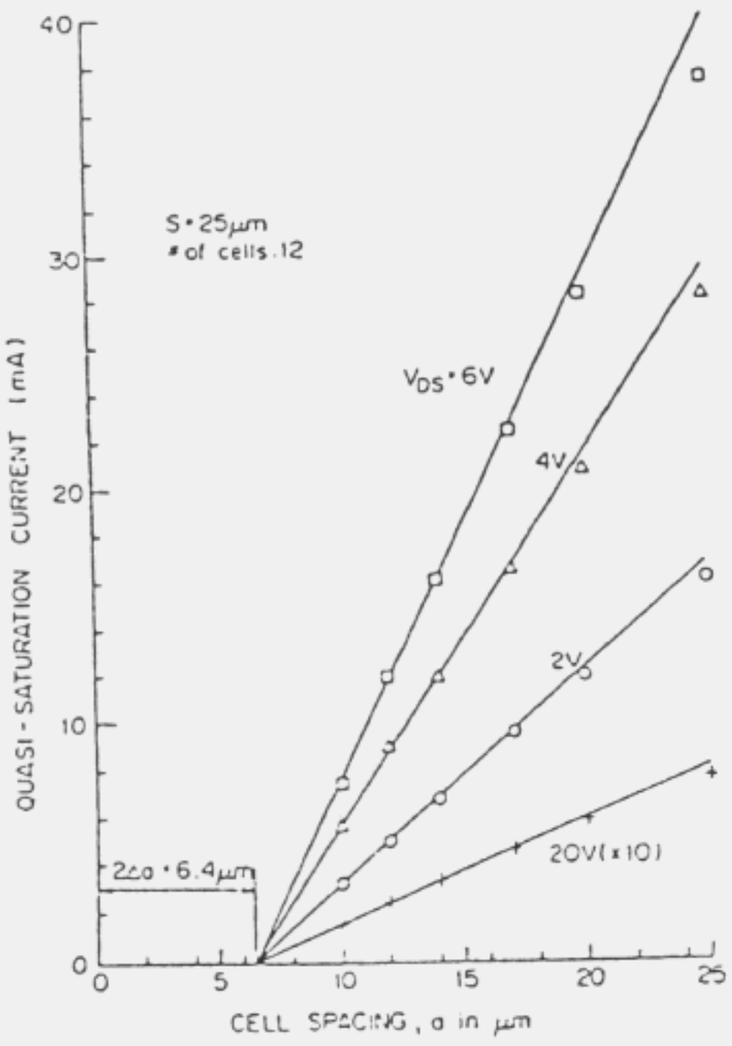


Fig. 5. Quasi-saturation current vs. cell-to-cell spacin for various drain-to-source voltages. Th current for V_{DS} = 20V is obtained b multiplying 10 to the value shown in the plot.

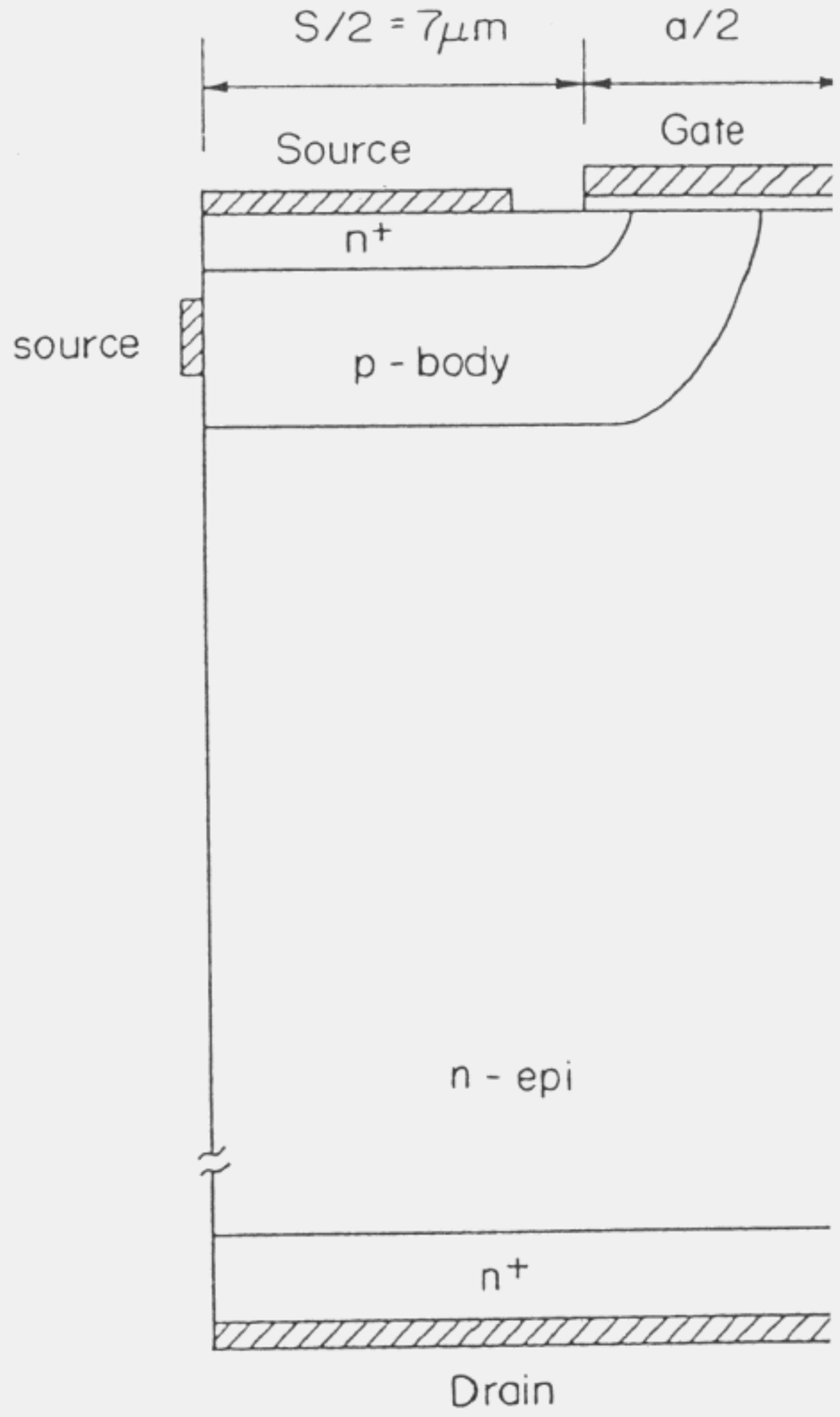
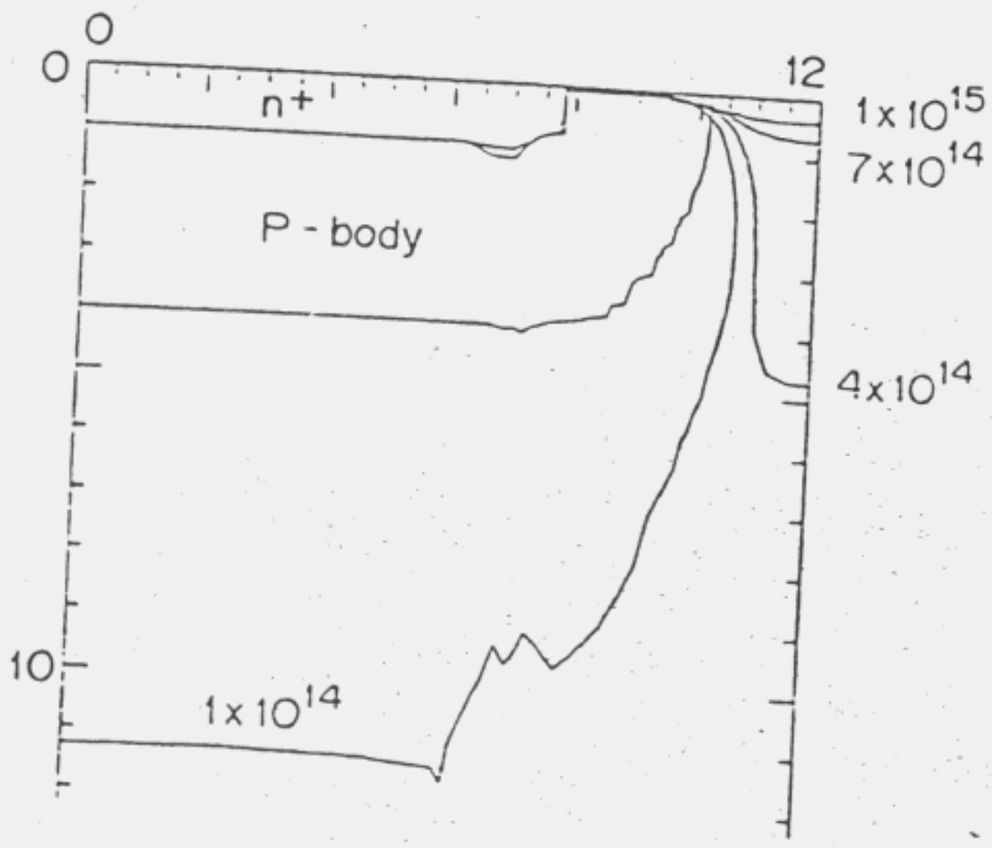
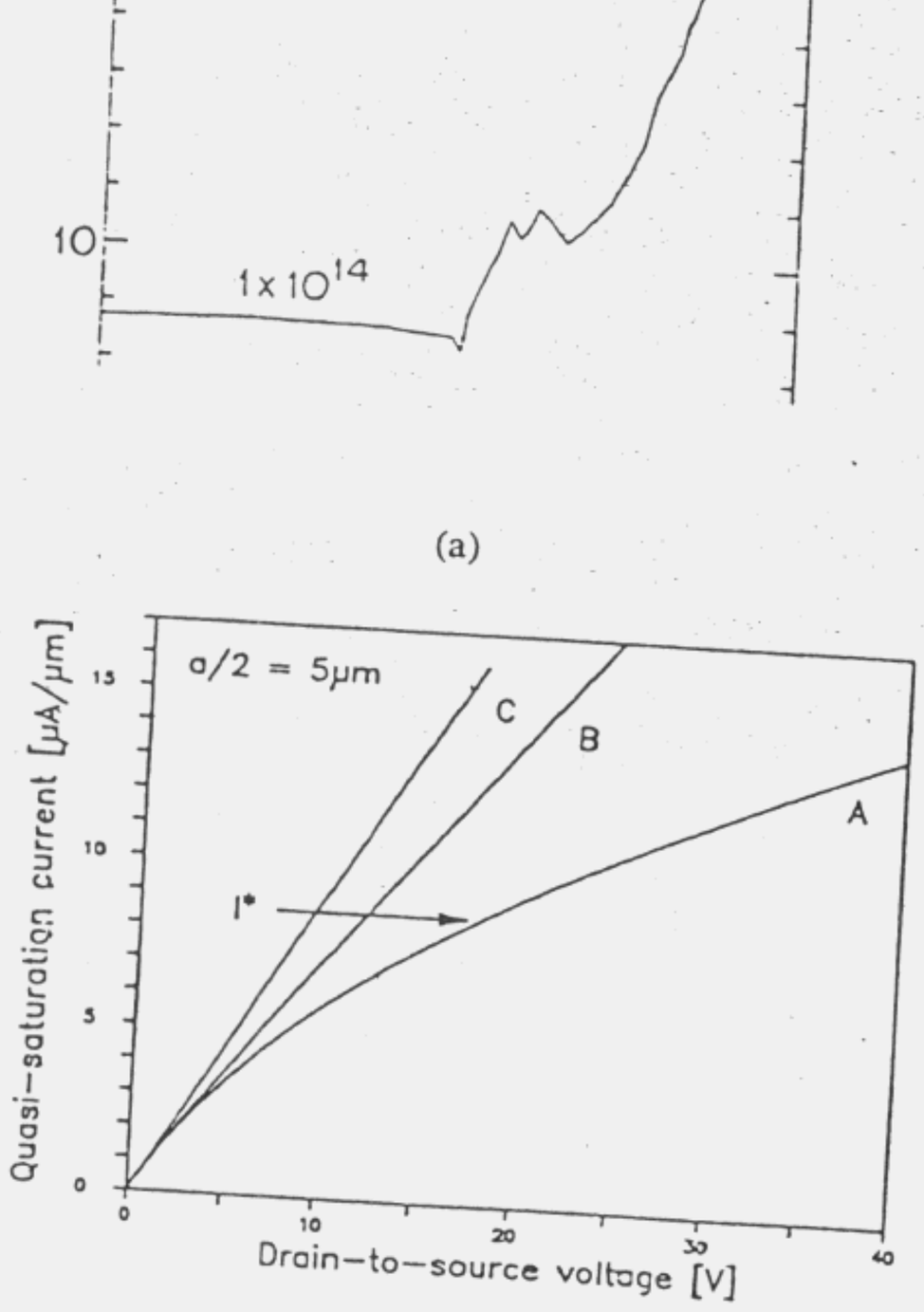


Fig. 6. The structure for two dimensional dev simulation. The thickness of epitaxial laye 49μm, the doping concentration is 3×10^{14}cr junction depths of p-body and n^+ are 4μm 1μm, respectively. s/2=7μm instead of 12.5 is used to effectively treat 3D rectangular structure by 2D.



(a)

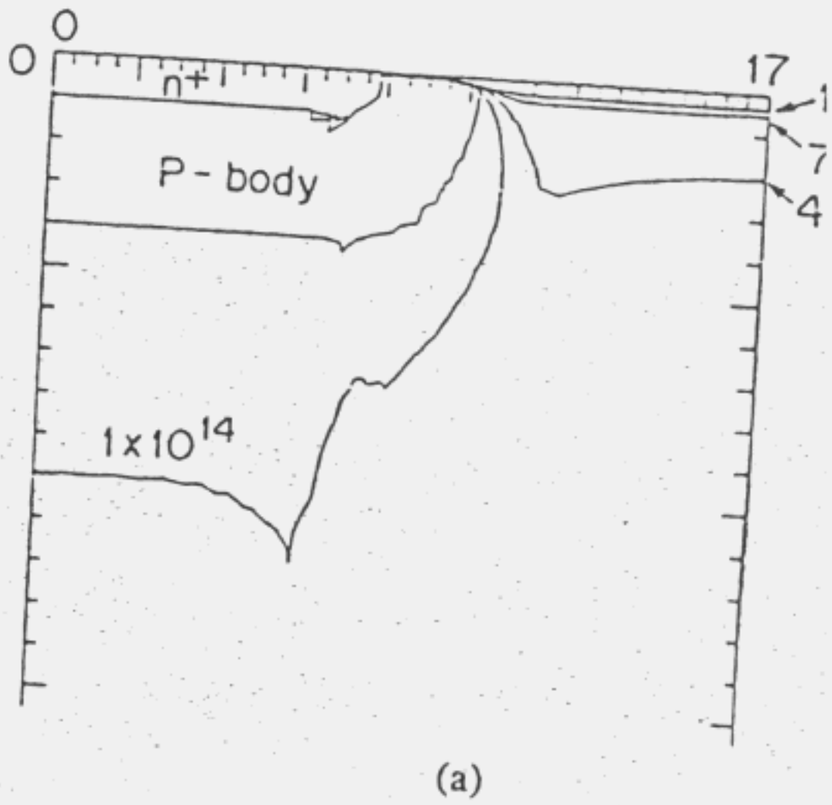


(b)

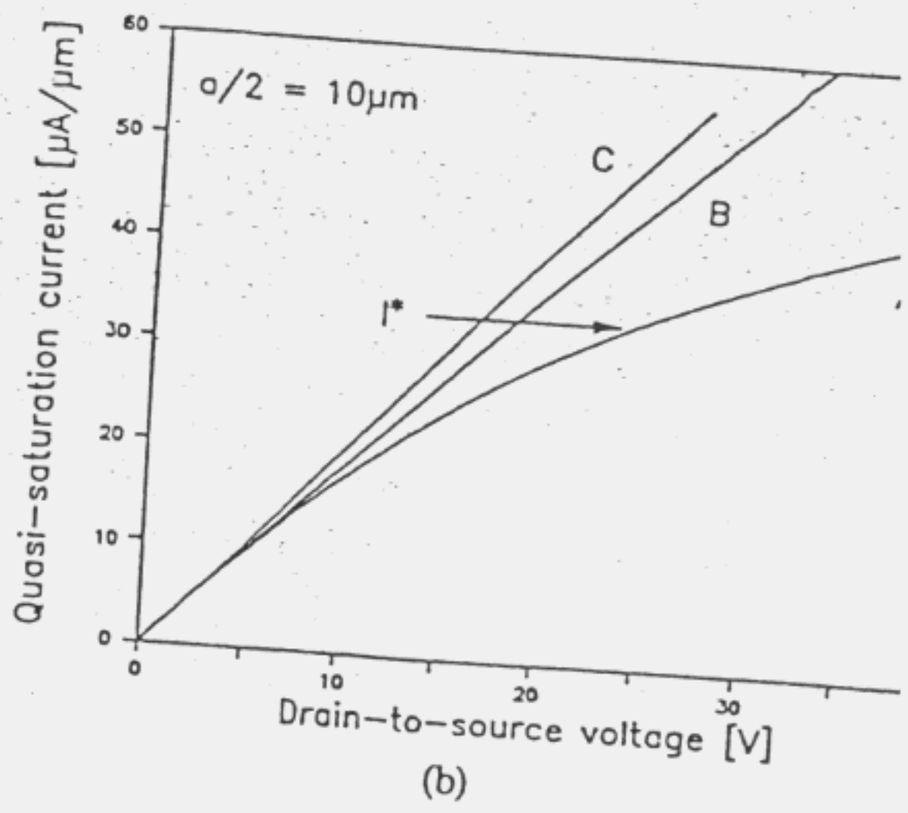
Fig. 7. Simulated results for a/2=5μm device at V_{GS}=14V.

(a) Contour plot for electron concentration at V_{DS}=20V. This shows the effective cell spacing, a_{eff}, is almost the same as the distance between two p-body to n-substrate metallurgical junctions.

(b) Quasi-saturation current vs. drain-to-source voltage. Curve A is obtained assuming velocity saturation, B is for constant mobility and C is for constant R_{on} obtained at low V_{DS}.



(a)



(b)

Fig. 8. Same as Fig. 7 with a/2=10μm.

Table I.

Summary of parameters for different devices studied i this paper. Note that at $I_{DS}=I^*$ (critical current), th actual power dissipation of each device is about twic larger than that calculated assuming constant low fiel R_{on}, due to the non-linearity of I-V characteristics.

a	R_{on} (V_{DS}=0)	I^* [from Eq.(1)]	V_{DS}^* ($I=I^*$)	$I^* \cdot R_{on}$	$\frac{V_{DS}^*}{I^* R_{on}}$
10μm	610Ω	14mA	16V	8.4V	1.9
12μm	380Ω	24mA	18V	9.1V	2.0
14μm	290Ω	35mA	20V	10V	2.0
17μm	258Ω	52mA	22V	12V	1.8
20μm	187Ω	70mA	25V	13V	1.9
25μm	165Ω	103mA	34V	17V	2.0