A 4.86 μW/Channel Fully Differential Multi-Channel Neural Recording System

Taeju Lee[1], Ji-Hyoung Cha[2], Su-Hyun Han[2], Seong-Jin Kim[2], and Minkyu Je[1]

[1]School of Electrical Engineering, Korea Advanced Institute of Science and Technology, (KAIST), Daejeon, Korea
[2]School of Electrical and Computer Engineering, Ulsan National Institute of Science and Technology (UNIST), Ulsan, Korea
{taeju.lee, mkje}@kaist.ac.kr

***Abstract*— This paper presents a fully differential multi-channel neural recording system. The system consists of four key blocks which are a low-noise amplifier (LNA), programmable gain amplifier (PGA), buffer, and successive approximation register ADC (SAR ADC). The input stage of the OTA used in LNA is designed as the inverter-based structure for improving the current efficiency. For an energy efficient system, the dual sample-and-hold (S/H) structure is applied to the SAR ADC. Each channel consumes the power of 4.86 μW/Channel and achieves an input-referred noise of 2.58 μV_{rms}. The implemented IC operates under a 1-V supply voltage for core blocks and 1.8-V for output digital buffers. The system is implemented in a standard 1P6M 0.18-μm CMOS process.**

Keywords—Neural recording system, low-noise amplifier, inverter-based input stage, energy efficient system.

I. Introduction

The low-power, low-noise multi-channel neural recording system is one of the many parts required to perform brain research. Thanks to the development of a multi-channel electrode array, the recorded neurons have steadily increased. Accordingly, the number of recording circuits has to increase. In the case of the implantable biomedical devices, the system must be driven with low power to prevent necrosis caused by heat. At the same time, the system should be designed to have low noise characteristics to measure microscale neural signals. The neural signals are distributed in the frequency band from sub-1 Hz to several kHz. This band is vulnerable to the interference such as power lines and stimulation signals. Therefore, the recording system that is robust against the interference should be designed. In this paper, we present a low-power, low-noise fully differential multi-channel neural recording system for implantable biomedical devices.

II. System Architecture

Fig. 1 shows the proposed system architecture, which consists of analog front-ends (AFEs), analog multiplexers (AMUXs), dual SAR ADCs, digital multiplexers (DMUXs), a bias circuit, and an output driver. To implement the 64-channel recording system, eight unit blocks (*Set N, N*=1-8) are used. Each unit block consists of LNAs, PGAs, buffers, an AMUX, and a 10-bit dual SAR ADC. The AFE that consists of LNA, PGA, and buffer is designed as a fully differential structure. In the unit block, eight AFEs share an AMUX and an ADC. An AMUX accepts eight channels and sends two channels to the ADC through selection signals SEL_A and SEL_B. After the digitization of neural signals, the channel selection is performed by four DMUXs, which are controlled through S_{X1} and S_{Y1}. The final channel selection is conducted by a DMUX controlled by S_{X2} and S_{Y2}. The output signals are 11 bits consisting of one end-of-conversion (EOC) signal and 10-bit data. The overall system is driven with 1-V and 1.8-V supply voltages. The 1-V supply voltage is to operate AFEs, AMUXs, ADCs, DMUXs, and a bias circuit.

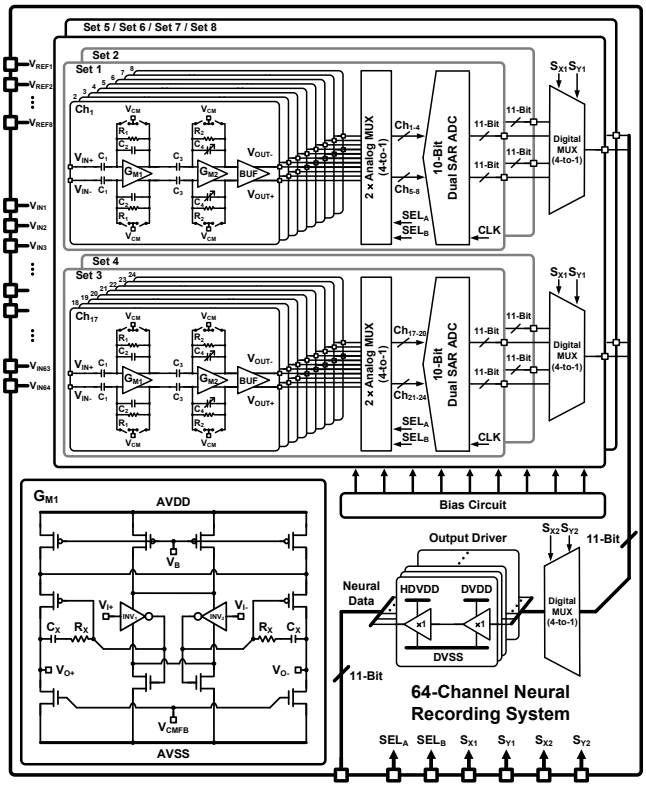


Fig. 1. Architecture of the multi-channel neural recording system.

The 1.8-V supply voltage is used for the output driver, which up-shifts the voltage level of the final output bits to interface with the field-programmable gate array (FPGA). The LNA and PGA are implemented as a capacitively-coupled structure. The OTA G_{M1} used in the LNA is shown in Fig. 1. The input stage of the G_{M1} is implemented as the inverter-based structure, reported in [1], [2], for improving the current efficiency. The output DC bias point of the G_{M1} is set by one common-mode feedback (CMFB) OTA. The input stage of the OTA G_{M2} used in the PGA is designed as only PMOS pair. The voltage gains of the LNA and PGA are set by the ratio of C_1/C_2 and C_3/C_4, respectively. The input DC bias points of G_{M1} and G_{M2} are set by R_1 and R_2, respectively. The R_1 and R_2 are implemented using two diode-connected MOSFETs for area efficient design while achieving the high resistance. The output buffer for driving the ADC input is implemented as a rail-to-rail type based on [2].

In the digitization stage, the dual S/H structure in [2] is employed to increase the sampling time for the A/D conversion, which can reduce the power burden on the buffer. To lower the power consumption in the ADC, the delay chain based time domain comparator, that is reported in [3], is adopted as shown in Fig. 2. In this work, the 4-stage delay chain is used to convert the input signals of V_{DAC+} and V_{DAC-}

This research was supported by the Convergence Technology Development Program for Bionic Arm (2017M3C1B2085296) and the Brain Research Program (2017M3C7A1028859) through the National Research Foundation Korea (NRF) funded by Ministry of Science and ICT.

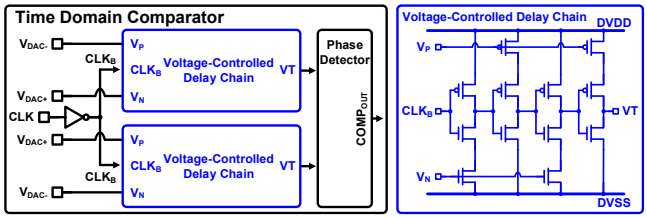


Fig. 2. Block diagram of the time domain comparator [3].

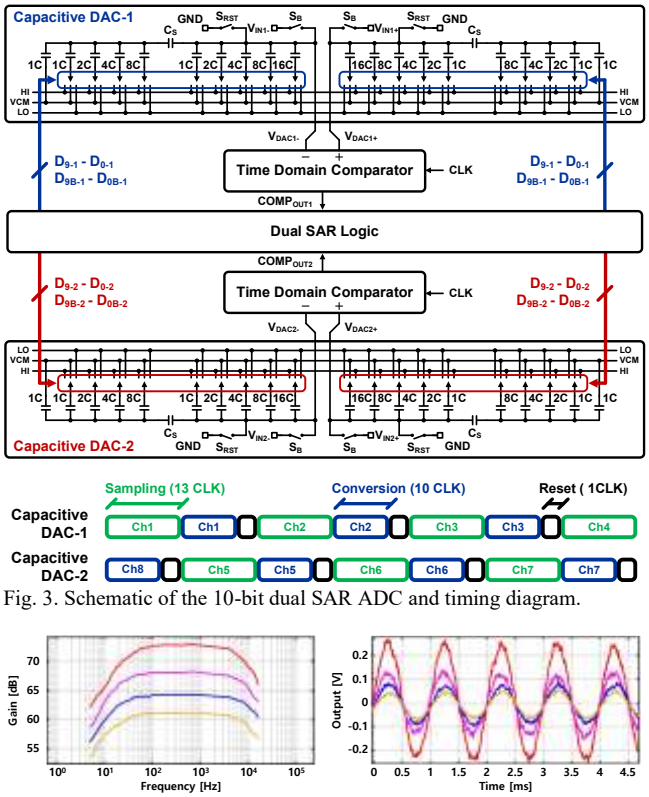


Fig. 3. Schematic of the 10-bit dual SAR ADC and timing diagram.

Fig. 4. Measured frequency response (left) and time domain results corresponding to each gain with a 100 μV_{pp} input at 1 kHz (right).

to the delay difference based on the reference clock CLK_B. The dual operation of the ADC is performed using two capacitive DACs (CDACs) that are implemented as the split array for area efficient design. The unit capacitance used in the CDAC is 150 fF with MIM structure occupying the area of 72 μm^2. Fig. 3 shows the schematic of the 10-bit dual SAR ADC and timing diagram for channel conversion.

III. Measurement Results

The IC is fabricated in a 1P6M 0.18-µm CMOS process. The active area of a 64-channel recording system is 9.4 mm^2. The power consumption of a single channel, including LNA, PGA, buffer, and ADC, is 4.86 µW/Ch. The system gain is measured from 61 dB to 74 dB with the bandwidth of 10 kHz. Fig. 4 shows the measured frequency response and time domain results corresponding to each gain. The input-referred noise (IRN) is measured as 2.58 μV_{rms} when integrated from 10 Hz to 10 kHz as shown in Fig. 5. The noise efficiency factor (NEF) is calculated as 2.19, resulting in the power efficiency factor (NEF^2V_{DD}) of 4.80. The total harmonic distortion of the AFE is measured as 1.5 %, corresponding to –36.5 dB that is measured using 100 μV_{pp} input at 1 kHz as shown in Fig. 6(a). The output power

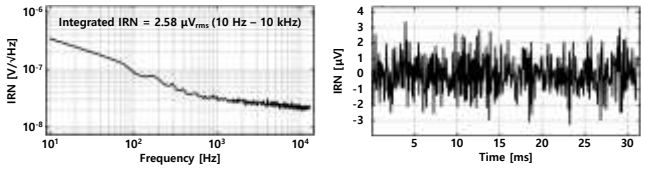


Fig. 5. Measured input-referred noise in the frequency domain (left) and time domain (right).

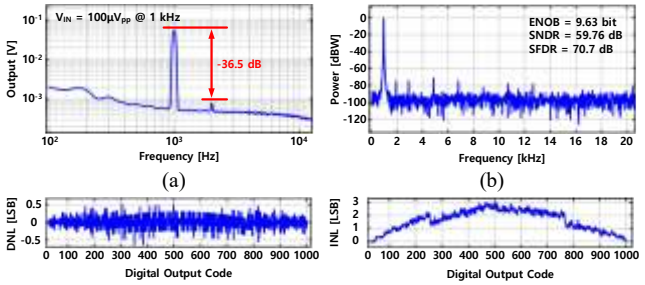
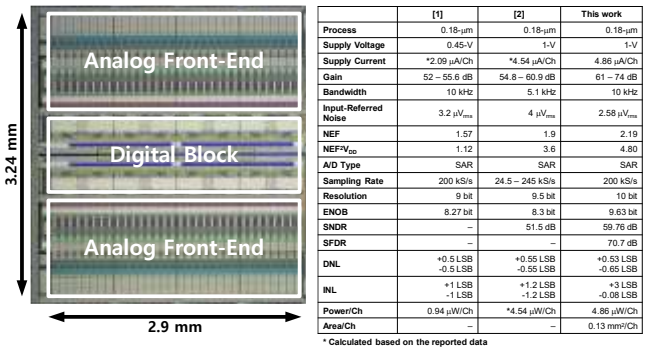


Fig. 6. (a) Measured total harmonic distortion of the analog front-end, (b) Output power spectrum of the ADC, (c) Differential nonlinearity (DNL), and (d) Integral nonlinearity (INL).



	[1]	[2]	This work
Process	0.18-µm	0.18-µm	0.18-µm
Supply Voltage	0.45-V	1-V	1-V
Supply Current	*2.09 µA/Ch	*4.54 µA/Ch	4.86 µA/Ch
Gain	52 – 55.6 dB	54.8 – 60.9 dB	61 – 74 dB
Bandwidth	10 kHz	5.1 kHz	10 kHz
Input-Referred Noise	3.2 μV_{rms}	4 μV_{rms}	2.58 μV_{rms}
NEF	1.57	1.9	2.19
NEF^2V_{DD}	1.12	3.6	4.80
A/D Type	SAR	SAR	SAR
Sampling Rate	200 kS/s	24.5 – 245 kS/s	200 kS/s
Resolution	9 bit	9.5 bit	10 bit
ENOB	8.27 bit	8.3 bit	9.63 bit
SNDR	–	51.5 dB	59.76 dB
SFDR	–	–	70.7 dB
DNL	+0.5 LSB -0.5 LSB	+0.55 LSB -0.55 LSB	+0.53 LSB -0.65 LSB
INL	+1 LSB -1 LSB	+1.2 LSB -1.2 LSB	+3 LSB -0.08 LSB
Power/Ch	0.94 µW/Ch	*4.54 µW/Ch	4.86 µW/Ch
Area/Ch	–	–	0.13 mm^2/Ch

* Calculated based on the reported data

Fig. 7. Die micrograph (left) and performance summary (right).

spectrum of the ADC is measured using 1 V_{pp} input at 1 kHz, resulting in the effective number of bits (ENOB) of 9.63 bit, signal-to-noise and distortion ratio (SNDR) of 59.76 dB, and spurious-free dynamic range (SFDR) of 70.7 dB as shown in Fig. 6(b). The differential nonlinearity (DNL) and integral nonlinearity (INL) are measured as +0.53/–0.65 LSB and +3/–0.08 LSB respectively as shown in Fig. 6(c) and (d). The clock frequency for ADC operation is set to 2.5 MHz. Fig. 7 shows the die micrograph and performance summary.

IV. Conclusion

The implemented IC consumes the power of 4.86 µW/Ch and occupies the area of 0.13 mm^2/Ch while achieving the input noise of 2.58 μV_{rms} by employing the inverter-based structure in the LNA input stage. The power burden on the buffer is reduced by using the dual S/H technique while maintaining the sampling rate of 200 kS/s.

References

[1] D. Han et al., "A 0.45 V 100-Channel Neural-Recording IC With Sub-µW/Channel Consumption in 0.18 µm CMOS," *IEEE TBioCAS*, vol. 7, no. 6, pp. 735-746, Dec. 2013.

[2] X. Zou et al., "A 100-Channel 1-mW Implantable Neural Recording IC," *IEEE TCAS–I*, vol. 60, no. 10, pp. 2584-2596, Oct. 2013.

[3] S.-K. Lee et al., "A 21fJ/Conversion-Step 100 kS/s 10-bit ADC With a Low-Noise Time-Domain Comparator for Low-Power Sensor Interface," *IEEE JSSC*, vol. 46, no. 3, pp. 651-659, Mar. 2011.