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A Physically Based High Frequency Noise Model of MESFET's Taking Static Feedback Effect into Account

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Abstract. A new physically based thermal noise model for MESFET's has been proposed, which is compatible with small signal equivalent circuit and large signal current-voltage characteristics. Specifically, the static feedback effect is taken into account to model noise characteristics correctly especially in low current regime. The gate and drain bias dependence of the gate noise voltage, the drain noise current, and the correlation coefficient between them has been investigated thoroughly, showing good agreement with experimental results from 0.5μm gate length MESFET. As a result, our formulation is successfully used to model bias dependence of the four noise parameters with reasonably good accuracy. Our model is simple and physical enough for device design and circuit simulation especially for MMIC application.

1. Introduction

The high frequency noise model of MESFET has been widely studied since 1970's[1]. Though Statz's model is physically solid, its formulation was not extensively compared with experimental results and the relationship with large signal current-voltage model is obscure. Moreover, the static feedback effect which is appreciable in modern short channel MESFET was not considered. Though Fukui's model[2] is a good first order estimation for minimum noise figure, the other noise parameters were not investigated. Pospieszalski's[3] model proposed a simple noise equivalent circuit where two noise sources are used at the gate and drain ports. Although this model is simple enough to give physical insight into circuit design, the accuracy is strongly dependent on the noise sources whose values are not physically explained. And the correlation between the noise sources is neglected.

In this paper, we propose a new physically based noise model of MESFET's, which is compatible not only with small signal equivalent circuit, but also with large signal I-V as well as C-V models.

2. Current-voltage and capacitance-voltage relation of MESFET

Our I-V model is derived based on the following assumptions. Firstly, we divide the channel into two regions. One is the so called gradual channel approximation region and the other is the so called velocity saturation region. Secondly, we assume that the channel capacitance per unit area, C_{in}, is constant along the channel for a given gate-source voltage, V_{GS}. Thirdly, the two-piece velocity-electric field relation is assumed,

i.e., the electron velocity is proportional to electric field below critical field, F_{crit}, and saturated at v_{sat} above F_{crit}.

The saturation voltage, V_{Dsat}, is calculated as $V_{GST}+V_L-(V_{GST}^2+V_L^2)^{0.5}$ [4]. Here, V_L is $F_{crit}L_G$. As V_D increases over V_{Dsat}, the potential in the velocity saturation region increases exponentially and the effective channel length decreases. As a first order approximation, the potential profile in the velocity saturation region can be written as [5]

$$V(x) = V_{Dsat} + V_\lambda(\exp(x/\lambda) - 1), \tag{1}$$

where λ is the characteristic length of velocity saturation region, and $V_\lambda = F_{crit}\lambda$. Inverting Eq.(1), the length of velocity saturation region, ΔL can be calculated. To take into account the current increase in saturation regime due to the channel length modulation, we use the following expression for the saturation regime drain current[5]

$$I_{DS} \approx I_{sat}\left(1 + \frac{V_\lambda}{V_L}\ln\left(1 + \frac{V_D - V_{Dsat}}{V_\lambda}\right)\right). \tag{2}$$

Here I_{sat} is the drain current at $V_{DS}=V_{Dsat}$. The static feedback effect can be considered by taking threshold voltage as a function of V_{DS}. We adopt the following dependence[6]

$$V_{GST} = V_{GST0} + \sigma V_{DS}, \tag{3}$$

where V_{GST0} is V_{GST} at V_{DS}=0V, σ is the static feedback effect coefficient. Lastly the following expression is used to take σ dependence on V_{GS} into account[7],

$$\sigma = \frac{\sigma_0}{1 + \exp\left(\dfrac{V_{GST0} - V_{\sigma T}}{V_\sigma}\right)}. \tag{4}$$

The gate-source capacitance, C_{gs}, and the gate-drain capacitance C_{gd} can be defined by partial derivative of gate charge with respective to source voltage, V_S, and drain voltage, respectively. We assume that the sum of the gate charge and the channel charge is conserved. Based on the gradual channel approximation, the channel current can be written as $\mu C_{in}W(V_{GT}-V(x))\, dV(x)/dx$. Using this relation, the potential distribution in the region 1 can easily be found as following

$$V(x) = V_{GT} - \sqrt{V_{GST}^2 - 2I_{DS}R_nV_x}, \tag{5}$$

where V_x is $F_{crit}x$ and R_n is the inverse of $v_{sat}C_{in}W$. The total channel charge can be obtained from the following integration,

$$\frac{Q_n}{C_{in}W} = -\int_0^{L_1} dx\sqrt{V_{GST}^2 - 2I_{DS}R_nV_x} - \Delta L(V_{GT} - V_{Dsat}). \tag{6}$$

$x=L_1$ is the point where the potential is equal to V_{Dsat}. Using Eqs.(5)~(6), C_{gs} and C_{gd} can be calculated. Then, C_{gs} can be written as

$$\frac{C_{gs}}{C_{in}W} = L_1\left(\frac{V_{GST}}{V_{GST} - \frac{1}{2}V_{DS}} - \frac{\left(V_{GST} - \frac{1}{3}V_{Dsat}\right)V_{Dsat}}{2I_{DS}R_{B0}\left(V_{GST} - \frac{1}{2}V_{DS}\right)}\right) + \frac{\Delta L V_{GST}}{\sqrt{V_{GST}^2 + V_L^2}}, \tag{7}$$

where the inverse of R_{B0} is defined by $-dI_{DS}/dV_S$ with constant V_{GT} and V_D. And C_{gd} can be written as

$$\frac{C_{gd}}{C_{in}W} = L_1\frac{(V_{GST} - V_{Dsat})\left(V_{GST} - \frac{1}{3}V_{Dsat}\right)}{2I_{DS}R_{A0}\left(V_{GST} - \frac{1}{2}V_{Dsat}\right)} - \Delta L\frac{V_{GST} - V_{Dsat}}{I_{DS}R_{A0}}, \tag{8}$$

where the inverse of R_{A0} is defined by dI_{DS}/dV_D with constant V_{GT} and V_S.

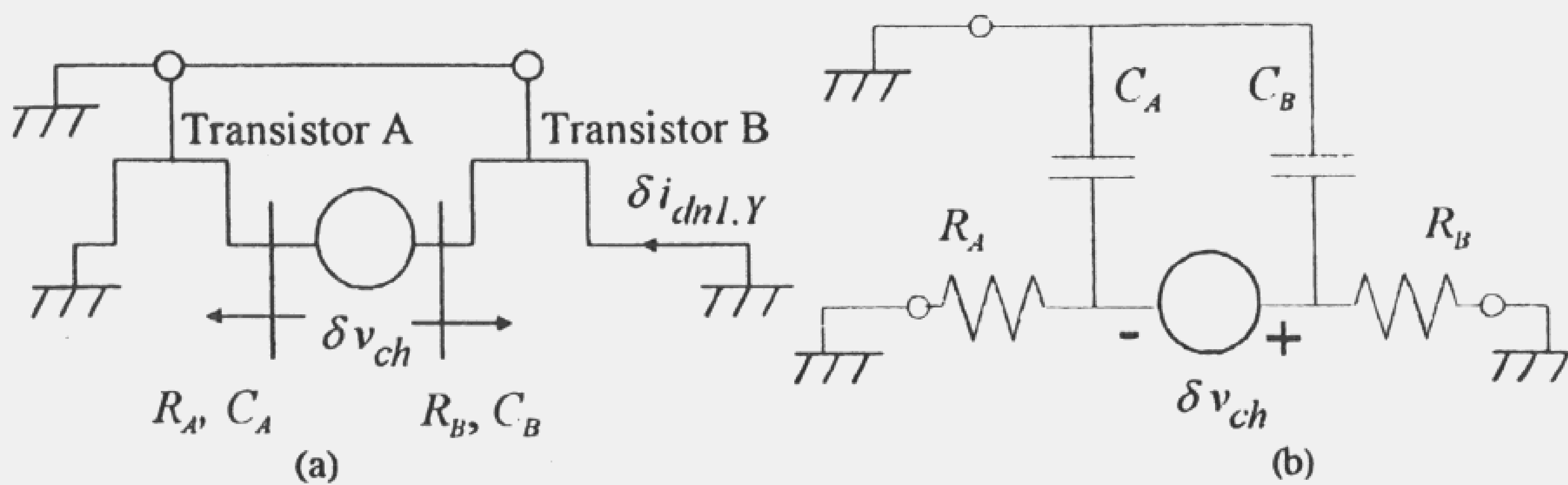

Fig.1. (a) Division of MESFET into two parts. (b) Small signal equivalent circuit of (a).

3. Noise modeling

The infinitesimal thermal noise voltage source, δv_{ch} is distributed along the region 1. In reference to δv_{ch}, we divide MESFET into two parts, i.e., sub-transistors A and B which are located toward the source and drain side of the MESFET, respectively (Fig.1). R_A, R_B, C_A and C_B are the small signal resistance's and capacitance's seen from the drain and source side of the sub-transistors A and B. The values of these parameters are position dependent. $R_A(x)$ and $R_B(x)$can be derived from partial derivative of I_{DS} of sub-transistors A and B. And $C_A(x)$ and $C_B(x)$ are C_{gd} and C_{gs} of sub-transistors A and B. The infinitesimal noise voltage is thermally generated one at some point of the region 1. Its quantity is proportional to the infinitesimal resistance δR. In addition, we find that the consideration of the mobility degradation by the transverse electric field[8], gives better fit with the experimental results. We introduce the factor, γ, to take the transverse field induced mobility degradation into account. Then, $\langle \delta v_{ch}^2 \rangle$ can be written as

$$\left\langle \delta v_{ch}^2 \right\rangle = 4kT\Delta f \frac{\gamma \, dV_x}{\mu C_{in} W \sqrt{V_{GT}^2 - 2 I_{DS} R_n V_x}}, \tag{9}$$

where k is the Boltzmann constant, T the absolute temperature, and Δf is the bandwidth. γ should be equal to 1 at zero drain bias and increase with drain bias. This is taken into account as following equation.

$$\gamma = \frac{2\gamma_0}{\gamma_0 + 1 - (\gamma_0 - 1)\dfrac{V_{DS}^3 - 3V_{Dsat}^3}{V_{DS}^3 + 3V_{Dsat}^3}}. \tag{10}$$

The infinitesimal drain noise current in Y-representation induced by δv_{ch} is

$$\delta i_{dn1,Y} = -\frac{\delta v_{ch}}{R_A + R_B}. \tag{11}$$

The infinitesimal gate noise current is also calculated from equivalent circuit in Fig.2 as

$$\delta i_{gn1,Y} = \delta v_{ch} \frac{j\omega \left(-R_B C_B + R_A C_A\right)}{R_A + R_B}. \tag{12}$$

The noise sources in H-representation can be easily derived from Eqs.(11)~(12) as

$$\delta v_{gn1,H} = \delta v_{ch} \frac{-R_B C_B + R_A C_A}{(R_A + R_B) C_{gs}}, \text{ and} \tag{13}$$

$$\delta i_{dn1,H} = -\frac{\delta v_{ch}}{R_A + R_B}\left(1 - \frac{g_m \left(R_B C_B - R_A C_A\right)}{C_{gs}}\right). \tag{14}$$

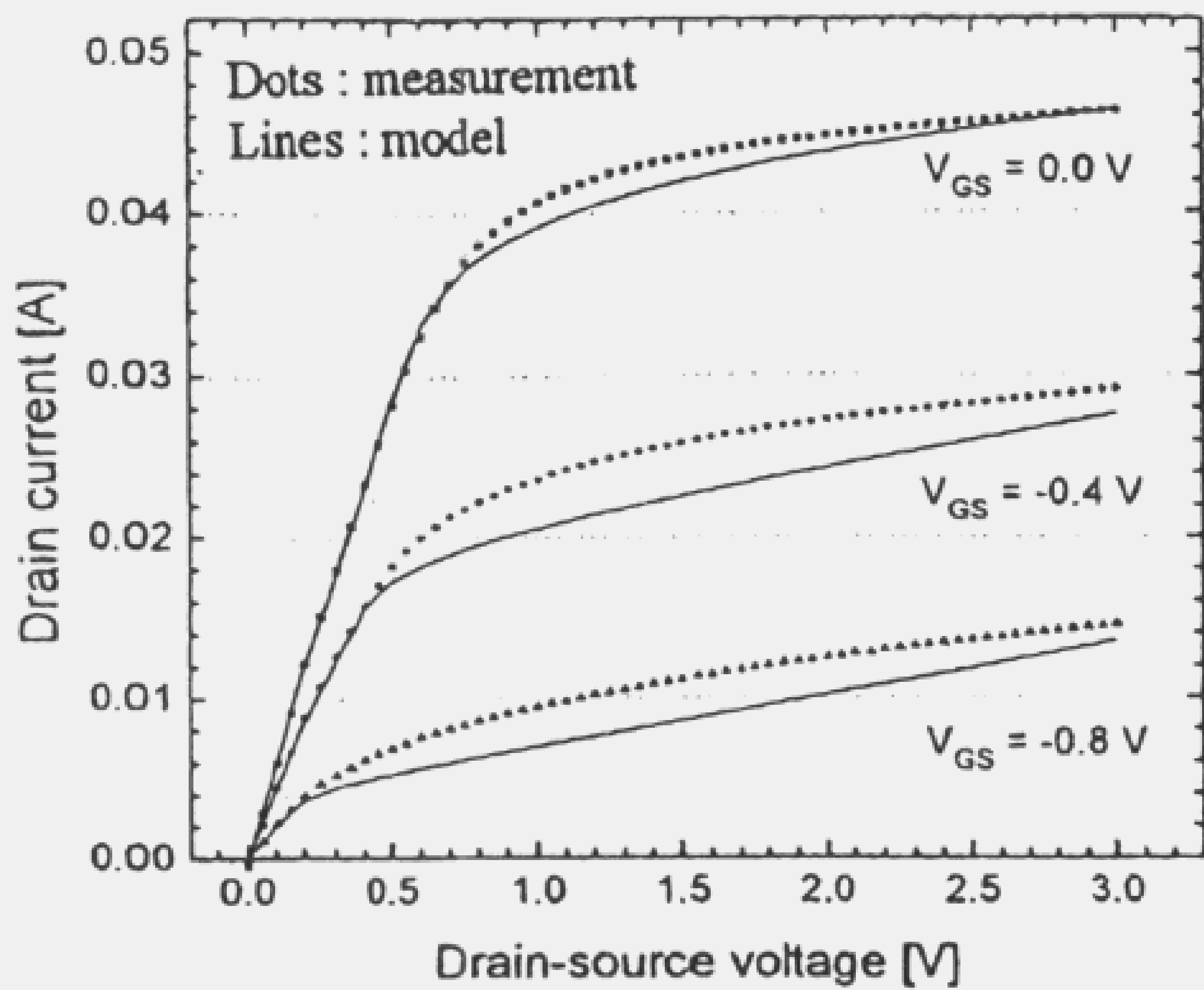

Fig.2. DC I-V characteristics.

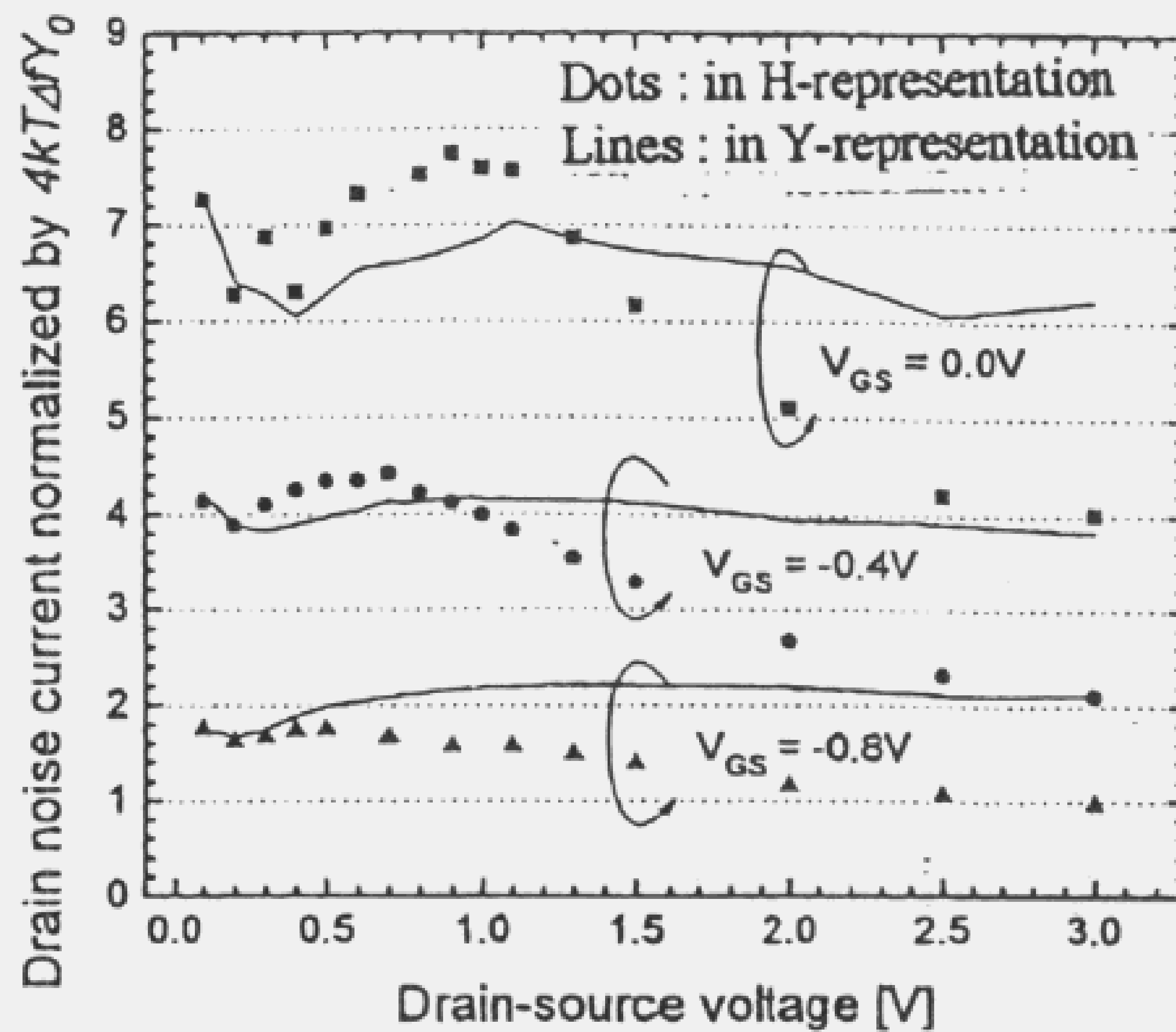

Fig.3. Measured drain noise current vs. V_{DS}.

It is obvious from Eqs.(13)~(14) that the correlation between $v_{gn1,H}$ and $i_{dn1,H}$ is not zero.

To calculate the drain noise, we firstly neglect the displacement current to the gate terminal, meaning current continuity along the channel. Under this assumption, we can use the impedance field method to calculate the open circuit drain noise voltage as below[9]

$$\left\langle v_{dn2}{}^2 \right\rangle = \int_{\text{Region II}} 4q^2 \Delta f D_h \left| \frac{dR_{ds}(x')}{dx'} \right|^2 nWdx'. \tag{15}$$

Here, D_h is high field diffusion constant. $R_{ds}(x)$ has two parallel components. One is the resistance due to the channel length modulation, and the other is to the static feedback effect, σg_m. Using the relation $I_{DS}=qnWv_{sat}$ and $qV_T=kT$, $\langle v_{dn2}{}^2 \rangle$ can be written as

$$\left\langle v_{dn2}{}^2 \right\rangle = 4kT\Delta f \frac{I_{DSS} D_h}{v_{sat} V_T} \frac{-1}{6\sigma^2 g_m{}^2 \lambda} \left[\frac{1+3\alpha \exp(x'/\lambda)}{\left(1+\alpha \exp(x'/\lambda)\right)^3} \right]_0^{\Delta L}. \tag{16}$$

$v_{gn2,H}$ and $i_{dn2,H}$ are easily expressed by v_{dn2} as

$$i_{dn2,H} = \frac{v_{dn2}}{R_{ds}} \left(1 + \frac{g_m R_{ds} C_{gd}}{C_{gs}} \right), \text{ and} \tag{17}$$

$$v_{gn2,H} = -v_{dn2} \frac{C_{gd}}{C_{gs}}. \tag{18}$$

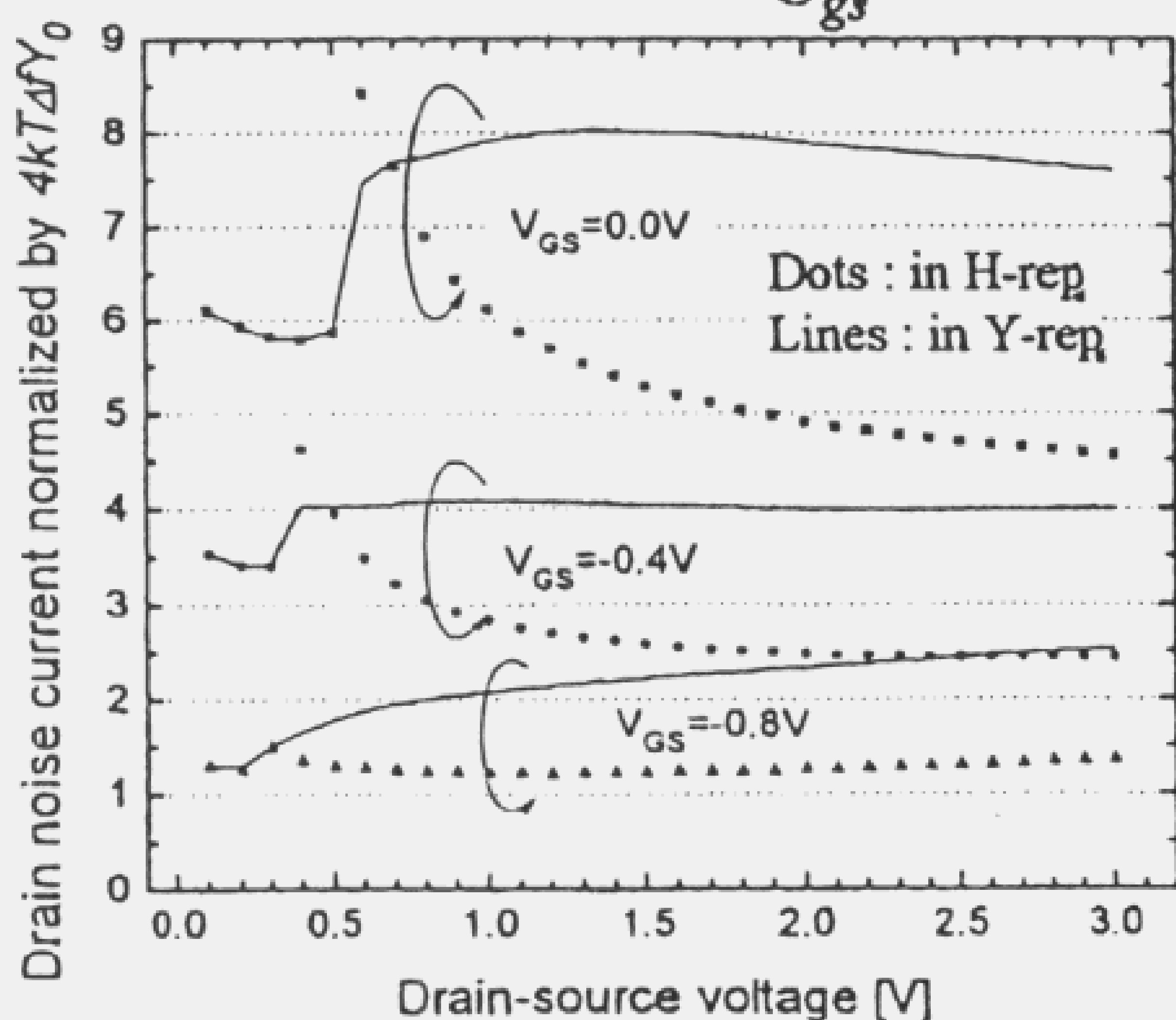

Fig.4. Modeled drain noise current vs. V_{DS}

Table. Measured small signal parameters. MR_{gn} and CR_{gn} are measured and calculated $\langle v_{gn,H}{}^2 \rangle$ normalized by $4kT\Delta f$, respectively.

V_{DS}	1.0			2.0		
V_{GS}	0	-.4	-.8	0	-.4	-.8
r_i [Ω]	5.0	6.4	9.9	5.4	6.9	9.4
g_m[mS]	47	43	32	44	40	32
r_{ds}[Ω]	230	250	250	340	330	310
C_{gs}[pF]	.27	.22	.18	.31	.26	.21
C_{gd}[pF]	.04	.05	.05	.03	.04	.04
MR_{gn}	10	9.0	9.8	12	11	11
CR_{gn}	5.4	6.7	11	5.4	6.4	9.3

4. Measurement and comparison with theory

Both S-parameters and noise characteristics are measured from ion-implanted MESFET whose geometry is 0.5×300 μm^2. The drain saturation current at V_{GS} = 0.0V is 45 mA and the external unit current gain frequency is 22 GHz. The r_g, r_s and r_d values are measured using the conventional method[10]. Since it is not easy to separate C_{gsp} from C_{gs} by s-parameter measurement, we adopt the approximate estimation of C_{gsp}=0.18pF/mm[11].

Fig.2 compares the DC I_{DS}-V_{DS} characteristics between measurement and theory. The overall accuracy is good. The four noise parameters are measured with ATN solid tuner and HP noise figure meter. The intrinsic noise characteristics are Extracted from the measured noise parameters by eliminating the effect of parasitic elements such as r_g, r_s, r_d, C_{gd} and C_{gsp} in Fig.1 using the method in [12].

Fig.3 shows the measured $\langle i_{dn,H}^2 \rangle$ and $\langle i_{dn,Y}^2 \rangle$ versus the drain voltage at several gate bias points. There are several interesting features in Fig.3. Firstly, in linear regime, $\langle i_{dn,H}^2 \rangle$ is almost the same as $\langle i_{dn,Y}^2 \rangle$ for all the gate bias studied in this work. Secondly, in the deep saturation regime, $\langle i_{dn,H}^2 \rangle$ becomes smaller than $\langle i_{dn,Y}^2 \rangle$ and the difference between them increases with increasing V_{GS}. One remarkable feature is that $\langle i_{dn,H}^2 \rangle$ decreases drastically just after the saturation point and becomes constant in the deep saturation regime, while $\langle i_{dn,Y}^2 \rangle$ stays almost constant independently of V_{DS} in saturation regime. Thirdly, near the saturation point, there are bumps both in $\langle i_{dn,Y}^2 \rangle$ and in $\langle i_{dn,H}^2 \rangle$.

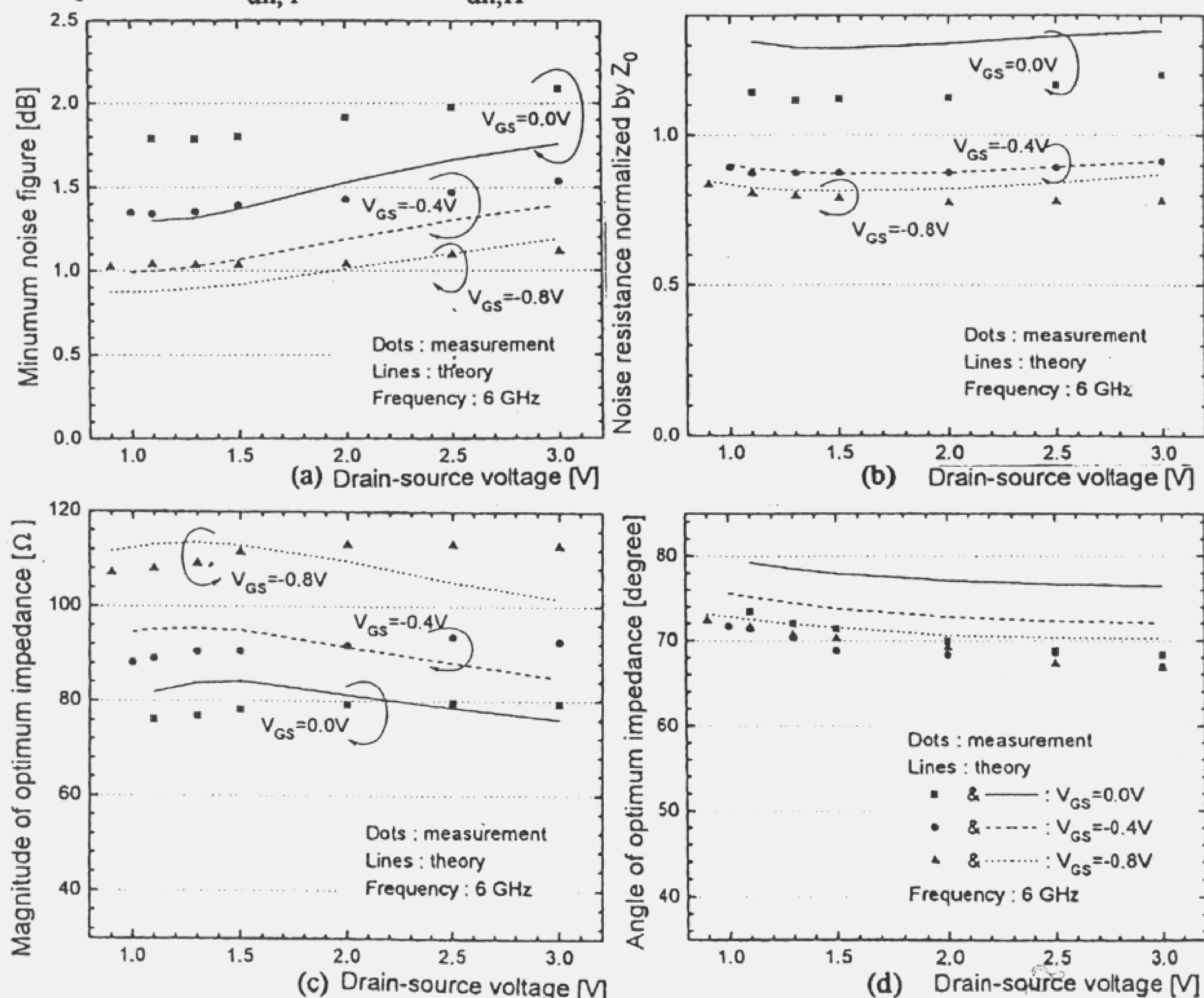

Fig.5. Comparison of four noise parameters between measurement and theory at 6GHz. (a) Minimum noise figure, (b) noise resistance, (c) the magnitude and (d) the angle of optimum impedance.

Moreover, as shown in Table, measured $<v_{gn,H}^2>$ is almost constant independently of V_{DS} as well as V_{GS} in the deep saturation regime. The result of independence on V_{GS} is quite in contrast with the previous results. Both Pospieszalski[3] and Ladbrooke[8] claimed that it is proportional to r_i as a first order approximation. Therefore it is hard to explain why, in our device, $<v_{gn,H}^2>$ is almost constant while the value of r_i changes twice(see Table) as the gate bias varies.

To fit the experimental data, v_{sat}, D_h, γ_0(see Eq.(10))and λ are chosen as 1.2×10^7cm/sec, 11cm^2/sec, 2.3, and 0.055μm, respectively. The values of D_h and λ agree fairly well with the conventionally accepted value of 20 cm^2/sec for D_h[13], 0.1~0.2 of the gate length for λ[5]. The value of γ=2.3 in deep saturation agrees also fairly well with 3 suggested in Ref.[8]. The calculation result of the drain noise current in H- and Y-representation shows good agreement with the measurement as can be seen in Fig.4. The theoretical explanation of the bias dependence of the drain noise current is as follows. The drain noise current from region 2, $<i_{dn2,H}^2>$ begins to be generated after V_{DS} becomes larger than V_{Dsat}. This appears as the increase of the total drain noise current. C_{gd}/C_{gs} is not small near V_{Dsat}, so that $<i_{dn2,H}^2>$ is larger than $<i_{dn2,Y}^2>$(Eq.(17)) This is why total drain noise current in H-representation is larger than in Y-representation near V_{Dsat} at V_{GS}=0 and -0.4V. Since C_{gd} over C_{gs} decreases as MESFET operation goes into the deep saturation regime, $<i_{dn1,H}^2>$ also decreases. Meanwhile, the drain noise current from region 1, $<i_{dn1,H}^2>$ also increases with increasing V_{GS}, because total channel conductance becomes higher. As can be seen from the comparison between measured (Fig.3) and calculated(Fig.4) drain noise, our model explains well the trends of $<i_{dn,H}^2>$ and $<i_{dn,Y}^2>$ as V_{GS}, V_{DS} change. Our model shows somewhat faster saturation of the drain noise current source in the saturation regime compared with the measurement.

5. Conclusion

Drain and gate noise sources and their correlation coefficient for MESFET are formulated based on the large signal I-V and C-V models. The static feedback effect is taken into account, which gives better accuracy in low current regime. The comparison of noise sources and four noise parameters shows reasonably good agreement between measurement and theory in wide range of V_{GS} and V_{DS} for 0.5μm MESFET.

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