Thick Metal CMOS Technology on High Resistivity Substrate for Monolithic 900 MHz and 1.9 GHz CMOS LNAs

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Abstract---**Thick metal CMOS technology on high resistivity substrate (RF CMOS technology) is demonstrated for the RF IC applications, and we firstly implemented it to the monolithic 900 MHz and 1.9 GHz LNAs. The 1.9 GHz LNA shows a *NF* of 2.8 dB that is an excellent noise performance compared with the off-chip matched CMOS LNAs. And the 900 MHz LNA shows a high gain of 18.8 dB and *NF* of 3.2 dB. The proposed RF CMOS technology is a very simple process and shows a high reproducibility, and the monolithic LNAs employing the technology show a good and uniform RF performances in a wafer.**

INTRODUCTION

Recently, CMOS technology has drawn much attention since it allows us RF circuit blocks of portable communications system into one chip [1]-[3]. But the big challenges of CMOS technology for the RF IC applications are how to enhance the quality factor (Q) of spiral inductor without process complexity and how to maximize the RF performance of MOSFET. The spiral inductor fabricated using conventional CMOS technology shows a low Q value due to the substrate loss and inductor metal resistance, so the noise and the gain performance of monolithic CMOS LNA is severely degraded by the on-chip spiral inductors. Therefore the use of on-chip inductors is very limited to the circuit designer [3].

In this paper, we demonstrate thick metal CMOS technology on high resistivity substrate, and successfully implemented it to the monolithic 900 MHz and 1.9 GHz CMOS LNAs. The proposed RF CMOS technology shows a high reproducibility, and the monolithic LNAs employing the technology show a good RF performances.

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RF CMOS TECHNOLOGY

Fig. 1 shows the cross sectional view of the RF CMOS technology, which is 0.8 μm poly-silicon gate CMOS technology on high resistivity (>2 kΩ•cm) substrate with thick (3.1μm) aluminum metal inductor process. By employing the thick metal process and high resistivity substrate, a 13.2 nH inductor shows a Q value of 13 at 1.9 GHz, and the 1~30 nH inductors with the Q of 3~13 range can be easily obtained as shown in Fig. 2 [4]. With the optimization of the MOSFET gate layout, we obtained the minimum noise figure (F_{min}) of a 0.9 dB at 1.9 GHz and a 0.5 dB at 900 MHz, respectively [5].

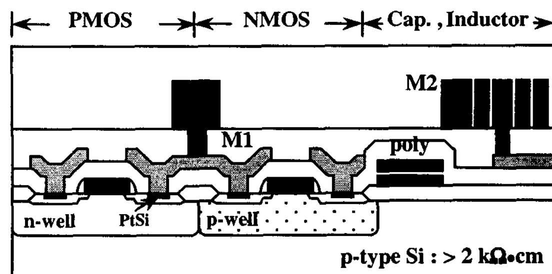

Fig.1. Cross sectional view of the RF CMOS technology. The passive components are placed on the high resistive substrate for the high quality factor.

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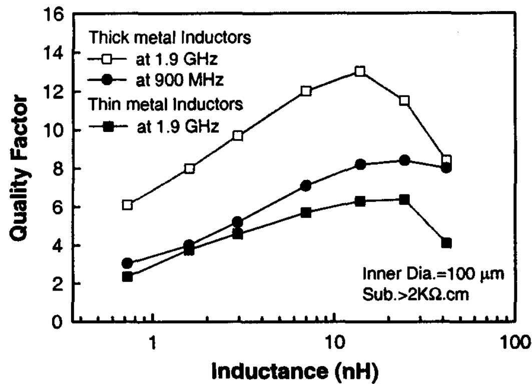


Fig. 2. Quality factor versus inductance of spiral inductors fabricated with thick (3.1μm) and standard thin (1.1 μm) metal process.

LNA DESIGN

Fig. 3 shows the schematic of two stage common source type LNA for 900 MHz and 1.9 GHz. The first stage of the circuit employ a common source with inductive source degeneration type for simultaneous matching of noise and power gain. The bias condition of the second stage transistor M_2 is chosen for the high gain and linearity. Transistors M_3 and M_4 with 10 KΩ resistor R_b for AC blocking forms the biasing circuitry. For the in/output matching element, 5 nH~26 nH inductors and 2~9 nH inductors are used in the 900 MHz and 1.9 GHz LNA, respectively.

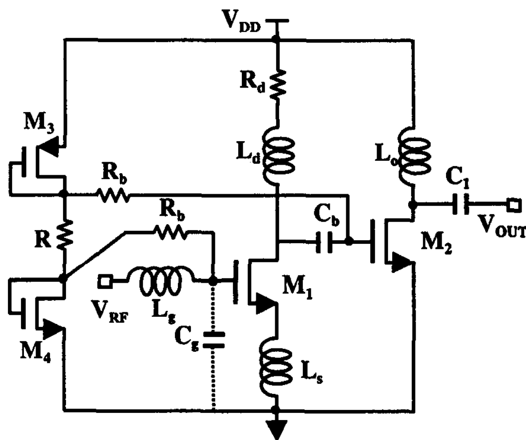
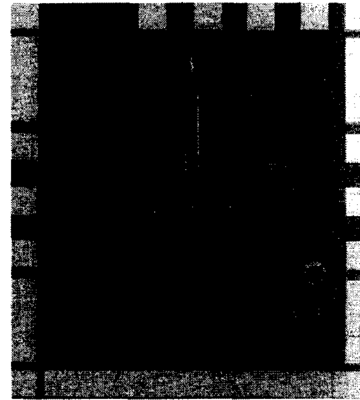
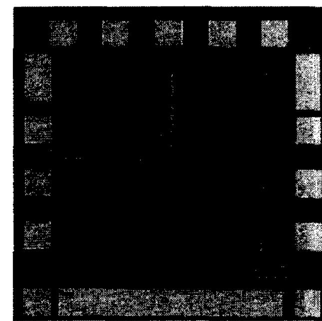


Fig.3. Simplified schematic of the fully integrated 900 MHz and 1.9 GHz LNA. Capacitor C_g is used only for 900 MHz circuit.



(a)



(b)

Fig. 4. Microphotographs of fully integrated LNA fabricated with thick metal process. Chip size of 900 MHz LNA (a) and 1.9 GHz LNA (b) was 1.1 x 1.2 mm^2 and 0.93 x 0.93 mm^2, respectively.

MEASURED RESULTS

Fig. 4 shows the microphotographs of the proposed 900 MHz and 1.9 GHz LNA fabricated using the RF CMOS technology. On wafer s-parameter and noise parameter measurement are carried out using the Network analyzer and ATN setup, respectively.

Fig. 5 shows the measured gain and S_{11} of the 900 MHz LNAs that are randomly selected five chips in a 5-inch wafer. The circuit shows a high gain of 18.8±0.3 dB and a good input match of –15 dB at 875 MHz. And the DC consumption current is 14.7mA at the V_{DD} of 3.6V. The *NF* of the 900 MHz LNA shows a 3.2 dB as shown in Fig. 6. The figure also shows that a 4 dB gain and a 1.4 dB *NF* of the circuit are improved by employing thick metal inductors compared with those of standard thin metal inductors.

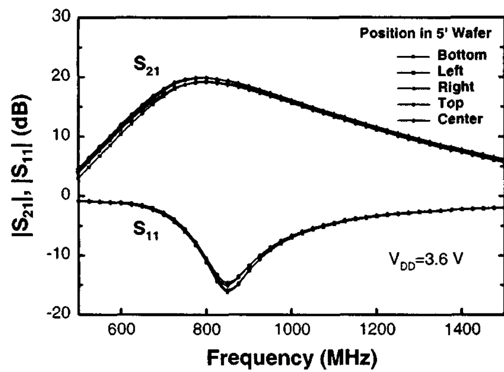


Fig. 5. Measured gain and S_{11} of the 900 MHz LNA. The amplifier shows a good uniformity in 5 inch wafer (V_{DD}=3.6, I_{DD}=14.7 mA).

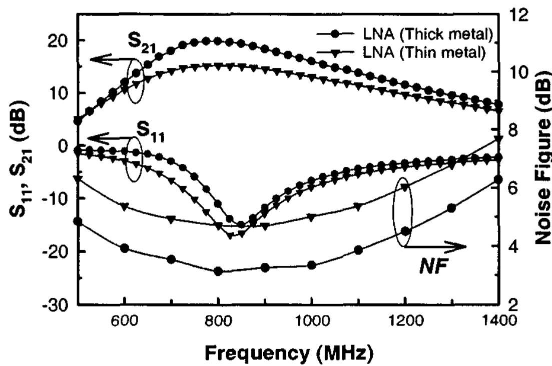


Fig. 6. Measured gain and *NF* of the 900 MHz LNA employing thick metal inductors and thin metal CMOS process.

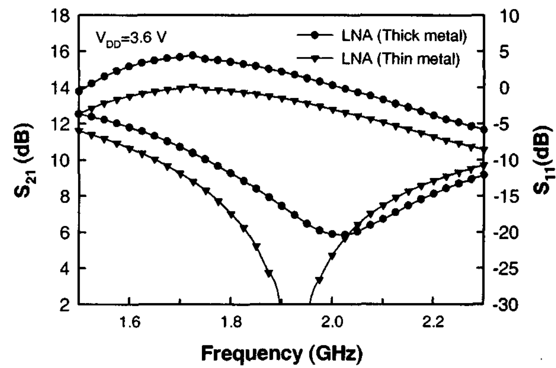


Fig. 7. Measured gain and S_{11} of the 1.9 GHz LNA. The amplifier shows a gain of 15 dB and a S_{11} of −16 dB at 1.9 GHz. (V_{DD}=3.6, I_{DD}=15 mA)

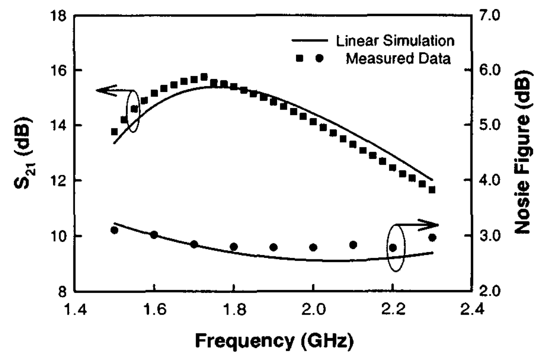


Fig. 8. Measured gain and *NF* of the 1.9 GHz LNA. The measured data shows a good agreement with the simulated one.

Fig. 7 shows the measured gain and S_{11} of the monolithic 1.9 GHz LNA employing the different metal thickness. The circuit fabricated using the thick metal process shows a gain of 15 dB and a S_{11} of −16 dB at 1.9 GHz. And the LNA shows a *NF* of 2.8 dB with the minimum noise figure (F_{min}) of 2.6 dB as shown in Fig. 8. Compared to other CMOS LNA's which usually use the off-chip, or bonding wire inductor as input matching element [1-3], [6-8], this monolithic 1.9 GHz LNA shows the excellent noise figure up to date. And the measured results show a good agreement with the simulated ones using small signal parameters of active and passive devices.

A two-tone inter-modulation intercept point (IP3) measurement is performed on the 900MHz and 1.9 GHz LNA as shown in Fig. 9. The input third-order inter-modulation intercept points of 900 MHz LNA and 1.9 GHz LNA was 1 dBm and 5 dBm input power, respectively.

For low power applications, the V_{DD} of 900 MHz LNA can be reduced to 3 V without severe degradation of the gain and *NF* as shown in Fig. 10. The circuit shows the gain of 16.7 dB and the NF of 3.4 dB at the DC current of 9.1mA.

The performances of 900 MHz and 1.9 GHz LNA are summarized in detail at Table I.

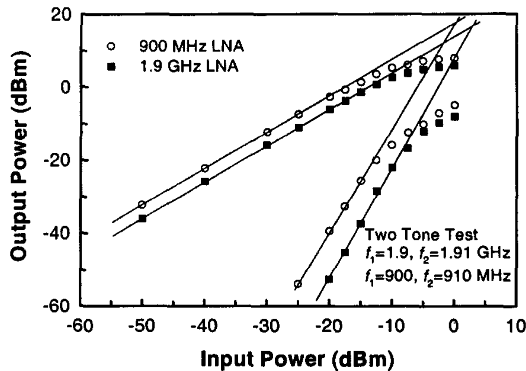


Fig. 9. Two-tone IP_3 measurement of 900 MHz and 1.9 GHz LNA at V_{DD}=3.6V

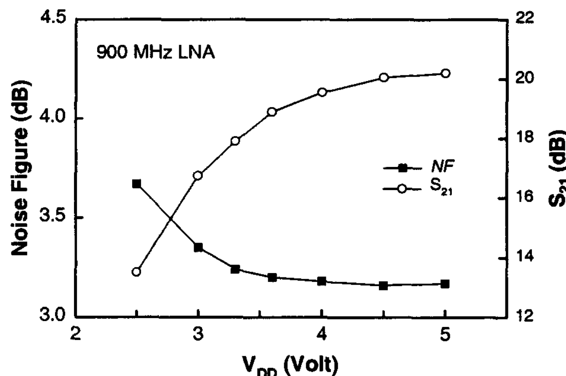


Fig. 10. Measured gain and *NF* of LNA with variation of power supply voltage. The DC consumption current at V_{DD}=3.0 V is 9.1 mA.

Table I. Summary of LNA performance employing the thick metal spiral inductors. (IIP3: input third-order inter-modulation intercept point)

	V_{DD} (V)	Gain (dB)	S_{11} (dB)	S_{22} (dB)	*NF* (dB)	F_{min} (dB)	IIP_3 (dBm)
900 MHz LNA	3.6	18.8	-14	-5.4	3.2	2.7	1.0
1.9 GHz LNA	3.6	15	-16	-6.7	2.8	2.6	5.0

CONCLUSIONS

The RF CMOS technology suitable for the application of RF IC is proposed by employing the high resistivity substrate and thick metal inductor process. The proposed RF CMOS technology is very simple process and shows a high reproducibility. And the monolithic LNAs employing the technology show a good and uniform RF performances in a 5 inch wafer. The 1.9 GHz LNA shows a low *NF* of 2.8 dB. And the 900 MHz LNA shows a high gain of 18.8 dB and *NF* of 3.2 dB. These results confirm that the proposed RF CMOS technology is a promising candidate for the application of *L*-band RF ICs.

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