A Single-Chip 2.4GHz Low-Power CMOS Receiver and Transmitter for WPAN Applications

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***Abstract* – A single chip 2.4GHz low power CMOS receiver and transmitter for WPAN applications are implemented and measured. The receiver uses a low-IF architecture with a poly-phase filter and transistor linearization technique to improve linearity per power, and the transmitter adopts a ROM based direct-conversion architecture for low power consumption and high integrated density. Experimental results show –79dBm of sensitivity, 13dB of receiver NF, -4.5dBm of receiver IIP3, and -4dBm of transmitter output power. The power consumption is 9mW in receiver and 17mW in transmitter at 1.8V, respectively.**

INTRODUCTION

Recently, the ubiquitous network concept has been drawn much attention as a new networking paradigm [1]. The ubiquitous space, networked by Intellectual Property (IP) through WPAN, is composed of human, computer, and other components. Many short-range wireless radios will be used to provide the means of function control and limited data access in the ubiquitous space. These low-rate applications such as WPAN demand low-cost and low-power solutions for their widespread and long-term uses. Low power Bluetooth transceivers, as standardized in IEEE 802.15.1, have been already reported [2]. However, these are too expensive and consuming much power for low rate applications. In our work, for low-cost integration and low-power consumption, low-IF receiver and direct-conversion transmitter are used. I/Q mismatch and LO emission problem have been compromised to achieve acceptable performance.

In 2000, IEEE started to standardize IEEE 802.15.4 for low rate WPAN application. The radio operates with data rate 200kbps spreaded by an 11-bit Barker code, which is occupied 8 channels with 3MHz channel spacing in 2.4GHz ISM band. Because 2.4GHz ISM band is crowded with many interferes, improvement of linearity is a matter of concern in 2.4GHz ISM band. Accordingly, in this work, to implement a radio for 2.4GHz, which lay emphasis on linearity rather than sensitivity, transistor linearization technique in receiver and series feedback using source degeneration by resistor in transmitter are used.

In this paper, the 2.4GHz receiver and transmitter satisfying preliminary specifications of IEEE 802.15.4 are described. The transceiver is implemented in 0.18μm, 1-poly, 6-metal CMOS technology and measured.

RECEIVER/TRANSMITTER ARCHITECTURE

The block diagram of the designed 2.4GHz receiver and transmitter for WPAN application is shown in Fig. 1. In GMSK (h=0.5, BT=0.5) modulation, the spectrum has energy near zero-IF, therefore DC offset and 1/f noise can corrupt modulated signal. The receiver uses low-IF architecture, which discharges received signal from signal corruption by 1/f noise and dc offset. Intermediate frequency is selected as 4MHz by considering digital clock frequency, 1/f noise corner frequency and harmonic mixing. In the receiver path, the RF signal is down-converted to 4MHz I/Q signals by LNA and I/Q mixers, and then the 5^{th} order poly-phase filter is used for channel selection and image rejection capability. Because the filter provides sufficient image rejection, external image rejection filters can be eliminated. These external filters can occur the cost of area, and they have a parasitic effect on the power consumption. Therefore, it is possible to achieve low-power and low-cost receiver by eliminating these additional components. The non-coherent detector which is composed of limiters and a frequency discriminator is also designed in low power consumption.

The transmitter uses direct-conversion architecture for high level of integration and low power consumption. In the transmitter path, I/Q ROM-based DSSS GMSK signals are directly up-converted to 2.4GHz by DAC, LPF, I/Q mixer and amplified by differential driver amplifier with high power efficiency. The GMSK modulation is constant envelope modulation. Such waveform carries information only in the zero-crossing point and can be processed by a nonlinear amplifier with high power efficiency, which has a positive effect on the transmitter power consumption.

To improve the performance, calibration circuit is added. It takes the role of mismatch calibration from process variation, as well as gain control and bias current control in receiver and transmitter. It is controlled by digital baseband chip through serial interface.

RECEIVER DESIGN

Receiver linearity is very important characteristic in the polluted 2.4GHz ISM band. Fig. 2 shows the merged LNA and mixer adopting the multiple gated transistor (MGTR) technique, which can effectively reduce gm nonlinearity of transconductor and give more than 4dB receiver IIP3 improvement at the same current. As illustrated in Fig. 3, in MGTR technique, negative gm'' peak of main transistor can be cancelled by the positive gm'' peak of the properly sized additional transistor. Transfer function of the additional transistor is shifted by gate bias voltage. Because additional transistor is biased subthreshold voltage, this technique does not require any additional power consumption [3].

The 5th order polyphase filter is designed using active RC type for good linearity, channel selection, and image rejection. As shown in Fig. 4, the complex filter is designed by moving the low pass filter pole to the complex pole location. Fig. 5 shows the frequency characteristic of polyphase filter. The deviation of center frequency and bandwidth according to RC variation is controlled by the digital trimming of a switched capacitor array.

Limiter makes the desired signal adequate voltage level for demodulation. Limiter consists of 5-stage limiting amplifiers and 4-stage RSSI.

As shown in Fig. 6, frequency demodulator is composed of differentiator, multiplier, and LPF. It multiplies I path signal with differential Q path signal and Q path signal with differential I path signal, respectively. It takes the demodulation by adding the multiplied products [4].

Data slicer with peak and valley detector finds the proper threshold voltage from the output of the demodulator and discriminates between logic-low and logic-high with the output of the demodulator and the threshold voltage.

TRANSMITTER DESIGN

The transmitter takes analog I/Q input signals from digital base-band, followed by variable gain gaussian LPFs, which shape modulated signal spectrum and reject the undesired harmonics from DAC. A LPF is implemented as the 4th order active RC filter with constant group delay. Its 3dB bandwidth is corrected by the digital trimming of a switched capacitor bank, and the gain is controlled by the digital switching of feedback resistors. Fig. 7 shows the frequency characteristic of the LPF.

Both the linearity and the matching performance of I/Q up-conversion mixer affect the quality of the modulated signal. The unwanted signal from 3rd order non-linearity must be small enough that the output spectrum meets the required transmission mask. The up-mixer is implemented as double balanced Gilbert mixer with resistive degenerations, which helps to improve the linearity. The mismatch of quadrature signals leads to cross-talk between the two data streams modulated on the quadrature phase of the carrier [5]. To avoid the mismatch, symmetric layout is done and the LO emission which is from differential mismatch is also suppressed sufficiently.

A driver amplifier consists of a gain stage and output stage, as shown in Fig. 8. The gain stage uses a cascode scheme and feedback resistor and MOS capacitor for stability. For input matching, it uses capacitive matching to boost input voltage level. This can reduce entire transmitter current consumption. The constant envelope modulation scheme allows using power efficient class-C amplifier in output stage for low power transmitter

EXPERIMENTAL RESULTS

The chip has been fabricated in 0.18μm CMOS process. The active power consumption is 9mW and 17mW at 1.8V supply voltage in receiver and transmitter, respectively. The measured overall receiver NF, IIP3 and sensitivity are 13dB, –4.5dBm and –79dBm, respectively. The receiver eye diagram is shown in Fig. 9. Fig. 10 and Fig. 11 show baseband I/Q waveforms and the GMSK output spectrum at transmitter output when GMSK modulated signals are applied from external digital baseband, respectively. Table 1 shows the performance of receiver and transmitter. The chip photograph is shown in Fig. 12.

CONCLUSION

A single chip 2.4GHz low power CMOS receiver and transmitter for low rate WPAN application are designed and measured. To achieve the low power consumption and high integration, low-IF architecture in receiver and direct up-conversion architecture in transmitter are used. For high linearity performance, transistor linearization technique in receiver and resistive degeneration in transmitter are used. The receiver and transmitter meet the preliminary specifications of WPAN (IEEE802.15.4). The single-chip 2.4GHz low-power receiver and transmitter for WPAN show the feasibility for low-cost and low-power commercial application.

ACKNOWLEDGEMENT

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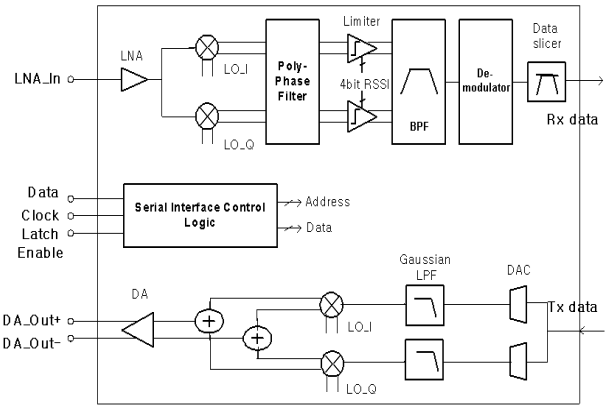

Fig 1. Block diagram of the 2.4GHz receiver and transmitter for WPAN

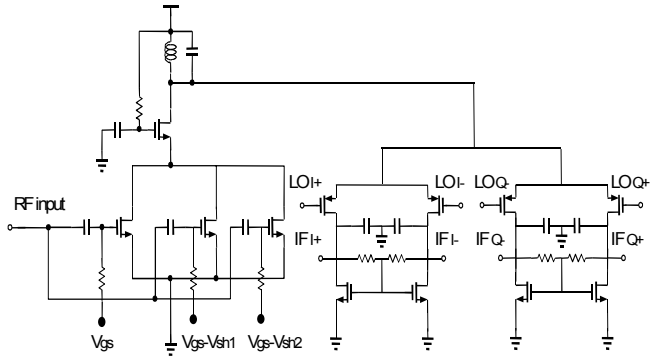

Fig. 2. Circuit schematic of the receiver front-end

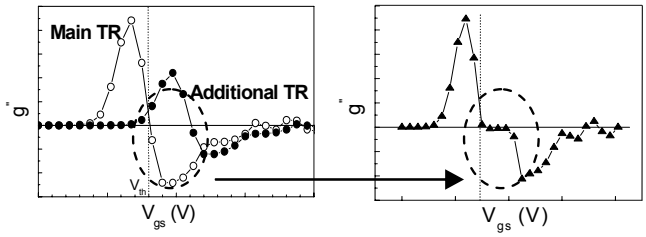

Fig. 3. Illustrations of MGTR technique

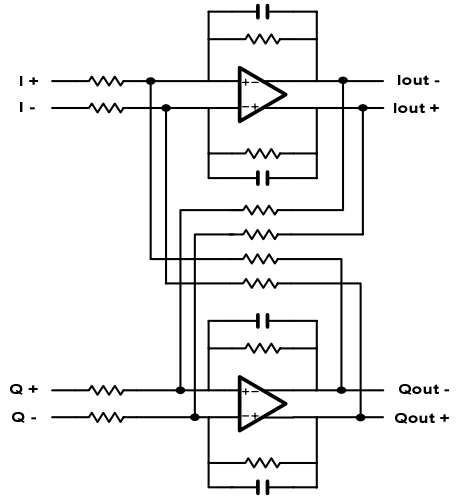

Fig. 4. 1st order complex filter

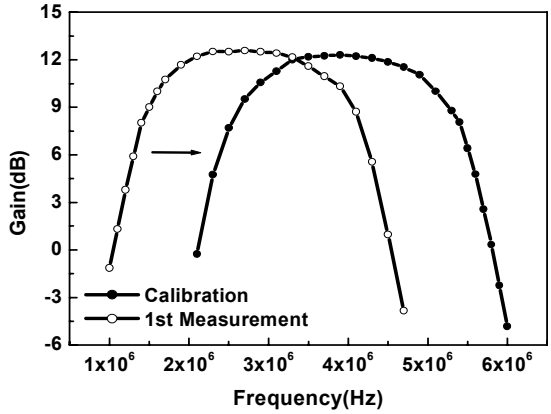

Fig. 5. Frequency characteristic of digitally trimmed polyphase filter

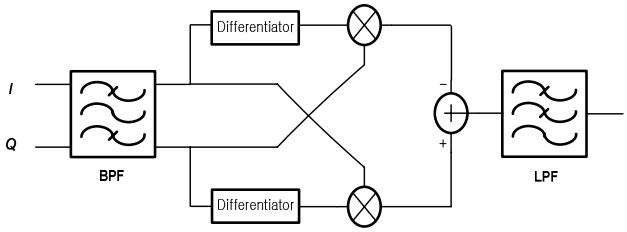

Fig. 6. Block diagram of frequency demodulator

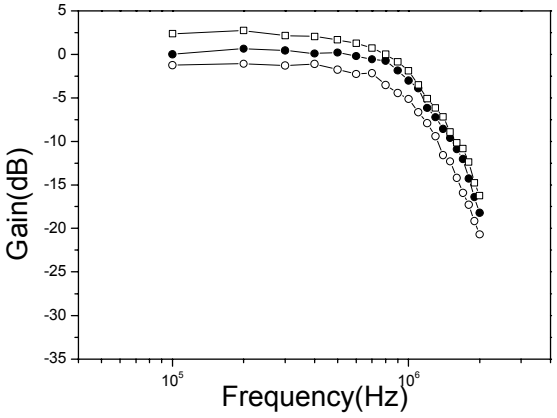

Fig. 7. Frequency and Gain characteristic of LPF

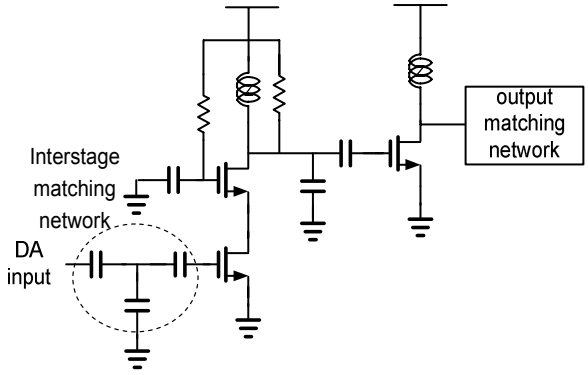

Fig. 8. Drive anplifier schematic

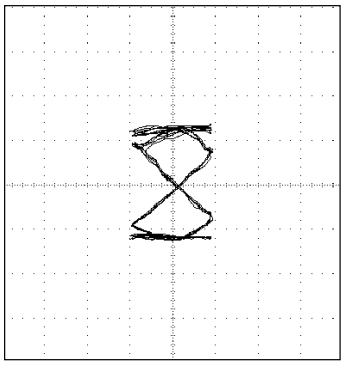

Fig. 9. Receiver output eye diagram

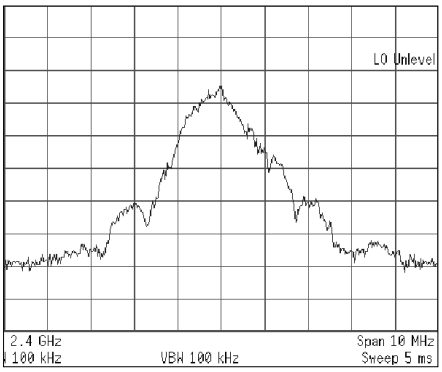

Fig. 11. Transmitter output spectrum

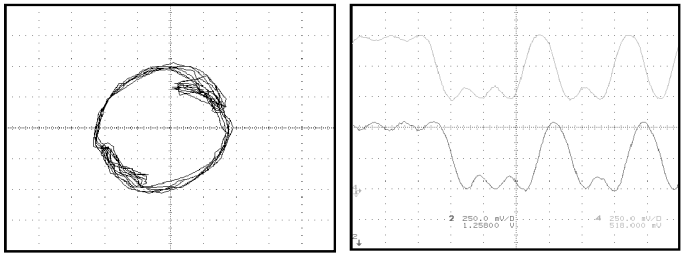

Fig. 10. The GMSK modulated signal

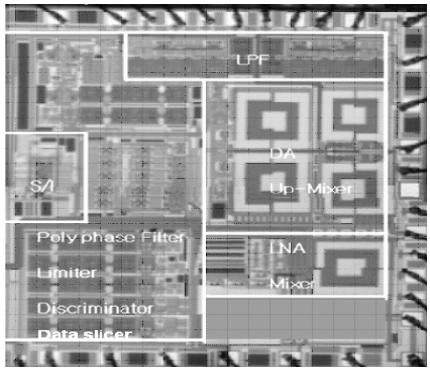

Fig. 12. Chip photograph of the receiver and transmitter

Table 1. Performance of receiver and transmitter

Power supply	1.8 V
Receiver sensitivity	- 79dBm
Receiver IIP3	- 4.5dBm
Receiver image rejection	> 30dB
Transmitter output power	- 4dBm
Receiver power consumption	9mW
Transmitter power consumption	17mW
Die size	2.3mm x 2.5mm