Analytical Drain Thermal Noise Current Model Valid for Deep Submicron MOSFETs

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***Abstract*—In this paper, a physics-based MOSFET drain thermal noise current model valid for deep submicron channel lengths was derived and verified with experiments. It is found that the well-known $\mu Q_{\rm inv}/L^2$ formula, previously derived for long channels, remains valid for short channels. Carrier heating in the gradual channel region was taken into account implicitly with the form of diffusion noise source and then impedance field method taking velocity saturation effect was used to calculate the external drain thermal noise current. The derived model was verified by experimental noise for devices with channel lengths down to 0.18 μm. Excellent agreement between measured and modeled drain thermal noise was obtained for the entire $V_{\rm GS}$ and $V_{\rm DS}$ bias regions.**

***Index Terms*—Carrier heating, channel length modulation, impedance field method, inversion channel charge, RF CMOS, thermal noise, velocity saturation.**

I. Introduction

DUE TO continuous reduction of channel length in CMOS technologies, CMOS has become a viable candidate for radio frequency (RF) applications. Accurate modeling of RF CMOS is very important to optimize circuit performance and yield as well as to decrease develop time. In spite of lots of progress in RF CMOS current–voltage (*I–V*) and charge–voltage (*Q–V*) modeling [1], [2], the thermal noise behavior in short-channel MOSFETs is not well understood yet and even controversial. Among many noise sources, the drain current noise has been found to be the dominant noise source and most of the analytical CMOS low noise amplifier is designed assuming this to be proportional to drain conductance at $V_{\rm DS} = 0$ V employing excess factor, γ [3], [4]. It has often been reported that the thermal noise generated in short-channel MOSFETs is higher than predicted by the long-channel noise model. Jindal [5] and Abidi [6] reported the significant excess noise even in the linear regime as well as in the saturation regime. And there are many literatures to try to explain such increase of the thermal noise by introducing hot electron effect in velocity saturation region [5]–[8]. However, recently reported thermal noise value of 0.18 μm MOSFET does not show so large excess factor. Excess factor for 0.18 μm n-channel MOSFET does not exceed more than two at strong inversion [3], [9], [10]. Recently, many experimental and simulation works have addressed that the noise generated due to hot electrons in velocity saturation region is negligible [9]–[11].

We suspect that part of this controversy has originated from the measurement accuracy. So the noise measurement accuracy has to be confirmed at first. And many previous results have addressed the thermal noise only at saturation regime. However, since the change of thermal noise with drain bias is basically most prominent in the linear regime, modeling the noise in the linear regime is very important to obtain a basic insight of noise behavior. Especially, noise comparison between theory and experiment at $V_{\rm DS} = 0$ V is very important for checking measurement accuracy as well as noise calibration. As far as we know, drain noise measurement covering entire $V_{\rm DS}$ regions has been seldom reported for short-channel MOSFETs except the one in [12]. And the velocity saturation effect should be considered for short-channel MOSFETs. However, since the accurate impedance field in short-channel devices was not used in the previous models, they did not correctly take into account the velocity saturation effect.

In this paper, the drain thermal noise model for short-channel MOSFETs, including velocity saturation effect and carrier heating effect, is derived and verified with extensively measured noise from linear to saturation regime. The accuracy of measured noise data was checked carefully. In Section II, physics underlying the thermal noise is presented in detail and an analytical model is derived. In Section III, extraction procedures of parameters for modeling the noise are described. Finally, the model verifications are discussed in Section IV.

II. Derivation of Drain Thermal Noise Current Model

A noise modeling approach was proposed by Van der Ziel [13], which was based on Shockley's theory [14]. Using concept of linear transmission line, Klaassen [15] refined this approach and offered a basic insight of noise behavior in the long-channel MOSFETs. Such an approach is based on thermal noise formulation of infinitesimal linear ohmic resistor distributed along the channel. However, since the mobility of carriers in short-channel MOSFETs is degraded due to the lateral electric field, the infinitesimal channel segment cannot be regarded as a linear resistor any more. Therefore, we should recalculate the thermal noise for short-channel MOSFETs. To calculate the drain thermal noise in short-channel MOSFETs, the impedance field method [16] was adopted taking the mobility degradation along the channel into account.

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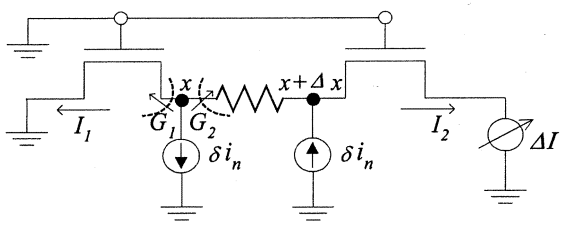

Fig. 1. Norton represented current noise source is divided into two current noise sources, which have same amplitude but are oppositely directed. Impedance field can be calculated by using small signal conductance, G_1 and G_2.

A. Calculation of Drain Thermal Noise Current

The channel of a MOSFET is divided into two regions. One is the so called gradual channel region (region I) with length of $L_{\rm elec} = L_{\rm eff} - \Delta L$ and the other is velocity saturation region (region II) with length of ΔL. Since it was argued and shown recently that the contribution of the carriers in the velocity saturation region to the drain thermal noise current is negligible [3], we only considered the contribution of the carriers in the gradual channel region to formulate the drain thermal noise. The infinitesimal thermal noise current source, δi_n, is distributed along the gradual channel region. In the impedance field method, the noisy segment located from x to $x+\Delta x$ is modeled as a noiseless segment with a Norton current generator representing the local current fluctuation and the current noise source is divided into two current noise sources, which have the same amplitude but opposite direction at x and $x+\Delta x$ as shown in Fig. 1. ΔI is the short-circuited drain noise current contributed by two local noise sources at x and $x+\Delta x$. The local noise source is given by the diffusion noise [17]

$$\langle \delta i_n^2 \rangle = 4q^2 \Delta f D_n n_{\rm inv} \frac{W}{\Delta x} \tag{1}$$

where q is the electronic charge, Δf is the measurement bandwidth, D_n is the diffusion coefficient, $n_{\rm inv}$ is the areal carrier number density, W is the device width, and the direction of x is along the channel. To calculate the impedance field, we write the drain drift current with mobility degradation effect as

$$I_d = g_o(V) \frac{\left(\frac{dV}{dx}\right)}{1 + \frac{\left(\frac{dV}{dx}\right)}{E_C}} \tag{2}$$

where $g_o(V) = \mu_{\rm eff} W(q n_{\rm inv}) = \mu_{\rm eff} W C_{\rm ox}(V_{\rm GT} - \alpha V)$, $\mu_{\rm eff}$ is the gate effective mobility, $C_{\rm ox}$ is the gate oxide capacitance per unit area, $V_{\rm GT}$ is the gate overdrive voltage $(V_{\rm GS} - V_{TH})$, V is the source-referenced channel potential at x, α is the coefficient accounting for the bulk charge effect, and E_C is the critical field at which the carrier velocity becomes saturated. Integrating (2), we find drain currents of two MOSFETs shown in Fig. 1 with length x and $L_{\rm elec} - x$ by

$$I_1 = \frac{\int_0^V g_o(V) dV}{x + \frac{V}{E_C}} \text{ and}$$
$$I_2 = -\frac{\int_V^{V_{\rm DS}} g_o(V) dV}{L_{\rm elec} - x + \frac{(V_{\rm DS} - V)}{E_C}} \tag{3}$$

respectively, where the direction for each current is indicated in Fig. 1. Note that $I_1 = -I_2$ from the current continuity. From (3), the left side and right side small signal conductance $(\partial I / \partial V)$, which is denoted as G_1 and G_2, respectively, is obtained as follows:

$$G_1 \cdot \left(x + \frac{V}{E_C} \right) + \frac{I_1}{E_C} = g_o(V) \tag{4a}$$
$$G_2 \cdot \left(L_{\rm elec} - x + \frac{(V_{DS} - V)}{E_C} \right) - \frac{I_2}{E_C} = g_o(V). \tag{4b}$$

Subtracting (4b) from (4a), we obtain

$$\frac{G_2}{(G_1 + G_2)} = \frac{\left(x + \frac{V}{E_C} \right)}{(L_{\rm elec} + \frac{V_{\rm DS}}{E_C})}. \tag{5}$$

Then, the drain noise current due to two local noise sources at x and $x + \Delta x$ is given by

$$\Delta I = \delta i_n \left(\left. \frac{G_2}{G_1 + G_2} \right|_{x+\Delta x} - \left. \frac{G_2}{G_1 + G_2} \right|_{x} \right)$$
$$= \delta i_n \left(\frac{\Delta x + \frac{\Delta V}{E_C}}{L_{\rm elec} + \frac{V_{\rm DS}}{E_C}} \right). \tag{6}$$

Using $I_d(\Delta x + \Delta V / E_C) = g_o(V) \Delta V$, (6) can be expressed as

$$\Delta I = \delta i_n \frac{g_o(V) \Delta V}{I_d (L_{\rm elec} + \frac{V_{\rm DS}}{E_C})}. \tag{7}$$

This gives the contribution of the noisy element located at between x and $x + \Delta x$ to the drain terminal current noise. Assuming that the contributions of all similar elements in the channel are uncorrelated, the spectral density of the total drain current noise results in

$$\langle i_{dn}^2 \rangle = \sum \langle \Delta I \rangle^2$$
$$= \sum 4q^2 \Delta f D_n n_{inv} \frac{W}{\Delta x} \cdot \frac{g_o^2(V) \Delta V^2}{I_d^2 (L_{\rm elec} + \frac{V_{\rm DS}}{E_C})^2}. \tag{8}$$

By substituting $\Delta x = (g_o(V)/I_d - 1/E_c)\Delta V$, (8) leads to

$$\langle i_{dn}^2 \rangle = \sum 4q^2 \Delta f D_n n_{inv} W \cdot \left(\frac{g_o(V)}{I_d} - \frac{1}{E_C} \right)^{-1} \cdot \frac{g_o^2(V) \Delta V}{I_d^2 (L_{\rm elec} + \frac{V_{\rm DS}}{E_C})^2}. \tag{9}$$

In order to obtain the numerical solution of the drain terminal noise given by (9), the electric field dependences of the diffusivity must be given. The diffusivity in the gradual channel region is nearly constant, independent of the electric field because the decrease of the mobility with electric field is compensated by the increase of electron temperature. Therefore, we assume that the diffusion coefficient is constant over the channel [18], [19]

$$D_n = D_o = \left(\frac{k T_o}{q} \right) \mu_{\rm eff} \tag{10}$$

where D_o is the diffusion constant at low field, k is the Boltzmanns constant, and T_o is the ambient temperature. From (2), we can obtain a useful relation

$$\frac{g_o}{g_o - \frac{I_d}{E_C}} = 1 + \frac{E}{E_C}. \tag{11}$$

Substituting (10) into (9) and using (11) leads to

$$\langle i_{dn}^2 \rangle = \frac{4kT_o\Delta f}{I_d L_{\rm elec}^2 \left(1+\frac{V_{\rm DS}}{L_{\rm elec}E_C}\right)^2} \int_0^{V_{\rm DS}} g_o^2(V)\left(1+\frac{E}{E_C}\right)dV. \tag{12}$$

Note that in the case of $E_C \to \infty$ (or long-channel limit) (12) reduces to (13), which coincides with that derived earlier [17], as it should do

$$\langle i_{dn,long}^2 \rangle = \frac{4kT_o\Delta f}{I_d L_{\rm elec}^2} \int_0^{V_{\rm DS}} g_o^2(V)dV. \tag{13}$$

If we ignore the heating effect of electrons in the gradual channel region, namely we assume the thermal equilibrium prevails in gradual channel region ($D_n = kT_o/q \cdot \mu_{\rm eff} \cdot 1/(1+E/E_C)$), the drain thermal noise would be given as follows:

$$\langle i_{dn,equ}^2 \rangle = \frac{4kT_o\Delta f}{I_d L_{\rm elec}^2 \left(1+\frac{V_{\rm DS}}{L_{\rm elec}E_C}\right)^2} \int_0^{V_{\rm DS}} g_o^2(V)dV. \tag{14}$$

The comparison between (12) and (14) to the measured data will be shown in the Section IV.

B. Expressing Drain Noise Current With Inversion Charge

Equation (12) is a very complicated expression. Therefore, let us approximate (12) to obtain compact analytical equation. If we approximate $(1+E/E_C) \approx (1+V_{\rm DS}/L_{\rm elec}E_C)$ in (12), it becomes

$$\langle i_{dn}^2 \rangle \approx 4kT_o\Delta f G_{\rm do} \frac{1-u+\frac{u^2}{3}}{1-\frac{u}{2}}. \tag{15}$$

Here, $G_{\rm do} = (\mu_{\rm eff} W C_{ox} V_{\rm GT}/L_{\rm eff})$ is the intrinsic drain conductance at $V_{\rm DS} = 0$ V, and $u = \alpha V_{\rm DS}/V_{\rm GT}$. On the other hand, we can express the total inversion charge ($Q_{\rm inv}$) as a function of applied biases:

$$\begin{aligned} Q_{\rm inv} &= \frac{1}{\mu_{\rm eff}} \int_0^{L_{\rm elec}} g_o(x)dx \\ &\approx \left(\frac{L_{\rm elec}^2}{\mu_{\rm eff}}\right) G_{\rm do} \left(\frac{1-u+\frac{u^2}{3}}{1-\frac{u}{2}}\right). \end{aligned} \tag{16}$$

From (15) and (16), we finally obtain the following simple and closed drain thermal noise form expressed by total inversion charge, $Q_{\rm inv}$:

$$\langle i_{dn}^2 \rangle \cong 4kT_o\Delta f \frac{\mu_{\rm eff}}{L_{\rm elec}^2} Q_{\rm inv}. \tag{17}$$

Note that $L_{\rm elec} = L_{\rm eff} - \Delta L$ is the length of the gradual channel region, not the length of total channel region and $\mu_{\rm eff}$ is only gate bias dependent effective mobility, not the mobility including the degradation due to lateral field. The maximum difference between (12) and (17) occurs in between and is numerically calculated to be less than 5% for all channel lengths, gate biases, and drain biases. Thus we can conclude that (17) is simple and accurate enough to be useful for all practical engineering purpose. The same equation was derived for long-channel MOSFETs, although it did not take into account the velocity saturation effect and assumed thermal equilibrium in the gradual channel region [20]. In long channel, the impedance field of local current noise source in gradual channel region is constant along the channel, i.e., $\Delta I = \delta i_n(\Delta x/L_{\rm elec})$, which naturally makes the drain thermal noise proportional to the total inversion charge. Compared to the impedance field of long channel, however, the impedance field of short channel is dependent on the position and decreases at source side and increases at drain side. When it is collaborated with carrier heating effect expressed by (10), the decrease of noise contribution of source side is approximately balanced with the increase of contribution of drain side, which makes the drain thermal noise in short channel proportional to the total inversion charge. We have shown rigorously the well-known formula, $\mu_{\rm eff}Q_{\rm inv}/L_{\rm elec}^2$, which was valid for the long channel, can be extended into the short channel. More detailed steps to obtain (15) and (16) are in Appendix I.

III. Characterization of MOSFET Device Parameters

To verify the drain thermal noise model shown in (17) for short-channel MOSFETs, effective channel length ($L_{\rm eff}$), effective mobility ($\mu_{\rm eff}$), and total inversion charge ($Q_{\rm inv}$) should be obtained accurately. In this section, extraction procedures to obtain the above electrical parameters will be described. N-channel devices with gate length of 0.5, 0.35, 0.25, and 0.18 μm, were chosen for comparison. Each finger width and the number of fingers were fixed to 5 μm and 16, respectively. V_{TH}'s of all the DUT were almost the same about 0.42 V.

So far we have derived the drain thermal noise model in terms of intrinsic applied biases. In fact, both the parasitic series resistances, R_{dc} and R_{sc}, play an important role in determining the intrinsic biases. R_{dc} and R_{sc} include the drain/source resistances in MOSFET, interconnection resistances in GSG pad layout, and cabling resistances from DC source to test fixture. These resistances may be accounted for by using the following expressions relating the intrinsic gate-source and drain-source voltages, $V_{\rm GS}$ and $V_{\rm DS}$, to the extrinsic gate-source and drain-source voltages, $V_{\rm gs}$ and $V_{\rm ds}$

$$\begin{aligned} V_{\rm GS} &= V_{\rm gs} - I_d R_{sc} \\ V_{\rm DS} &= V_{\rm ds} - I_d(R_{dc}+R_{sc}). \end{aligned} \tag{18}$$

For convenience, we measured the thermal noise as a function of $V_{\rm ds}$ at constant $V_{\rm gs}$ and transformed the extrinsic biases into intrinsic biases using (18).

A. Determination of Effective Channel Length and Source/Drain Resistance

The accurate determination of the effective channel length ($L_{\rm eff}$) is very important for the analysis of the device modeling. The reduction of channel length ($\delta L = L_{\rm mask} - L_{\rm eff}$), where $L_{\rm mask}$ is the drawn gate length, and series source/drain resistance ($R_{\rm sd}$) are extracted from the measured ac channel resistance ($R_{\rm do}$) at $V_{\rm DS} = 0$ V versus $L_{\rm mask}$ [21]. All the lines were crossed at one point, where $\delta L = 36.5$ nm and $R_{\rm sd} = 2.495\ \Omega$ were obtained [10]. Recently, a new method to extract effective channel length by using the scalability of $C_{\rm gb}$ in accumulation region has been proposed [22]. We obtained $\delta L = 30$ nm using the method, which is close to that obtained from above method.

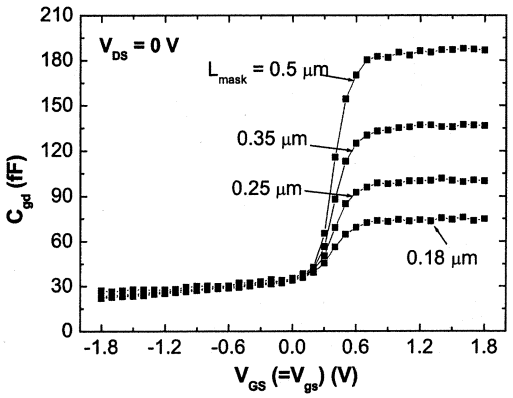

Fig. 2. Measured gate-channel capacitance, $C_{\rm gd}$, at $V_{\rm DS} = 0$ V for various channel lengths as a function of gate bias.

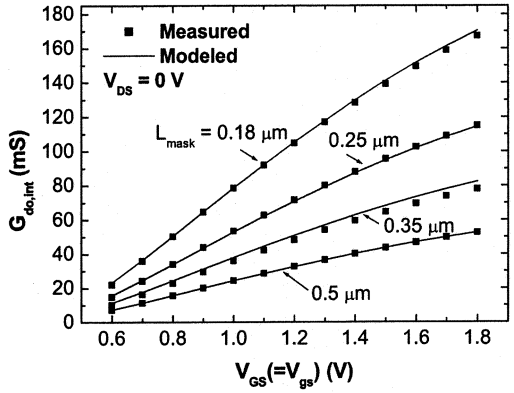

Fig. 3. Measured (symbol) intrinsic conductance $G_{\rm do,int}$ was excellently modeled (line) for various channel lengths using the obtained $L_{\rm eff}$, $\mu_{\rm eff}$, and $Q_{\rm inv}$, which shows the accurate parameter extraction.

B. Extraction of Mobility and Inversion Charge

Conventionally, the effective mobility $(\mu_{\rm eff})$ is extracted from long-channel devices, where source and drain resistance are negligible. However, in the pocket-implanted devices, the mobility of short-channel devices can differ from that of long-channel devices, because average substrate doping concentrations are different. Recently a new method to extract the mobility of short channel was proposed [23]. Fig. 2 shows the measured gate-channel capacitance $(C_{\rm gd})$ at $V_{\rm DS} = 0$ V with various $V_{\rm GS}$. The capacitance was extracted from the measured S-parameters. There are two distinct regions in $C_{\rm gd}$ characteristics with respect to $V_{\rm GS}$. The capacitance–voltage *(C–V)* characteristics in the one region is independent of device channel length and the characteristics in the other is strongly dependent on channel length. The former is considered to be contributed from the parasitic component and the latter from the intrinsic component. The total charge, $Q_{\rm tot}$, was obtained by integrating the measured $C_{\rm gd}$ with respect to $V_{\rm GS}$

$$\begin{aligned}|Q_{\rm tot}(V_{\rm GS}, V_{\rm DS}=0V)| &= \int_0^{V_{\rm GS}} 2C_{dg}dV_{\rm GS}^* \\ &= \int_0^{V_{\rm GS}} 2C_{\rm gd}dV_{\rm GS}^* \\ &= CL_{\rm mask} + D \end{aligned} \tag{19}$$

where $C = Wq_{\rm inv}$ and D includes charge associated with parasitic capacitance. We used the reciprocal and symmetrical characteristics of C_{sg} and C_{dg} at $V_{\rm DS} = 0$ V in (19). The C and D were determined by linear regression of $Q_{\rm tot}$ with $L_{\rm mask}$. The effective mobility was then calculated by using $\mu_{\rm eff} = 1/(AC)$ [23], where A is the slope of the total resistance versus $L_{\rm mask}$. $Q_{\rm inv}$ was obtained by using $Q_{\rm inv} = CL_{\rm eff}$. Using $Q_{\rm inv}$, $\mu_{\rm eff}$, and $L_{\rm eff}$, the intrinsic conductance of the MOSFET $(G_{\rm do,int})$ at $V_{\rm DS} = 0$ V was calculated to be $(\mu_{\rm eff}Q_{\rm inv})/L_{\rm eff}^2$. Measured $G_{\rm do,int}$ was excellently modeled with extracted mobility, inversion charge, and effective channel length, as shown in Fig. 3, which shows the validity of extraction procedures. Accurate $G_{\rm do,int}$ -modeling is very important with respect to noise modeling, since it determines the thermal noise value at $V_{\rm DS} = 0$ V by the Nyquist theorem.

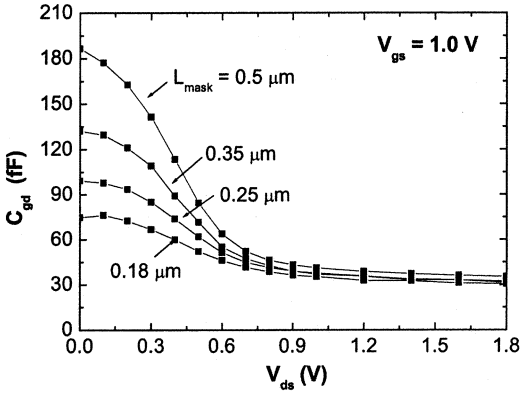

Fig. 4. Measured gate-channel capacitance, $C_{\rm gd}$, at $V_{\rm gs} = 1.0$ V for various channel lengths as a function of drain bias.

With determined $Q_{\rm inv}(V_{\rm GS} = V_{\rm gs}, V_{\rm DS} = V_{\rm ds} = 0)$, we increased $V_{\rm ds}$ with a fixed $V_{\rm gs}$. Note that both the intrinsic voltage $V_{\rm GS}$ and $V_{\rm DS}$ change when only $V_{\rm ds}$ changes with a constant $V_{\rm gs}$. Therefore, the corresponding increments of intrinsic voltages are given by, respectively

$$\begin{aligned}\Delta V_{\rm GS} &= -R_{sc}\Delta I_d, \\ \Delta V_{\rm DS} &= \Delta V_{\rm ds} - (R_{dc} + R_{sc})\Delta I_d \end{aligned} \tag{20}$$

where $\Delta V_{\rm gs} = 0$ because $V_{\rm gs}$ is kept to be constant. Therefore, the inversion charge can be obtained as follows:

$$\begin{aligned}|Q_{\rm inv}(V_{\rm GS}, V_{\rm DS})| &= |Q_{\rm inv}(V_{\rm GS}, 0)| \\ &\quad - \int_0^{V_{\rm ds}} (C_{gd,int} + C_{bd,int})dV_{\rm ds}^* \\ &\quad + \int_0^{V_{\rm ds}} \Big((C_{gd,int} + C_{bd,int}) \\ &\qquad \times \left(\frac{R_{dc}}{R_{sc}} + 1\right) \\ &\qquad -(C_{dg,int} + C_{sg,int})\Big) \\ &\quad \times R_{sc}\frac{\partial I_d}{\partial V_{\rm ds}^*}dV_{\rm ds}^* \\ &\approx |Q_{\rm inv}(V_{\rm GS}, 0)| \\ &\quad - \int_0^{V_{\rm ds}} \alpha C_{gd,int}dV_{\rm ds}^* \end{aligned} \tag{21}$$

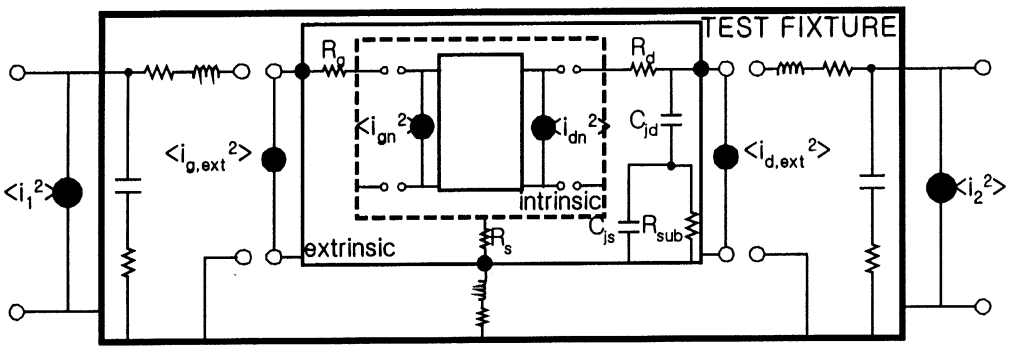

Fig. 5. Equivalent circuit for calculation of intrinsic drain thermal noise, $\langle i_{dn}^2 \rangle$, from measured output noise, $\langle i_2^2 \rangle$. Noise deembedding means the sequential process to find the wanted noise value from measured noise data. Firstly, the noise information of extrinsic part was determined from that of test fixture by eliminating the effects of probing pad. And intrinsic noises were further obtained from that of the extrinsic by eliminating the effects of parasitic in the extrinsic.

where $\alpha = 1 + C_{bd,int}/C_{gd,int} \approx 1 + g_{mb}/g_m$ [20]. The value of α was extracted from the ratio of g_{mb} to g_m. The third term in (21) was neglected because the net capacitance is small and the weighting factor, $R_{sc}(\partial I_d \partial V_{\rm ds})$, is much less than 1. From (21), total inversion charge is obtained by integrating the intrinsic capacitances with extrinsic drain bias when $V_{\rm ds}$ changes with a constant $V_{\rm gs}$. Fig. 4 shows the measured $C_{\rm gd}$ as a function of $V_{\rm ds}$ with various channel lengths. The parasitic capacitance, C_p, was assumed to be reciprocal, namely to be function of $V_{\rm G} - V_D$. Since the work function difference between $n+$ poly gate and n-LDD region is small, the flat band voltage is about 0 V. Therefore, C_p was assumed to be constant for $V_{\rm GD} > 0$ V because LDD region is accumulated, and C_p was assumed to be bias dependent for $V_{\rm GD} < 0$ V because LDD region is depleted. The bias dependent C_p was extracted from negatively gate biased region in Fig. 2. After subtracting C_p from measured $C_{\rm gd}$, we obtained total inversion charge by using (21), which was very accurately modeled as a function of bias.

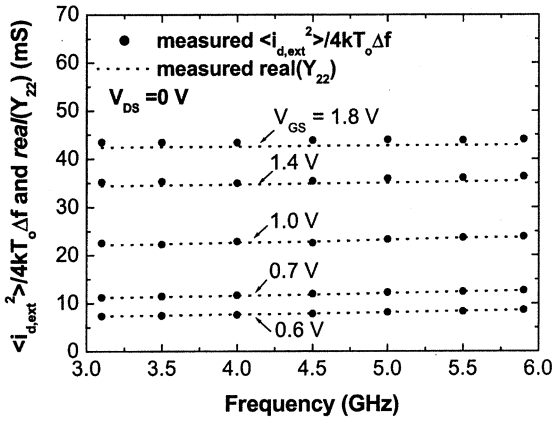

Fig. 6. $\langle i_{\rm d,ext}^2 \rangle / 4kT_o\Delta f$ and $real(Y_{22})$, versus frequency with larger $V_{\rm GS}$ than V_{TH} at $V_{\rm DS} = 0$ V. The ratio of $\langle i_{\rm d,ext}^2 \rangle / 4kT_o\Delta f$ to $real(Y_{22})$ is nearly equal to 1, which verifies the Nyquist theorem and shows the measurement accuracy.

IV. Noise Measurement and Model Verification

A. Noise Measurement Accuracy and Deembedding for Extraction of Channel Noise

Noise parameters and scattering parameters were measured by ATN noise and Agilent S-parameter measurement setup in the frequency range from 3 to 6 GHz. Noise correlation matrix [24] of admittance representation was constructed from the measured noise parameters ($NF_{\rm min}$, R_n, and Γ_{opt}) and the network parameters (S-parameter) to calculate $\langle i_1^2 \rangle$ and $\langle i_2^2 \rangle$ as indicated in Fig. 5. Additional OPEN and SHORT test structures were measured and the noise correlation matrix was constructed to deembed the parasitic components related to probing pad and interconnection lead, which interconnects with DUT in parallel and in series, respectively. To check the noise measurement accuracy, we first measured extrinsic drain noise current for various $V_{\rm GS} > V_{TH}$ at $V_{\rm DS} = 0$ V, which should be equal to $4kT_o\Delta f \cdot real(Y_{22})$ from thermodynamic theory, where Y_{22} was independently measured using S-parameter setup. The bias point of $V_{\rm DS} = 0$ V was selected to check the measurement accuracy because the theoretical value of the noise is known by Nyquist theorem. In Fig. 6, the symbol and the line represent the measured $\langle i_{d,ext}^2 \rangle / 4kT_o\Delta f$ and measured $real(Y_{22})$, respectively. It was confirmed that $\langle i_{d,ext}^2 \rangle / 4kT_o\Delta f$ and $real(Y_{22})$ are nearly equal to each other over whole frequencies and various gate bias ranges, which not only verifies the Nyquist theorem but also demonstrates the accuracy of our noise measurements.

To extract intrinsic drain thermal noise ($\langle i_{dn}^2 \rangle$) accurately, the noise deembedding was carried out further from extrinsic to intrinsic device. The source/drain resistance extracted in Section III was used. The gate electrode resistance (R_g), substrate resistance (R_{sub}), and drain junction capacitance (C_{jd}) were extracted from measured Y-parameters at $V_{\rm GS} = 0$ V [25]. The source junction capacitance (C_{js}) was set to the value of C_{jd} when $V_{\rm DS} = 0$ V because the source and drain are symmetrical at $V_{\rm DS} = 0$ V. Note that the substrate network (Y_{sub}) which consists of source/drain junction capacitance and a substrate resistance, is in parallel and the parasitic resistances which consist of source/drain and gate resistance are in series with the intrinsic device as shown in Fig. 5. The corresponding noise correlation matrices were constructed in admittance and impedance form, respectively. The sequential noise matrix operation, which subtracts the effect of silicon substrate at first in admittance form and then the effect of the parasitic resistances in impedance form, was carried out to obtain the intrinsic drain thermal noise. Finally we obtained the admittance represented noise correlation matrix for intrinsic device, where the intrinsic drain noise was determined. Note that the effect of induced gate noise is automatically eliminated in the extraction of intrinsic drain noise.

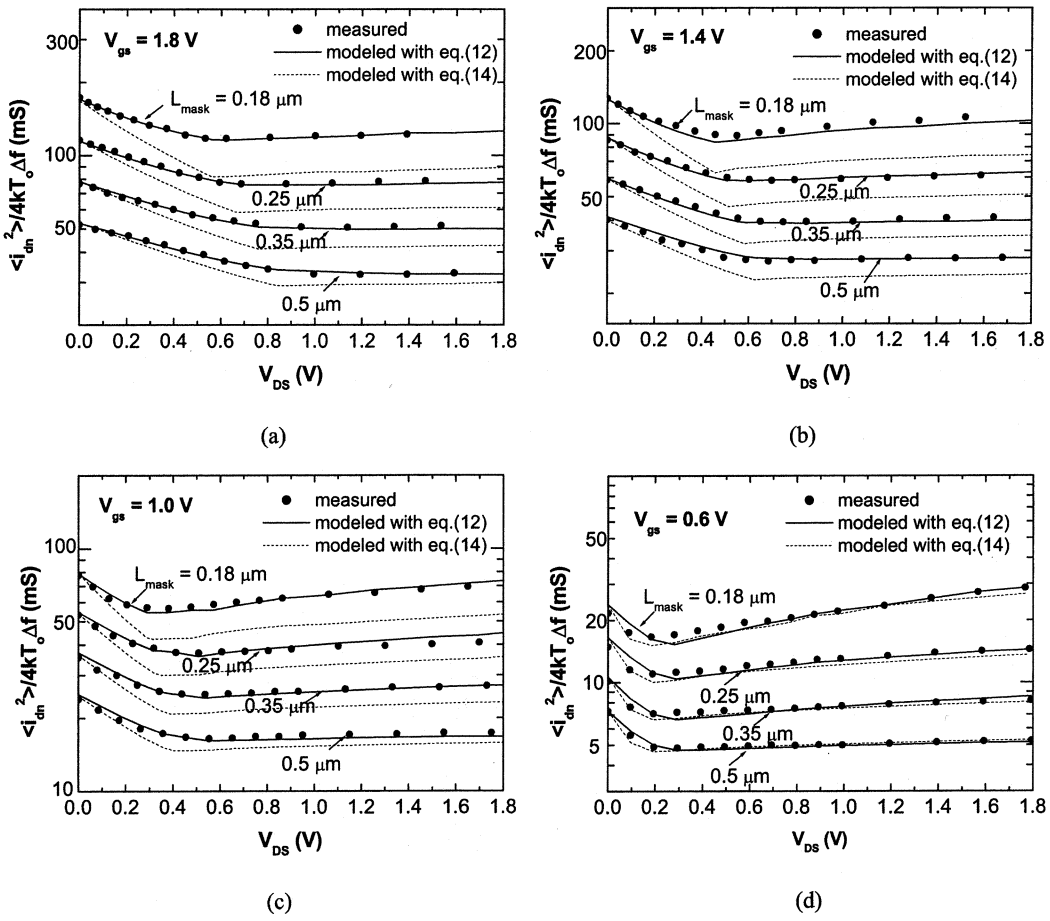

Fig. 7. Extracted (symbol) and modeled (lines) drain thermal noise versus $V_{\rm DS}$ at the various gate voltages (a) $V_{\rm gs} = 1.8$ V. (b) $V_{\rm gs} = 1.4$ V. (c) $V_{\rm gs} = 1.0$ V. (d) $V_{\rm gs} = 0.6$ V. The solid and dashed line represent the modeled drain thermal noise by using (12) and (14), respectively. The figure shows that the carrier heating effect should be taken into account, which becomes prominent as the channel length scales down. Excellent agreement in the linear regime indicates that the noise behaviors for short-channel MOSFET are explained very well with the model. The CLM effect becomes prominent with (d) small $L_{\rm eff}$, low $V_{\rm GS}$, and large $V_{\rm DS}$.

We found the extracted drain thermal noise is always white for various channel lengths and biases, indicating that $1/f$ noise is negligible in the measured frequency range of 3 GHz–6 GHz.

B. Thermal Noise Modeling With Total Inversion Charge

Fig. 7 compares the measured $\langle i_{dn}^2 \rangle$ with (12) and (14) from the linear regime to the saturation regime with various gate voltages. The symbol, the solid, and the dashed line represent the extracted intrinsic drain thermal noise, the modeled value using (12), and the modeled value using (14), respectively. The model given by (12) is plotted using (17) and measured inversion charge in Section III. And the model given by (14) is plotted using (A.2) as a function of intrinsic biases. Since the channel conductance decreases with increasing drain voltage, the drain thermal noise decreases steadily until $V_{\rm DS} = V_{DSsat}$, where V_{DSsat} is the drain saturation voltage. The model given by (17) excellently explains the drain bias dependency and channel length dependency of thermal noise for all gate biases and channel lengths. Note the excellent agreement between the measured and the modeled values at $V_{\rm DS} = 0$ V, which shows the accuracy of noise measurement and the validity of extracted parameters. The model, which assumes thermal equilibrium condition in the gradual channel region, predicts maximally about 30% less noise than measured thermal noise for the device with $L_{\rm mask} = 0.18$ μm as shown in Fig. 7, which indicates that thermal heating effect should be taken into account. The heating effect becomes more prominent with the smaller gate length and the higher gate bias because the electric field in gradual channel region becomes larger. But, abnormal large excess noise was not observed in the linear regime in contrary to the previous results [6], [7], which addressed that the large excess noise was observed in the linear regime. Excellent agreements with (17) in the linear regime indicate that the heating effect expressed by (10) is very accurate and the model properly takes into account the noise behavior for short-channel MOSFETs. Note that the velocity saturation effect makes V_{DSsat} smaller as the channel length scales down as shown in Fig. 7(a). Saturation velocity ν_{sat} of 1.15×10^7 cm/s was used to model *I–V* characteristics, which is reasonable value [26]. For the drain voltage larger than V_{DSsat}, the moderate increase of drain thermal noise was observed. And the increase becomes large as the channel length is scaled down and $V_{\rm GS}$ approaches to V_{TH} as shown in Fig. 7(d). We believe that such moderate increase of thermal noise is related to the channel length modulation effect, which was first pointed out in [12] and rigorously argued by Deen *et al.* in [27]. The ΔL can

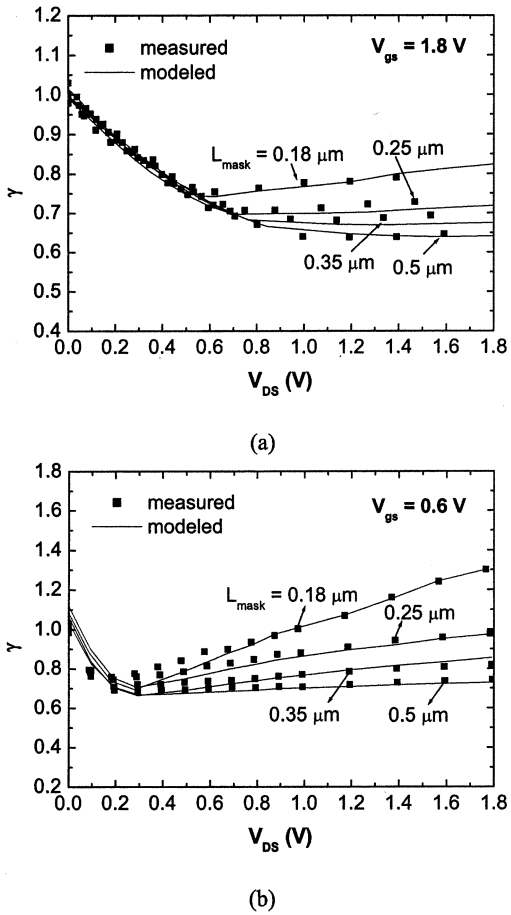

Fig. 8. Extracted (symbol) and modeled (dash line) value γ versus $V_{\rm DS}$ at the constant gate voltage of 1.8 V (a) and 0.6 V (b), respectively. In the linear regime, γ was nearly independent of channel lengths. At high gate bias, $V_{DS,sat}$ becomes small due to velocity saturation effect, which causes the increase of the drain thermal noise. In saturation regime, γ increased moderately at low gate voltage with drain bias, which is attributed to channel length modulation effect.

be calculated with pseudo two-dimensional analysis [26] as follows:

$$\Delta L = \lambda \ln \left[\frac{V_{\rm DS} - V_{DSsat}}{V_\lambda} + \sqrt{\left(\frac{V_{\rm DS} - V_{DSsat}}{V_\lambda} \right)^2 + 1} \right] \tag{22}$$

where $V_\lambda = \lambda E_C$ and λ is characteristic length which is a fitting parameter. We have modeled *I–V* characteristics excellently with help of (22) in the saturation regime. Equation (22) suggests that ΔL is independent of channel length and only a function of applied biases. Therefore, we extracted ΔL with independent IV measurement for the device with channel length of 0.5 μm. The DIBL characteristics of the device was so small that the device was selected to obtain ΔL. The extracted ΔL from IV for device with $L_{\rm mask} = 0.5$ μm was used to model the thermal noise for all channel lengths. When the channel length modulation effect was considered, excellent agreements between the measured and the modeled thermal noise were achieved at saturation regime as shown in Fig. 7.

The drain thermal noise, $\langle i_{dn}^2 \rangle$, is often expressed as [17]

$$\langle i_{dn}^2 \rangle = 4kT_o \Delta f \cdot \gamma \cdot G_{\rm do}. \tag{23}$$

For long-channel MOSFETs, γ satisfies the inequality $2/3 \leq \gamma \leq 1$. The value of 2/3 holds when the MOSFET is in the saturation regime and the value of one holds when the drain bias is zero. Fig. 8 shows the measured and modeled γ as a function of $V_{\rm DS}$ with different gate voltages at $V_{\rm gs} = 1.8$ V (a) and $V_{\rm gs} = 0.6$ V (b). Note that $G_{\rm do}$ changes as $V_{\rm gs}$ is constant and $V_{\rm ds}$ increases because the intrinsic $V_{\rm GS}$ changes. Therefore, the corresponding $G_{\rm do}$ to $V_{\rm GS}$ was used to calculate γ. In the linear regime, γ values were almost the same for different channel lengths because the change of inversion charge with drain bias has the same bias dependency independent of the channel lengths as shown in (16). Due to velocity saturation effect, $V_{\rm DSsat}$ was smaller as channel length scales down at high gate voltages, which results in the slight increase of thermal noise compared to that of long channel as shown in Fig. 8(a). And γ values were dependent on the channel length in the saturation regime. γ values increased steadily with the drain bias in saturation regime, which is attributed to the channel length modulation effect. Such increase of γ with the drain bias became more critical for devices with smaller channel lengths [(Fig. 8(b)], because the channel length modulation has larger effects for the short-channel devices.

V. Conclusion

In this paper, the physics-based drain thermal noise current model of MOSFET, which takes into account velocity saturation effect and carrier heating effect, was derived and verified by accurately measured drain thermal noise and total inversion charge for short-channel MOSFETs. The accuracies of noise measurement were confirmed by measuring the noise at $V_{\rm DS} = 0$ V. For the noise modeling, we obtained the total inversion charge by measuring and integrating capacitances extracted from S-parameters. The modeling results of the thermal noise have shown that the carrier heating effect in gradual channel region becomes important at high gate biases and the channel length modulation effect is important at low gate biases. The dependencies of the thermal noise on channel length, drain biases, and gate biases were explained excellently with the model.

Appendix

In this appendix, we evaluate (12) and (14) as a function of applied biases in detail. For convenience, the useful notations used in the Section II are explained again, here. $V_L (= L_{\rm elec} E_C)$ is a limit of saturation voltage due to the velocity saturation, $z (= V_{\rm DS}/V_L)$ is a normalized drain voltage, and $u (= \alpha V_{\rm DS}/V_{\rm GT})$ is a ratio of drain bias to saturation voltage due to pinch-off. From (12), the drain thermal noise can be separated into two terms

$$\begin{aligned} \langle i_{dn}^2 \rangle &= \langle i_{dn,equ}^2 \rangle + \langle i_{dn,heat}^2 \rangle \\ &= \frac{4kT_o \Delta f}{I_d L_{\rm elec}^2 \left(1 + \frac{V_{\rm DS}}{V_L}\right)^2} \int_{regionI} g_o^2(V) dV \\ &\quad + \frac{4kT_o \Delta f}{I_d L_{\rm elec}^2 \left(1 + \frac{V_{\rm DS}}{V_L}\right)^2} \int_{regionI} g_o^2(V) \left(\frac{E}{E_C}\right) dV. \end{aligned} \tag{A.1}$$

The first term, $\langle i^2_{dn,equ}\rangle$, corresponds to the thermal noise when the channel is under thermal equilibrium condition, which was given by (14). And the second, $\langle i^2_{dn,heat}\rangle$, corresponds to the noise added by the heating effect expressed with (10). It is straightforward to evaluate $\langle i^2_{dn,equ}\rangle$ as a function of applied biases

$$\langle i^2_{dn,equ}\rangle = 4kT_o\Delta f \cdot G_{\rm do} \cdot \frac{1-u+\frac{u^2}{3}}{1-\frac{u}{2}} \cdot \frac{1}{1+z}. \qquad \text{(A.2)}$$

$\langle i^2_{dn,heat}\rangle$ is evaluated as a function of applied biases

$$\begin{aligned}\langle i^2_{dn,heat}\rangle &= \frac{4kT_o\Delta f}{I_d L^2_{\rm elec}\left(1+\frac{V_{\rm DS}}{V_L}\right)^2} \\ &\quad\times \int_{regionI} g_o^2\Big(V\Big)\Big(\frac{E}{E_C}\Big)dV \\ &= \frac{4kT_o\Delta f \cdot I_d}{L^2_{\rm elec}\left(1+\frac{V_{\rm DS}}{V_L}\right)^2 E_C} \\ &\quad\times \int_{regionI}(1+2\frac{E}{E_C}+\left(\frac{E}{E_C}\right)^2)dx \\ &\approx 4kT_o\Delta f \cdot G_{\rm do}\frac{z}{(1+z)}\left(1-\frac{u}{2}\right). \qquad \text{(A.3)}\end{aligned}$$

It is also straightforward to evaluate the first and second integral of (A.3). However, the third integral of (A.3) could be evaluated with applied biases analytically with the information of electric field E as a function of x. And the analytical equation was expanded with the talyor series about z. Note that the last equation of (A.3) can be obtained directly if we use the approximation, $E = V_{\rm DS}/L_{\rm elec}$, which shows that the approximation is very accurate.

Adding (A.2) and (A.3) leads to

$$\begin{aligned}\langle i^2_{dn}\rangle &\approx 4kT_o\Delta f \\ &\quad\cdot G_{\rm do}\cdot\left(\frac{1-u+\frac{u^2}{3}}{1-\frac{u}{2}} - \frac{z}{(1+z)(1-\frac{u}{2})}\left(\frac{u^2}{12}\right)\right) \\ &\approx 4kT_o\Delta f \cdot G_{\rm do}\cdot\left(\frac{1-u+\frac{u^2}{3}}{1-\frac{u}{2}}\right). \qquad \text{(A.4)}\end{aligned}$$

The total inversion charge can be simply evaluated as a function of applied bias

$$\begin{aligned}Q_{\rm inv} &= \left(\frac{L^2_{\rm elec}}{\mu_{\rm eff}}\right)G_{\rm do}\left(\frac{1-u+\frac{u^2}{3}}{1-\frac{u}{2}} + \frac{1}{12}\frac{z}{1-\frac{u}{2}}u^2\right) \\ &\approx \left(\frac{L^2_{\rm elec}}{\mu_{\rm eff}}\right)G_{\rm do}\left(\frac{1-u+\frac{u^2}{3}}{1-\frac{u}{2}}\right). \qquad \text{(A.5)}\end{aligned}$$

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