Methodology of Parameter and Coupling Ratio Extraction for Source Side Injection (SSI) Flash Cell

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Abstract

We present a new methodology to generate a two-transistor MACRO model of a SSI Flash cell based on a practical cell partitioning and a systematic and rigorous parameter extraction scheme. Through judicious use of TCAD simulation and precise measurement techniques, BSIM3 parameters of the individual transistors and coupling ratios of the cell were extracted, yielding a SPICE-compatible MACRO model for a three-poly split-gate Flash cell.

1. Introduction

Source Side Injection (SSI) Flash cell has drawn much attention during the past few years for its high injection efficiency and low programming current, as a leading candidate for low-voltage operation or multi-bit storage technology [1, 2]. To optimize the cell operation and to facilitate the array control circuit design, better understanding of the cell behavior and accurate prediction of the I-V characteristics of the cell are necessary. Though series-connected 2 transistors with an appropriately coupled floating gate is the most feasible description for the SSI cell, there has been no general procedure of parameter extraction since the 2 transistors configuration makes it extremely difficult to extract physical and accurate parameters of the transistors independently. In this paper, we present a general methodology to create a MACRO model for a split-gate Flash cell using a two-transistor representation. Through extensive TCAD simulation and precise measurement techniques, BSIM3 parameters of the individual transistors and coupling ratios (CR's) of the cell were extracted, yielding a SPICE-compatible MACRO model for a three-poly split-gate Flash cell [3].

2. MACRO Cell Representation of SSI Cell

Fig. 1 (a) shows a cross-sectional view of our three-poly split-gate Flash cell and its operating parameters are shown in Table 1. TEM photography in Fig. 2 shows actual dimension of the cell including the size of the gap between select gate (SG) and floating gate (FG). The cell is approximated by a representation of two transistors and five coupling capacitors[1)] as shown in Fig. 1 (b). Device simulation shows that this 2-transistor representation is reliable under most operating

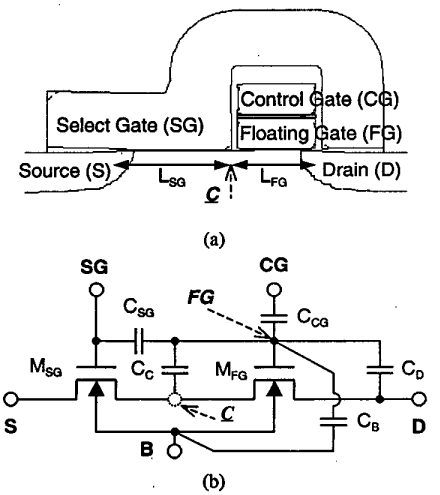

Fig. 1: Cross-sectional schematic of SSI Flash cell (a) and Equivalent circuit of MACRO cell (b). C represents a virtual node between the two transistors. The FG node is connected to 5 capacitors. L_{SG}=0.5μm, L_{FG}=0.4μm.

[1)] We note the "gap" transistor is not included and the capacitors are assumed to be bias-independent to yield fixed coupling ratios.

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	V_{SG}	V_{CG}	V_S	V_D	V_B
Write	1.0	10	0	5	0
Erase	0	-10	Open	5	0
Read	3.3	1.2	1.2	0	0

Table. 1: Operating conditions of 3-poly split-gate Flash cell. Values shown are in units of [V].

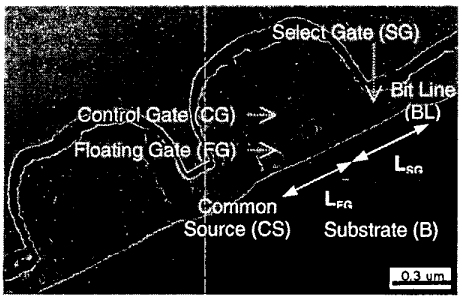


Fig. 2: Cross-sectional TEM photography of 3-poly split-gate Flash cell

conditions except when both transistors are in deep saturation. Here current flows penetrate deep into the bulk between SG (select gate) and FG (floating gate), and the node $\mathcal{C}$ between the two transistors does not have a well-defined position and hence is a virtual node. Further, interaction between M_{FG} and M_{SG} transistors can occur. For instance, the drain voltage of M_{FG}, which is applied to a deep junction, can substantially affect V_{th} of M_{SG}. Thus, the effect of the drain voltage of M_{FG} on the current of M_{SG} should be considered [4]. We have studied this effect and found it to be small for this specific cell and hence it was not modeled here.

3. Parameter and Coupling Ratio Extraction

For developing a reliable MACRO model, accurate and systematic parameter extraction for all these elements is critical. But the series-connected transistor configuration makes it difficult to extract parameters of one transistor independently of the other. Moreover, for each transistor, one of the junctions is physically absent. As shown in Fig. 3 (a), under the stated biasing condition, the drain of M_{SG} can be considered as an induced junction extended from the inversion layer of M_{FG}. Consequently the DIBL effect of M_{SG} is expected to be

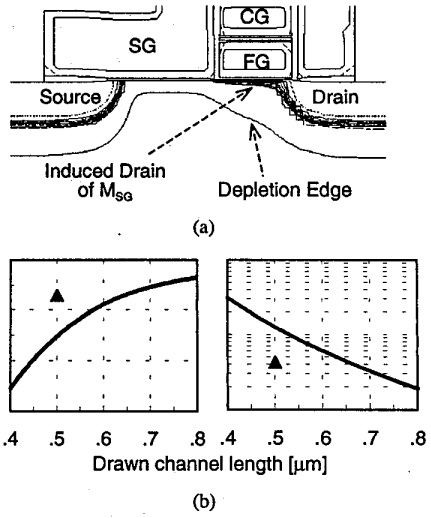


Fig. 3: (a) Simulated electron density contours with high V_{FG}. This bias condition is used to investigate M_{SG} without series resistance effect from M_{FG}. (b) Measured body effect (left) and DIBL (right) of M_{SG}. Component transistor of the split-gate cell (▲) shows much different characteristics from stand-alone transistor (line).

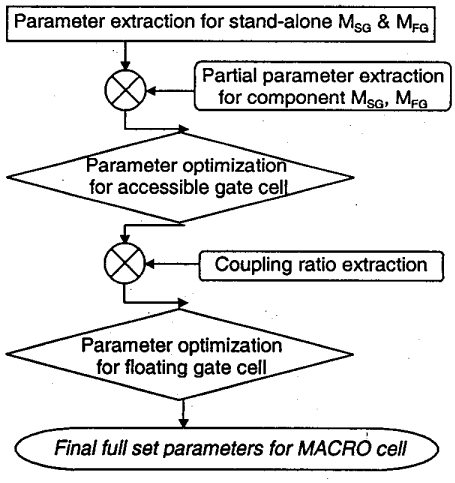
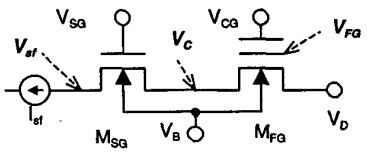


Fig. 4: Flow diagram for parameter extraction.



(a)

	α_{SG}	α_{CG}	α_C	α_D	α_B
CR	0.12	0.56	0.14	0.15	0.03

(b)

Fig. 5: Measurement set-up where $V_{sf} \cong V_C = (V_{FG} - V_{th}$ of $M_{FG})$ and extracted coupling ratio (CR) values under "Read" operation condition.

smaller than that of its stand-alone counterparts while the body effect is larger. Measurements results shown in Fig. 3 (b) confirm these projections[2]. The parameter extraction procedure is given schematically in Fig. 4. Here a divide-and-conquer strategy is deployed. First we extracted a full set of BSIM3 parameters for M_{SG} and M_{FG} via their respective groups of stand-alone transistors. Then using the accessible gate cell[3], some key parameters of each component-transistor MSG and MFG are extracted without any significant effect from the other transistor. Using a device simulator, in which we can arbitrarily exclude the effect of the series-connected transistors, we found that the following device parameters--effective channel length, body effect, DIBL, and channel length modulation--of the component-transistor are mostly different from those of a stand-alone transistor. Then the 2 sets of parameters are combined to yield an optimized parameter set to fit the split-gate transistors I-V characteristics using a commercial parameter optimizer, UTMOST [5].

To extract CR's, a method based on source follower voltage (V_{sf}) measurement as illustrated in Fig. 5 was used [6]. V_{sf} has a unique relationship with the floating gate potential (V_{FG}), which can be accurately measured using an accessible gate reference cell. The change in V_{FG}, which results in change in V_{sf}, is given by,

$$\Delta V_{FG} = \sum \alpha_i \Delta V_i + (\Delta Q_{FG} / C_{total}) \qquad (1)$$

[2] This entails the modeling parameters of each component-transistor will be dependent on the direction of the current flow.

[3] In accessible gate cell, FG and CG are tied together.

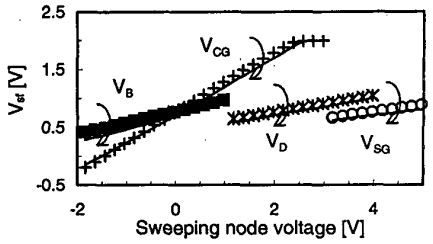


Fig. 6: V_{sf} as functions of sweeping voltages is well matched between measurements (symbols) and simulation (line).

where coupling ratio α_i is defined as C_i/C_{total} for each coupling node with voltage V_i and capacitance C_i. Measuring V_{sf} by ramping each of V_{SG}, V_{CG}, V_D, and V_B

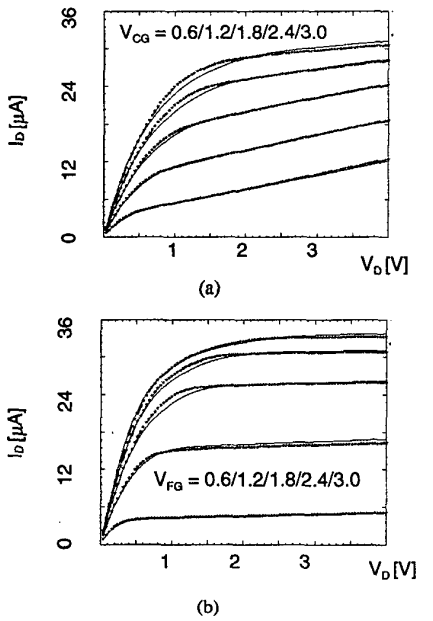


Fig. 7: Comparison of I-V characteristics between measurement (solid line) and SPICE simulation (dotted line) for accessible gate cell (b) and for floating gate cell (a) at $V_S = V_B = 0$, $V_{SG} = 1.2$[V].

sequentially, we obtain 4 equations containing 5 unknown coupling ratios α_i's. With the equation, $\sum \alpha_i = 1$, being the fifth equation, all 5 α_i's can be computed. After a final tuning of BSIM3 parameters and CR's with measured I-V data for the floating gate cell, a final full parameter set is attained.

4. Results and Conclusion

Using the optimized BSIM3 parameters and the extracted coupling ratios, our MACRO cell model was implemented in SPICE under a variety of conditions. Figs. 6 and 7 show excellent agreement between SPICE simulation and measurement results, for the coupling of floating node by other nodes and I-V characteristics of access gate and floating gate cell. In summary, we presented a SPICE-compatible MACRO model of a SSI Flash cell based on a methodology of practical cell partitioning and a systematic and rigorous parameter extraction scheme, augmented and guided by extensive TCAD simulation.

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