Low-voltage high-performance silicon photonic devices and photonic integrated circuits operating up to 30 Gb/s

Gyungock Kim,[1,*] Jeong Woo Park,[1] In Gyoo Kim,[1] Sanghoon Kim,[1] Sanggi Kim,[1] Jong Moo Lee,[1] Gun Sik Park,[1] Jiho Joo,[1] Ki-Seok Jang,[1] Jin Hyuk Oh,[1] Sun Ae Kim,[1] Jong Hoon Kim,[1] Jun Young Lee,[1] Jong Moon Park,[1] Do-Won Kim,[1] Deog-Kyoon Jeong,[2] Moon-Sang Hwang,[2] Jeong-Kyoum Kim,[2] Kyu-Sang Park,[2] Han-Kyu Chi,[2] Hyun-Chang Kim,[2] Dong-Wook Kim,[2] and Mu Hee Cho[3]

[1]*Electronics & Telecommunications Research Institute, 138 Gajeongno, Yuseong-gu, Daejeon, 305-700, Korea*
[2]*Seoul National University, 1 Gwanak-ro, Gwanak-gu, Seoul, 151-742, Korea*
[3]*Korea Advanced Institute of Science & Technology, 291 Daehak-ro, Yuseong-gu, Daejeon, 305-701, Korea*
[*]*gokim@etri.re.kr*

Abstract: We present high performance silicon photonic circuits (PICs) defined for *off-chip* or *on-chip* photonic interconnects, where *PN* depletion Mach-Zehnder modulators and evanescent-coupled waveguide Ge-on-Si photodetectors were monolithically integrated on an SOI wafer with CMOS-compatible process. The fabricated silicon $PIC_{off\text{-}chip}$ for *off-chip* optical interconnects showed operation up to 30 Gb/s. Under differential drive of low-voltage 1.2 V_{pp}, the integrated 1 *mm*-phase-shifter modulator in the $PIC_{off\text{-}chip}$ demonstrated an extinction ratio (ER) of 10.5dB for 12.5 Gb/s, an ER of 9.1dB for 20 Gb/s, and an ER of 7.2 dB for 30 Gb/s operation, without adoption of travelling-wave electrodes. The device showed the modulation efficiency of $V_\pi L_\pi$ ~1.59 Vcm, and the phase-shifter loss of 3.2 dB/mm for maximum optical transmission. The Ge photodetector, which allows simpler integration process based on reduced pressure chemical vapor deposition exhibited operation over 30 Gb/s with a low dark current of 700 nA at −1V. The fabricated silicon $PIC_{intra\text{-}chip}$ for *on-chip* (*intra-chip*) photonic interconnects, where the monolithically integrated modulator and Ge photodetector were connected by a silicon waveguide on the same chip, showed o*n-chip* data transmissions up to 20 Gb/s, indicating potential application in future silicon *on-chip* optical network. We also report the performance of the hybrid silicon electronic-photonic IC (*EPIC*), where a $PIC_{intra\text{-}chip}$ chip and 0.13μm CMOS interface IC chips were hybrid-integrated.

OCIS codes: (250.5300) Photonic integrated circuit; (130.3120) Integrated optics devices; (200.4650) Optical interconnects; (250.7360) Waveguide modulators; (130.0250) Optoelectronics; (130.4110) Electro-optical devices; (040.6040) silicon detectors; (040.5160) Photodetectors; (060.4510) Optical communications.

References and links

1. M. Haurylau, G. Chen, H. Chen, J. Zhang, N. A. Nelson, D. H. Albonesi, E. G. Friedman, and P. M. Fauchet, "On-chip optical interconnect roadmap: challenges and critical directions," IEEE J. Sel. Top. Quantum Electron. **12**(6), 1699–1705 (2006).
2. C. Gunn, "CMOS photonics for high-speed interconnects," IEEE. Micro. **26**(2), 58–66 (2006).
3. A. Shacham, K. Bergman, and L. P. Carloni, "Photonic networks-on-chip for future generations of chip multiprocessors," IEEE Trans. Comput. **57**(9), 1246–1260 (2008).
4. D. Miller, "Device requirements for optical interconnects to silicon chips," Proc. IEEE **97**(7), 1166–1185 (2009).
5. K. Preston, L. Chen, S. Manipatruni, and M. Lipson, "Silicon photonic interconnect with micrometer-scale devices," *6th International Conference on Group IV Photonics*, WA2, 1–3 (2009).
6. A. Narasimha, S. Abdaila, C. Bradbury, A. Clark, J. Clymore, J. Coyne, A. Dahl, S. Gloeckner, A. Gruenberg, D. Guckenberger, S. Gutierrez, M. Harrison, D. Kucharski, K. Leap, R. LeBlanc, V. Liang, M. Mack, D. Martinez,

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G. Masini, A. Mekis, R. Menigoz, C. Ogden, M. Peterson, T. Pinguet, J. Redman, J. Rodriguez, S. Sahni, M. Sharp, T. Sleboda, D. Song, V. Wang, B. Welch, J. Witzens, W. Xu, K. Vokoyama, and P. DobbeIaere, "An ultra low power CMOS photonics technology platform for H/S optoelectronic transceivers at less than $1 per Gbps," in *Proc. OFC 2010*, San Diego, USA (2010).
7. R. Soref and B. Bennett, "Electrooptical effects in silicon," IEEE J. Quantum Electron. **23**(1), 123–129 (1987).
8. L. Liao, A. Liu, D. Rubin, J. Basak, Y. Chetrit, H. Nguyen, R. Cohen, N. Izhaky, M. Paniccia, N. Izhaky, and M. Paniccia, "40Gbit/s silicon optical modulator high-speed applications," Electron. Lett. **43**(22), 1196–1197 (2007).
9. A. Liu, L. Liao, D. Rubin, H. Nguyen, B. Ciftcioglu, Y. Chetrit, N. Izhaky, and M. Paniccia, "High-speed optical modulation based on carrier depletion in a silicon waveguide," Opt. Express **15**(2), 660–668 (2007).
10. W. M. Green, M. J. Rooks, L. Sekaric, and Y. A. Vlasov, "Ultra-compact, low RF power, 10 Gb/s silicon Mach-Zehnder modulator," Opt. Express **15**(25), 17106–17113 (2007).
11. J. W. Park, J.-B. You, I. G. Kim, and G. Kim, "High-modulation efficiency silicon Mach-Zehnder optical modulator based on carrier depletion in a PN Diode," Opt. Express **17**(18), 15520–15524 (2009).
12. J.-B. You, M. Park, J.-W. Park, and G. Kim, "12.5 Gbps optical modulation of silicon racetrack resonator based on carrier-depletion in asymmetric p-n diode," Opt. Express **16**(22), 18340–18344 (2008).
13. P. Dong, S. Liao, D. Feng, H. Liang, D. Zheng, R. Shafiiha, C.-C. Kung, W. Qian, G. Li, X. Zheng, A. V. Krishnamoorthy, and M. Asghari, "Low Vpp, ultralow-energy, compact, high-speed silicon electro-optic modulator," Opt. Express **17**(25), 22484–22490 (2009).
14. N. N. Feng, S. Liao, D. Feng, P. Dong, D. Zheng, H. Liang, R. Shafiiha, G. Li, J. E. Cunningham, A. V. Krishnamoorthy, and M. Asghari, "High speed carrier-depletion modulators with 1.4V-cm V(π)L integrated on 0.25microm silicon-on-insulator waveguides," Opt. Express **18**(8), 7994–7999 (2010).
15. F. Y. Gardes, D. J. Thomson, N. G. Emerson, and G. T. Reed, "40 Gb/s silicon photonics modulator for TE and TM polarizations," Opt. Express **19**(12), 11804–11814 (2011).
16. D. J. Thomson, F. Y. Gardes, Y. Hu, G. Mashanovich, M. Fournier, P. Grosse, J.-M. Fedeli, and G. T. Reed, "High contrast 40Gbit/s optical modulation in silicon," Opt. Express **19**(12), 11507–11516 (2011).
17. G. Rasigade, M. Ziebell, D. Marris-Morini, J.-M. Fédéli, F. Milesi, P. Grosse, D. Bouville, E. Cassan, and L. Vivien, "High extinction ratio 10 Gbit/s silicon optical modulator," Opt. Express **19**(7), 5827–5832 (2011).
18. M. Watts, W. Zortman, D. Trotter, R. Young, and A. Lentine, "Low-voltage, compact, depletion-mode, silicon Mach–Zehnder modulator," IEEE J. Sel. Top. Quantum Electron. **16**(1), 159–164 (2010).
19. D. Ahn, C. Y. Hong, J. Liu, W. Giziewicz, M. Beals, L. C. Kimerling, J. Michel, J. Chen, and F. X. Kärtner, "High performance, waveguide integrated Ge photodetectors," Opt. Express **15**(7), 3916–3921 (2007).
20. L. Vivien, J. Osmond, J. M. Fédéli, D. Marris-Morini, P. Crozat, J. F. Damlencourt, E. Cassan, Y. Lecunff, and S. Laval, "42 GHz p.i.n Germanium photodetector integrated in a silicon-on-insulator waveguide," Opt. Express **17**(8), 6252–6257 (2009).
21. D. Feng, S. Liao, P. Dong, N. Feng, H. Liang, D. Zheng, C. Kung, J. Fong, R. Shafiiha, J. Cunningham, A. V. Krishnamoorthy, and M. Asghari, "High-speed Ge photodetector monolithically integrated with large cross-section silicon-on-insulator waveguide," Appl. Phys. Lett. **95**(26), 261105 (2009).
22. H. Yu S. Ren, W. Jung, A. Okyay, D. Miller, and K. Saraswat, "High-efficiency p-i-n photodetectors on selective-area-grown Ge for monolithic integration," IEEE Electron Device Lett. **30**(11), 1161–1163 (2009).
23. S. Assefa, F. Xia, and Y. A. Vlasov, "Reinventing germanium avalanche photodetector for nanophotonic on-chip optical interconnects," Nature **464**(7285), 80–84 (2010).
24. S. Liao, N. N. Feng, D. Feng, P. Dong, R. Shafiiha, C. C. Kung, H. Liang, W. Qian, Y. Liu, J. Fong, J. E. Cunningham, Y. Luo, and M. Asghari, "36 GHz submicron silicon waveguide germanium photodetector," Opt. Express **19**(11), 10967–10972 (2011).
25. M. Morse, O. Dosunmu, T. Yin, Y. Kang, H. D. Liu, G. Sarid, E. Ginsburg, R. Cohen, S. Litski, and M. Zadka, "Performance of Ge/Si receivers at 1310 nm," Physica E **41**(6), 1076–1081 (2009).
26. Y. Kang, H.-D. Liu, M. Morse, M. J. Paniccia, M. Zadka, S. Litski, G. Sarid, A. Pauchard, Y.-H. Kuo, H.-W. Chen, W. S. Zaoui, J. E. Bowers, A. Beling, D. C. McIntosh, X. Zheng, and J. C. Campbell, "Monolithic germanium/silicon avalanche photodiodes with 340 GHz gain–bandwidth product," Nature Photon. **3**, 59–63 (2009).
27. M. Jutzi, M. Berroth, G. Wöhl, M. Oehme, and E. Kasper, "Ge-on-Si vertical incidence photodiodes with 39-GHz bandwidth," IEEE Photon. Technol. Lett. **17**(7), 1510–1512 (2005).
28. D. Suh, S. Kim, J. Joo, and G. Kim, "36-GHz high-responsivity Ge photodetectors grown by RPCVD," IEEE Photon. Technol. Lett. **21**(10), 672–674 (2009).
29. J. Joo, S. Kim, I. Kim, K. Jang, and G. Kim, "High- sensitivity 10 Gbps Ge-on- Si photoreceiver operating at $\lambda \sim$ 1.55 µm ," Opt. Express **18**, 16474–16479 (2010).
30. J. Joo, S. Kim, I. Kim, K. Jang, and G. Kim, "Progress in high-responsivity vertical-illumination type Ge-on-Si photodetecor operating at $\lambda \sim$1.55 µm," *in Proc. OFC 2011*, Los Angeles, USA (2011).
31. T. Pinguet, B. Analui, E. Balmater, D. Guckenberger, M. Harrison, R. Koumans, D. Kucharski, Y. Liang, G. Masini, A. Mekis, S. Mirsaidi, A. Narasimha, M. Peterson, D. Rines, V. Sadagopan, S. Sahni, T. J. Sleboda, D. Song, Y. Wang, B. Welch, J. Witzens, J. Yao, S. Abdalla, S. Gloeckner, P. De Dobbelaere, and G. Capellini, "Monolithically Integrated High-Speed CMOS Photonic Transceivers," in *Proc. IEEE Int. Conf. Group IV Photonics*, 362–364 (2008).
32. X. Zheng, F. Liu, D. Patil, H. Thacker, Y. Luo, T. Pinguet, A. Mekis, J. Yao, G. Li, J. Shi, K. Raj, J. Lexau, E. Alon, R. Ho, J. E. Cunningham, and A. V. Krishnamoorthy, "A sub-picojoule-per-bit CMOS photonic receiver for densely integrated systems," Opt. Express **18**(1), 204–211 (2010).

#156656 - $15.00 USD Received 19 Oct 2011; revised 30 Nov 2011; accepted 8 Dec 2011; published 16 Dec 2011

33. T. Y. Liow, K. W. Ang, Q. Fang, J. F. Song, Y. Z. Xiong, M. B. Yu, G. Q. Lo, and D. L. Kwong, "Silicon modulators and germanium photodetectors on SOI: Monolithic integration, compatibility, and performance optimization," IEEE Sel. Top. Quantum Electron. **16**(1), 307–315 (2010).
34. M. Rasras, D. Gill, M. Earnshaw, C. Doerr, J. Weiner, C. Bolle, and Y. Chen, "CMOS silicon receiver integrated with Ge detector and reconfigurable optical filter," IEEE Photon. Technol. Lett. **22**(2), 112–114 (2010).
35. X. Zheng, D. Patil, J. Lexau, F. Liu, G. Li, H. Thacker, Y. Luo, I. Shubin, J. Li, J. Yao, P. Dong, D. Feng, M. Asghari, T. Pinguet, A. Mekis, P. Amberg, M. Dayringer, J. Gainsley, H. F. Moghadam, E. Alon, K. Raj, R. Ho, J. E. Cunningham, and A. V. Krishnamoorthy, "Ultra-efficient 10 Gb/s hybrid integrated silicon photonic transmitter and receiver," Opt. Express **19**(6), 5172–5186 (2011).
36. K. Park, B. Yoo, M. Hwang, H. Chi, H. Kim, J. Park, G. Kim, and D. Jeong, "A 10-Gb/s optical receiver front-end with 5-mW transimpedance amplifier," *IEEE Asian Solid-State Circuits Conference*, Beijing, 3–5 (2010).

Advancement of silicon photonics technology can offer a new dimension in chip-level data communications by providing high-performance optical interconnects with un-precedent bandwidth based on the cost-effective silicon photonic/CMOS platform [1–5]. In recent years, silicon photonics has shown remarkable progress [6–35], and is starting to find its position in practical applications in telecommunications and data communications.

Increasing the integration level in silicon photonics is required to develop compact high-performance optical interconnects for future systems. There have been reports on silicon photonic integration at various levels [31–35]. Monolithic integration of multiple optical components on the same wafer to realize silicon photonic integrated circuits (PICs) can cost-effectively increase both functionality and performance. Continued performance improvement of silicon photonic devices and their integration levels based on CMOS fabrication technology is necessary for full utilization of silicon photonics in chip-level data communications and telecommunications.

Silicon optical modulators and Ge-on-Si photodetectors, which are the main active components in silicon optical transceiver circuits, have made remarkable progress [6–35]. The silicon optical modulator, a key device for transmitting optical data, is based on the free-carrier plasma dispersion effect, where the refractive index of a silicon waveguide can be modulated by either carrier injection in a PIN diode or carrier-depletion effect in a PN diode [6–18]. In the modulator for chip-level optical interconnects, it is important to achieve high modulation efficiency up to high data rates with low optical loss while minimizing size for high energy efficiency. Intensive work has been done in this area in recent years. Silicon Mach–Zehnder (MZ) modulators and resonator-type modulators based on a PN junction in reverse bias modes have shown potential for wideband high-speed performance due to their faster modulations utilizing fast carrier depletion effects. Using vertical and lateral PN junctions, depletion-mode modulators with various efficiencies in high speed operation from 10 Gb/s up to 40 Gb/s have been reported [7–11, 14–18]. Most of the reported silicon MZ modulators require relatively high driving voltages greater than 6 to 7 V_{pp} to achieve efficient modulation depths. Low driving voltages below 1.2 V_{pp} potentially allow a modulator to be driven by monolithically integrated high-speed CMOS driving circuits, and also indicate low energy consumption. The Ge-on-Si photodetector, the key device for receiving optical data in a silicon chip, has also shown impressive progress in performance. Several Ge photodetectors have been reported for their large bandwidths and high responsivities. The reported waveguide-type Ge photodetectors [19–24] and vertical-illumination type Ge photodetectors [25–30] have achieved high performance comparable to conventional semiconductor photodetectors.

Simultaneous increases in the photonic integration level and the performance levels of the constituent devices are important. We previously reported a high-efficiency carrier-depletion PN-diode-based 12.5 Gb/s silicon MZ modulator [11] and a 12.5 Gb/s racetrack resonator-type silicon optical modulator [12]. We also presented high-performance vertical-illumination-type Ge-on-Si photodetectors grown by reduced pressure chemical vapor deposition (*RPCVD*), and a 10 Gb/s Ge photoreceiver with −19.5 dBm sensitivity for a BER of 1×10^{-12} at λ~1550nm [28–30], which can readily replace conventional III-V compound semiconductor photodetectors. In this paper, we have investigated simultaneous increases in

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the silicon photonic integration level and the performance levels of constituent silicon photonic devices.

Silicon PICs for chip-level optical data *I/*Os (inputs/outputs), that is, *off-chip* (*inter-chip*) and *on-chip* (*intra-chip*) optical interconnections have been fabricated, into which both silicon MZ modulators (MZM) and Ge waveguide photodetectors (PDs) were monolithically integrated on a Si-on-insulator (SOI) wafer, using a fabrication process compatible with CMOS integration. The integrated modulators of the PICs were optimized in terms of speed, efficiency, driving voltage, and optical loss simultaneously. For the monolithic integration of the Ge PDs, a simplified fabrication process was performed based on selective expitaxy growth (SEG) using RPCVD with omitting chemical mechanical polishing (CMP) and doping for Ge. Also to further increase of the integration level to electronic-photonic IC (EPIC), we hybrid-integrated a silicon PIC chip with 0.13μm CMOS interface circuit chips, which include modulator-drivers, trans-impedance amplifiers (TIAs) and limiting amplifiers (LAs). In the followings, the design, fabrication, performance characterizations up to 30 Gb/s operation are described. The silicon photonic devices and CMOS circuits were designed and fabricated in array form in this work.

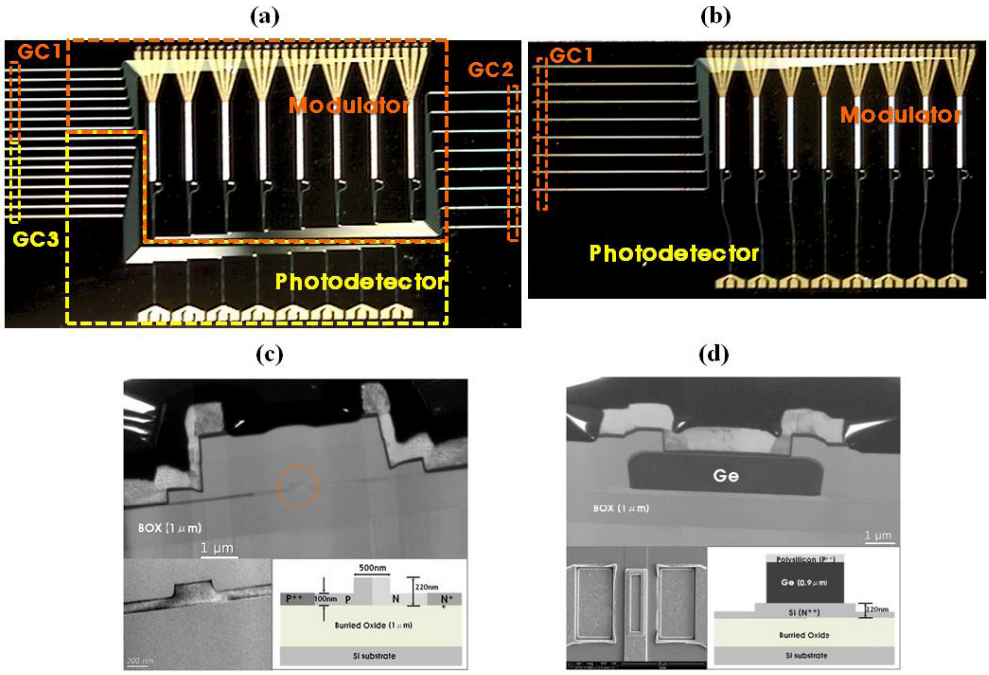

Fig. 1. Top views of microscopy images of the fabricated monolithically-integrated silicon photonic IC *(PIC)* chips for (a) *off-chip* optical interconnect ($PIC_{off\text{-}chip}$) and (b) *on-chip* optical interconnect ($PIC_{intra\text{-}chip}$). The TEM, SEM cross sectional images and schematic diagrams of (c) monolithically integrated silicon MZ modulator phase shifter, and (d) integrated Ge photodetector.

The two types of silicon PICs for the *off-chip* optical interconnect ($PIC_{off\text{-}chip}$) and the *on-chip* optical interconnect ($PIC_{intra\text{-}chip}$) consist of carrier-depletion-type asymmetric MZ modulators for 8-channel photonic transmitter parts, evanescent-coupled waveguide-type Ge PD for 8-channel photonic receiver parts, and grating couplers (GCs) for optical I/O coupling of fiber with silicon waveguides, which were monolithically integrated on a 6-inch SOI wafer with a top Si thickness of 220nm and a buried oxide thickness of 1μm as shown in Fig. 1. Figure 1(a) shows top-view microphotographs of a fabricated 8.7mm×3.5mm $PIC_{off\text{-}chip}$ chip, and Fig. 1(b) shows a fabricated 6.3mm×3.5mm $PIC_{intra\text{-}chip}$ chip. The integrated MZ modulators are shown in the top regions of the $PIC_{off\text{-}chip}$ and the $PIC_{intra\text{-}chip}$ chip, and the

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integrated Ge PDs are shown in the bottom region of each chip. The modulator is defined on an asymmetric Mach-Zehnder interferometer (MZI) with 2x1 multi mode interferometers (MMIs) and lateral PN junction phase shifters embedded in both arms. The Ge PD is integrated onto an 8 μm-wide silicon waveguide. The $PIC_{off\text{-}chip}$ chip shown in Fig. 1(a) has three kinds of GCs for surface normal coupling to fibers. GC1 is for input coupling of the external CW laser light into the chip to feed the MZMs, and GC2 is for the modulated optical outputs transmitted off the chip. GC3 couples the externally modulated input signals into the chip to be delivered to the integrated Ge PDs. The performance of the integrated active components in the $PIC_{off\text{-}chip}$, therefore, can be characterized individually. On the other hand, in the $PIC_{intra\text{-}chip}$ for *intra-chip* optical interconnection, the integrated modulator and the Ge PD are directly connected by the waveguide on the same chip, and GC1 for input coupling of the external CW laser light into the chip is integrated in Fig. 1(b). The optical signal modulated across a MZ modulator is transmitted through the connecting waveguide, the width of which is tapered from 0.5μm to 8μm, to be directly detected by the monolithically integrated Ge PD in the $PIC_{intra\text{-}chip}$. High-resolution focused ion beam (FIB) transmission electron microscope (TEM) and scanning electron microscope (SEM) cross-sectional images and schematic views of the modulator phase shifter and the integrated Ge PD are shown in Fig. 1(c) and Fig. 1(d), respectively.

For the fabrication of silicon PICs, ridge waveguides which configure or connect photonic devices were defined by I-line lithography and high dense plasma (HDP) dry etching process on a 6-inch SOI wafer. The silicon grating couplers with the pitch of 0.315μm were defined on the waveguides. The target etch depth was 70 nm. The ridge waveguide with 100 nm slab height is 0.5μm wide for the modulator, and 8μm wide for the Ge PD. In designing the PN depletion diode for a modulator, the electrical speed of a junction, carrier-dependent loss, and index change efficiency were considered simultaneously. These factors are related to each other based on the device configuration. The free carrier absorption loss is relatively large for the modulation efficient PN diode waveguide. Hole depletion can cause larger refractive index change, whereas electron depletion can give faster electrical response. Lower P-type doping than N-type doping reduces the total capacitance and enhances the operating speed. High N-type doping does not increase the total capacitance, and it enhances phase shift efficiency. The configuration of doping concentrations was designed to achieve a larger bandwidth by reducing junction capacitance with effective refractive-index change for modulation efficiency and relatively reasonable optical loss of the phase shifter. The target doping levels of the lateral PN junctions formed on the phase shifters on both arms of a modulator were 1×10^{18} cm^{-3} for the P-region and 3×10^{18} cm^{-3} for the N-region. The P^{++}, N^{++} implants for a Si modulator and the N^{++} implant for a photodetector were performed to the doping concentration levels of ~1×10^{20} cm^{-3}, followed by an activation process at 900°C for 30 seconds. After a 1-μm-thick SiO_2 layer was deposited, 6×13 μm^2 windows in SiO_2 above the predefined 8 μm-wide waveguides were etched by reactive ion etching (RIE) for the selective expitaxy of Ge. The growth of a 900 nm-thick Ge layer, which comprised a 0.11 μm-thick Ge single-crystal seed layer grown at 400°C and a Ge layer grown at 650°C without further thermal annealing was performed on a predefined window area, followed by the deposition of a 100 nm-thick P^+ polysilicon layer over Ge using RPCVD. This epitaxial growth of the Ge photodetector structure greatly simplifies the monolithic integration process by omitting chemical mechanical polishing and additional doping processes for Ge [28–30]. Metallization with 950nm-thick Ti/TiN/Al_1%Si/TiN and an alloying process were performed. The fabricated devices for channels showed reasonable uniformity in characteristics.

For the device characterization, continuous wave (CW) light from a tunable laser source was coupled to the GC on a chip through a polarization controller to feed a modulator, and the electrical signal from an external driver was connected to drive the modulator in a PIC. In the $PIC_{off\text{-}chip}$ chip, the optical signal modulated across an integrated MZM was transmitted off the chip through the output GC to fiber, and boosted using an erbium doped fiber amplifier (EDFA). This optical signal was measured by an Agilent 86100A Digital Communication

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Analyzer (DCA). Also the external optical input data signal was fed to the GC to be detected by the integrated Ge PD, and this detected electrical signal was measured by the Agilent DCA.

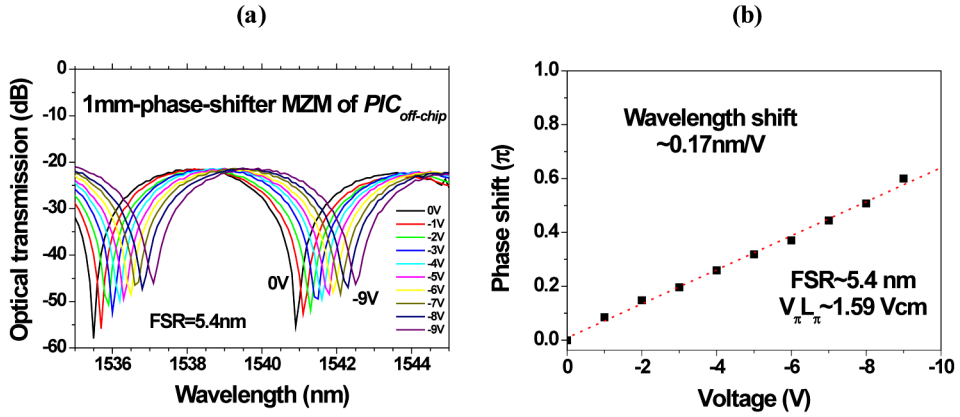

Fig. 2. Optical transmission spectra of the integrated asymmetric MZ modulator (MZM) with 1-mm-long phase shifter at biases from 0V to –9V, and (b) the voltage-induced phase shifts.

Figure 2 plots the measured transmission spectrum of the integrated modulator of the $PIC_{off\text{-}chip}$ as a function of the wavelength, which demonstrates high modulation efficiency. Figure 2(a) shows typical optical transmission spectra of the 1mm-phase-shifter MZM measured at various DC biases. Here, only one phase shifter arm is biased. An avalanche breakdown of the device occurs around −10 V. The black solid curve in Fig. 2(a) represents the transmission spectrum of the unbiased modulator. As is shown in the figure, total optical loss at the maximum of the transmission for a 1mm-phase-shifter MZM is measured to be ~22 dB at λ~1538.1 nm, which includes 1.7 dB/MMI loss, phase-shifter loss of 3.2 dB/mm, passive waveguide propagation loss of ~0.2 dB/mm, and ~7.5 dB loss for each grating coupler. Large coupling loss through grating couplers, which requires resolution of 315 nm, resulted from the I-line lithography limit greater than 350 nm. The free spectral range (FSR) of the integrated modulator is ~5.4 nm. The yellow solid curve represents transmission spectrum of the modulator biased at −6 V, which shows the wavelength shift, Δλ of ~1.0 nm. The voltage-induced wavelength shift, $\Delta\lambda/\Delta V$, is measured to be ~0.17 nm/V. The voltage-induced phase shifts, $\Delta\phi=2\pi\Delta\lambda/\mathrm{FSR}$ for a 1 mm-phase-shifter MZM are shown in Fig. 2(b). The modulation efficiency, $V_\pi L_\pi$, the applied voltage and length required to obtain $\Delta\phi = \pi$, was ~1.59 V·cm.

The high-speed performance of the integrated modulator was characterized by measuring the 3dB bandwidth and eye-diagrams at high transmission rates. The electrical speed of the modulator using a reverse biased PN junction is limited by capacitance. The measured capacitance of the modulator is < 840 fF near −3 V_{DC}. The predicted RC-limit −3dB bandwidth, $f_{-3dB} = 1/(2\pi RC)$, of the modulator was ~22 GHz.

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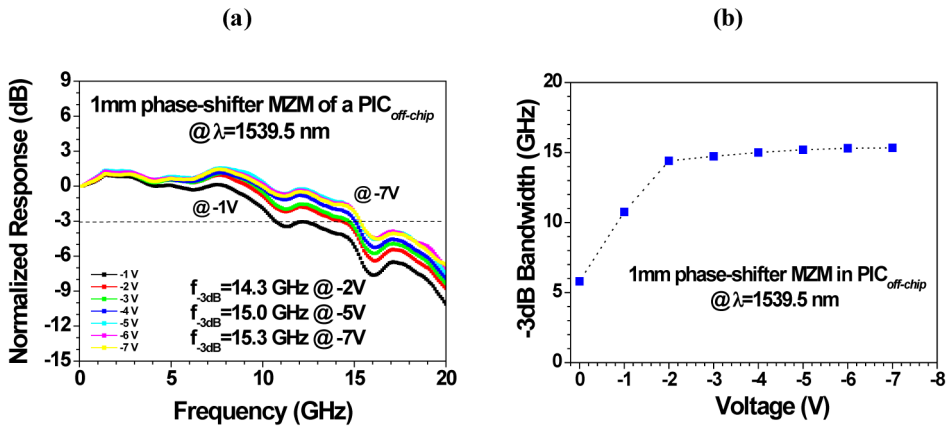

Fig. 3. Frequency response of the MZ modulator shows the −3 dB bandwidth (f_{-3dB}) of 15.0 GHz at −5 V_{DC} bias and 14.3 GHz at −2 V_{DC} bias for the wavelength of 1539.5nm.

The frequency response measurement of the integrated modulator of a $PIC_{off\text{-}chip}$ was carried out using a 20GHz HP 8730A lightwave component analyzer (LCA). The high-speed electrical signal and DC bias voltage were applied to the modulator through a bias-tee and a 40 GHz RF probe. The modulated output signal was amplified using an EDFA, before it was fed into the LCA. The measured frequency responses of the 1mm-phase-shifter MZM with varying reverse bias on one phase-shifter arm are shown in Fig. 3(a). As shown in the graph, the measured bandwidth of a modulator is ~14.3 GHz at −2 V_{DC} bias, and 15.0 GHz at −5 V_{DC} bias. Here, a travelling-wave electrode was not adopted for the device. The discrepancy between the measured bandwidth and the RC-limit bandwidth of the device resulted from the un-optimized metal electrode.

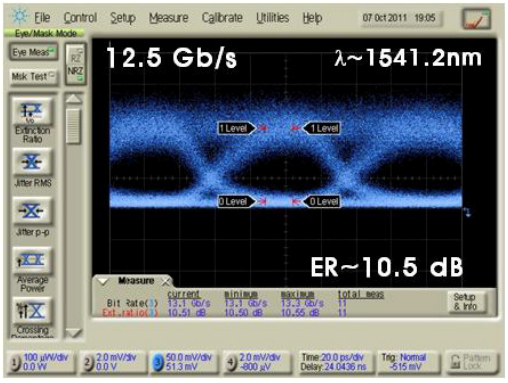

Fig. 4. Low-voltage driving 1.2V_{pp} of the integrated *MZ* modulator with 1-mm-long phase shifter at 12.5 Gb/s operation shows ER~10.5 dB at −3V_{DC} for λ~1541.2nm..

On-wafer measurements of eye diagrams were performed at various bit rates from 12.5 Gb/s to 30 Gb/s for the integrated modulator in $PIC_{off\text{-}chip}$. The non-return-to-zero (NRZ) pseudo-random bit sequence (PRBS) 2^{31}-1 signal of the Anritsu MP1758A pulse pattern generator (PPG) was combined with a DC bias using a bias-tee, and applied to the modulator. The modulator was driven differentially with RF signals from 1.2 V_{pp} to 2.5 V_{pp}. The input CW beam from a tunable laser was passed through a polarization controller and coupled to GC1 of Fig. 1(a) to feed the modulator. Due to the large GC coupling loss, relatively high optical input power was required in the measurement. The modulated output signal from the $PIC_{off\text{-}chip}$ chip was coupled to fiber probe aligned with GC3. EDFA was used to boost the modulated output signal, and a tunable wavelength filter was used before light signal was

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detected with a Discovery DSC1OH 43GHz photodiode and the Agilent DCA with an 8611A 70 GHz remote sampling module.

The low driving voltage of 1.2 V can allow a MZ modulator to be driven by monolithically integrated high-speed 0.13μm CMOS driving circuits. Figure 4 shows low-voltage operation characteristics of the 1 mm-phase-shifter MZM of the $PIC_{off\text{-}chip}$ driven differentially with $1.2V_{pp}$ using a 12.5 Gb/s PRBS signal source. The measured optical eye exhibits an ER of 10.5 dB at $-3V_{DC}$ bias for λ~1542.1 nm. The additional optical loss of ~4dB is measured at the '1' level of the signal compared with the maximum transmission case. This represents a large improvement compared to our previous result using a similar modulator [11].

Fig. 5. High-speed operations of an integrated 1 mm-phase-shifter *MZM* driven in differential mode of 1.2 V_{pp} for 20Gb/s and 30Gb/s modulations for λ~1541.2 nm in the $PIC_{off\text{-}chip}$. Measured ERs are 9.1 dB at $-3V_{DC}$ for 20Gb/s modulation, and 7.2 dB at -4 V_{DC} for 30Gb/s modulation.

Figure 5 shows measured eye-diagrams of the integrated 1 mm-phase-shifter MZM of the $PIC_{off\text{-}chip}$ driven differentially with 1.2 V_{pp} swing using 20 Gb/s and 30 Gb/s PRBS signal for λ~1541.2 nm. As seen in the figure, the measured eye diagrams exhibit good eye openings up to 30 Gb/s operations. The measured ER is 9.1 dB at 20 Gb/s data transmission with −3 VDC bias, and 7.2 dB at 30 Gb/s data transmission with −4 VDC bias.

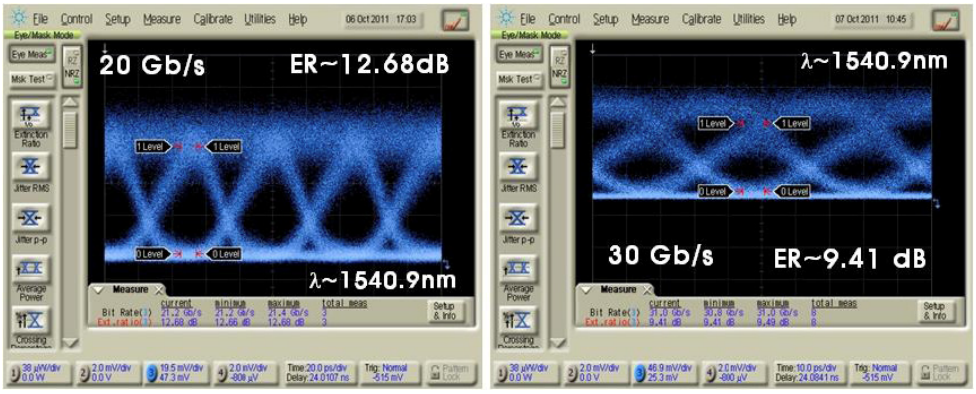

Fig. 6. On-wafer measurements of a monolithic-integrated 1 mm-phase-shifter MZM driven in differential mode of 2.5 V_{pp} for 20 Gb/s and 30 Gb/s operation, show ~12.6dB ER at 20Gb/s, ~9.4dB ER at 30Gb/s, with $-5V_{DC}$ bias in the $PIC_{off\text{-}chip}$.

The higher driving voltage of 2.5 V_{pp} resulted in larger extinction ratios. Figure 6 exhibits the performance of the integrated 1 mm-phase-shifter MZM of the $PIC_{off\text{-}chip}$ for $2.5V_{pp}$ drive with −5 V_{DC} bias. The measured ERs are 12.68 dB and 9.41 dB for 20 Gb/s and 30 Gb/s operation, respectively. Here, the measured additional optical losses at the '1' level of the

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signal compared to the maximum optical transmission are 1.4dB and 1.9dB for 20 Gb/s and 30 Gb/s operation, respectively. Also, the same modulator at 12.5 Gb/s operation exhibits a high ER of 13.45 dB for $2.5V_{pp}$ drive.

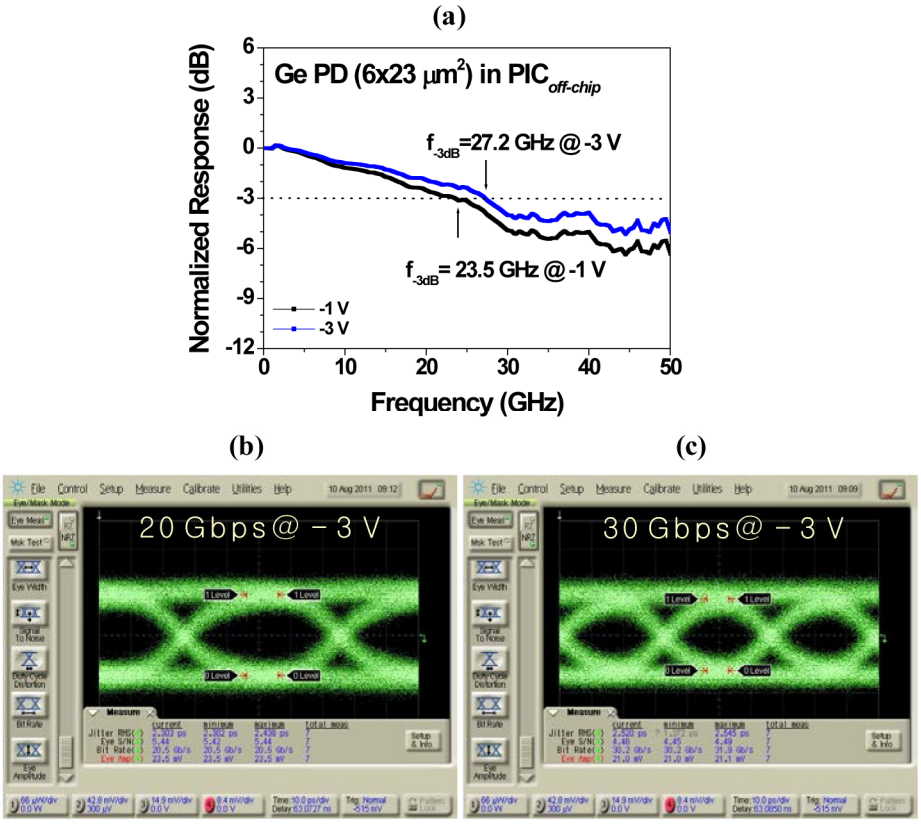

Fig. 7. (a) On-wafer measurement for the frequency response of integrated 6 × 23μm^2 Ge-PIN waveguide photodetector, which shows −3dB bandwidth (f_{-3dB}) greater than 27 GHz at −3V. (b) The eye-diagram measured at (b) 20 Gb/s and (c) 30 Gb/s operations at −3V bias.

For characterization of the 6×23μm^2 Ge PIN waveguide photodetector integrated on the silicon waveguide in a $PIC_{off\text{-}chip}$, the external light data signal was delivered to the *PD* through GC3 of Fig. 1(a) coupled to an optical fiber probe. The device exhibited low dark current under 700 nA at 1 V reverse bias. The frequency response was measured by impulse response measurement with a Pritel femtosecond pulse laser and the Agilent DCA with an 8611A 70 GHz remote sampling module. Figure 7(a) shows the normalized frequency response of a Ge PD. As shown in the figure, the measured −3dB bandwidths are 23.5 GHz at −1V bias and 27 GHz at −3 V bias. Figures 7(b) and 7(c) exhibit good eye-diagrams of the Ge PD at 20 Gb/s and 30 Gb/s operation at −3V bias for λ~1550 nm. The measured responsivity was ~0.3 A/W. This value is lower than expected. The Ge PD on 220nm SOI showed lower responsivity than the measured ~1 A/W responsivity of the same PD integrated on 450nm SOI. This reflects that Ge SEG process on the over-etched thin top silicon in SOI can affect the quality of the Ge epilayer in the bottom region, and this is under investigation. This suggests room for further optimization of the SEG process on the thin top Si layer of a SOI in RPCVD.

As are shown in the above, both integrated modulators and Ge photodetectors of the $PIC_{off\text{-}chip}$ have demonstrates 30 Gb/s operations in data transmitting and receiving separately. The modulators showed improved characteristics of high modulation depth at high-speed

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operations with low-voltage driving voltages, and the integrated photodetectors exhibited high-speed performance with low dark current.

In the measurements of the $PIC_{intra\text{-}chip}$, where intra-chip photonic interconnect could be investigated, higher optical input power was required than in $PIC_{off\text{-}chip}$ case. The CW light from a tunable laser was amplified by an EDFA and was coupled into the grating coupler through an optical filter and a polarization controller to feed the integrated MZM. Also, the PRBS electrical input signal was applied to drive the modulator. The optical signal modulated by the MZM transmits through the connecting silicon waveguide to be detected and converted into the electrical output signal by the monolithically integrated Ge PD in the same chip. The electrical output signal reflecting *on-chip* optical data interconnection was measured by the DCA with an 86105C 20 GHz electrical module.

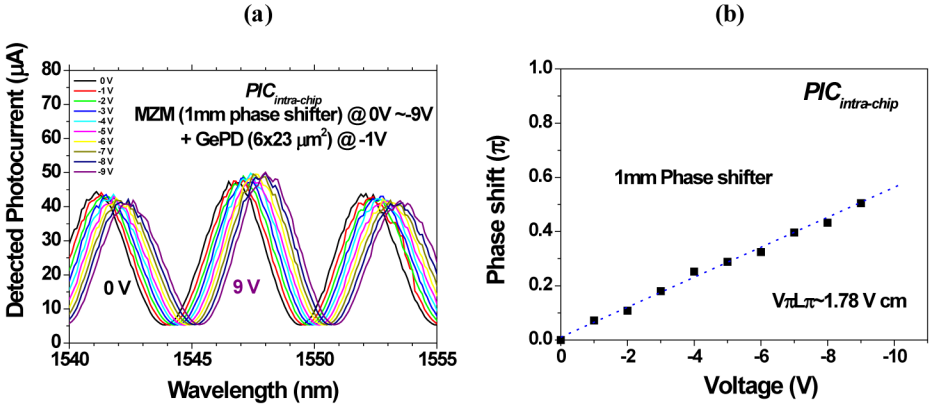

Fig. 8. The detected photocurrent curves for the optical transmission spectra of a integrated modulator by the monolithically integrated PD in the $PIC_{intra\text{-}chip}$. The modulator is biased from 0V to –9V, and the PD is biased –3V.

Figure 8(a) shows the measured photocurrent curves corresponding to the typical optical transmission spectra through an integrated 1 mm-phase-shifter MZM, detected by the monolithically integrated Ge PD in a $PIC_{intra\text{-}chip}$ chip. Here, the modulator was biased from 0V to −10V, and the detecting PD was biased at −1V. The measured FSR of the integrated modulator is ~5.6 nm in the figure. The black solid curve is the transmission spectrum through the unbiased modulator, and the violet solid curve is the measured photocurrent curve for the transmission spectrum through the modulator biased at −9 V, which shows the wavelength shift, $\Delta\lambda$ ~1.4 nm. The voltage-induced wavelength shift, $\Delta\lambda/\Delta V$ was measured to be ~0.157 nm/V. Figure 8(b) shows the voltage-induced phase shifts as a function of the modulator bias voltage. Although the same modulators as those used in the $PIC_{off\text{-}chip}$ were integrated, the modulation efficiency in the $PIC_{intra\text{-}chip}$ were measured to the larger value of $V_\pi L_\pi$ ~1.78 V·cm.

Figure 9 shows on-wafer measurements of optical eye diagrams in the $PIC_{intra\text{-}chip}$, where *on-chip* data transmissions of 12.5 Gb/s up to 20 Gb/s occur from the integrated 1 mm-phase-shifter MZM to the monolithically integrated Ge PD at λ~1542.7 nm. The NRZ PRBS signal from the Anritsu PPG was applied to the MZM. Here, the modulator was driven with a 2.5 V_{pp} signal at $-5V_{DC}$ bias and the PD was biased at −3V. This measured eye patterns were raw signals detected by the integrated Ge *PD* without any preamplifier *IC*s involved.

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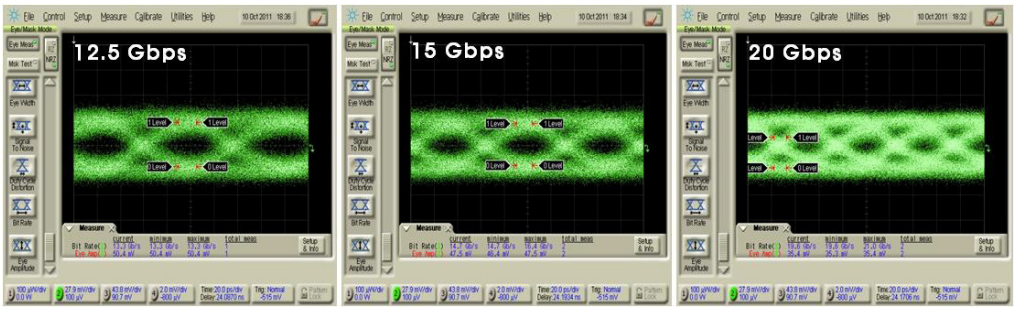

Fig. 9. On-wafer measurements of optical eye-diagrams for 12.5Gb/s, 15 Gb/s and 20 Gb/s on-chip optical interconnect signals in the monolithic integrated $PIC_{intra\text{-}chip}$, with $2.5V_{pp}$ at the wavelength $\lambda = 1542.7$ nm.

Although the same devices were integrated, the performance showed degradation compared with that of the 30 Gb/s $PIC_{off\text{-}chip}$ case, resulting from the high input optical power. The background heat in the chip and the ASE noise of EDFA limit the performance of both integrated devices. Further improvement in the coupling efficiency of the grating coupler and

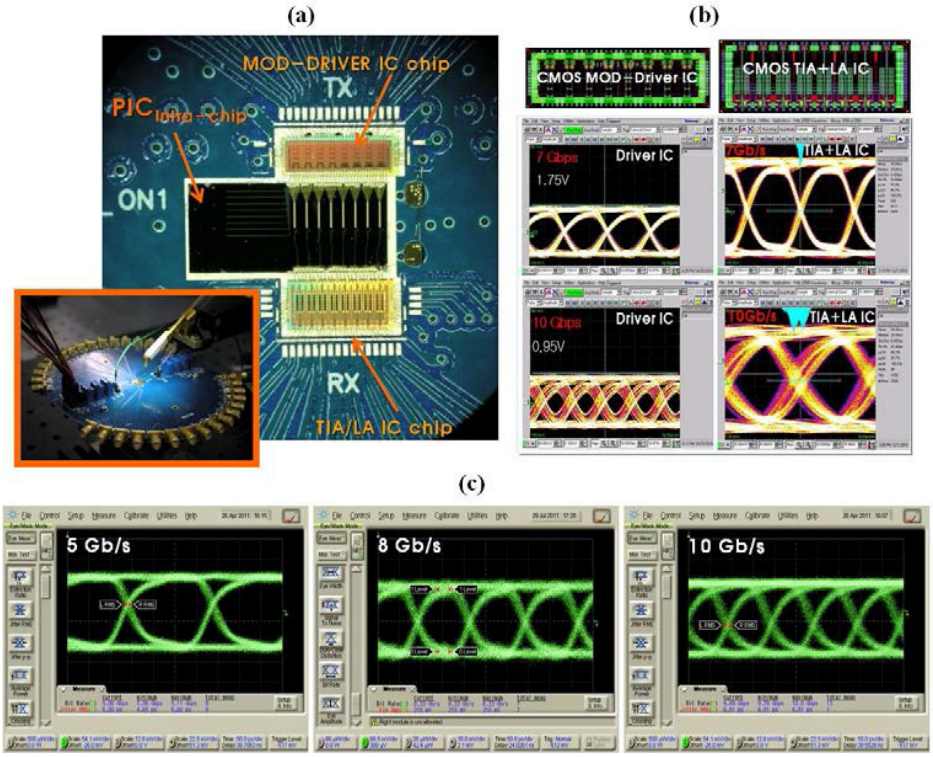

Fig. 10. (a) Silicon EPIC on a test PCB, where a silicon $PIC_{intra\text{-}chip}$ chip is hybrid-integrated with 0.13µm CMOS VLSI chips. Top chip is a CMOS modulator-driver IC, the middle chip is a silicon $PIC_{intra\text{-}chip}$ chip, and the bottom chip is a TIA-LA CMOS IC chip. Test setup for hybrid silicon EPIC characterization is shown in the inset. (b) The measured electrical eye of CMOS ICs at 7 Gb/s and 10 Gb/s operations. (c) Eye diagrams of the hybrid silicon EPIC at 5 Gbps, 8 Gbps, and 10 Gbps measured with 1.3 V_{pp} PRBS signal. Here, on-chip *EPIC* characteristics are limited by the 0.13µm CMOS interface circuits.

the responsivity of the integrated PD with the use of a smaller MZ modulator with high modulation efficiency can reduce the burden of high input power and result in improved *on-chip* transmission characteristics in the $PIC_{intra\text{-}chip}$ chip.

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To further increase the integration level to the electronic-photonic IC, we hybrid-integrated a silicon $PIC_{intra\text{-}chip}$ chip with 0.13μm CMOS interface circuit chips. Figure 10(a) shows photographic images of the hybrid silicon EPIC. The test setup for EPIC characterization is shown in the inset. The EPIC assembly is die-attached and wire-bonded on a test PCB, and a fiber is aligned with the grating coupler for optical input. In the figure, the top chip is a CMOS modulator-driver IC, the middle chip is a silicon $PIC_{intra\text{-}chip}$ chip and the bottom chip is a CMOS TIA-LA IC chip. The CMOS modulator-driver IC is the cascode voltage-mode driver designed for high voltage swings up to $3V_{pp}$ with a measured bandwidth of 5 GHz. The *TIA* is designed based on an RGC feedback loop with two coupled shunt series peaking inductors [36]. The measured bandwidth of the TIA in the chip is 7.9 GHz. The limiting amplifier is designed to have 6 gain stages with an offset compensator. The buffer and output driver IC are also included in the TIA-LA IC chip. Figure 10(b) shows the electrical performance of the modulator-driver IC and the TIA-LA IC measured at 7 Gb/s and 10 Gb/s operation. The size of the 8-channel CMOS modulator-driver chip is 4.3mm × 1.5mm, and the chip size of 8-channel CMOS TIA and LA is 4.2mm × 1.8mm. Figure 10(c) shows the measured "eye" diagram of the hybrid silicon EPIC for *on-chip* optical interconnection for 5, 8, 10 Gbps operation with $V_{RF} = 1.3\ V_{pp}$. As seen in the figure, the performance of the EPIC is limited by the performance of the 0.13μm CMOS interface circuits. Upgrading in CMOS interface ICs with a lower driving voltage design can improve the performance of silicon EPICs. With continued improvements in CMOS interface ICs and silicon photonic devices, we expect to develop even more efficient silicon PICs and EPICs leading to high performance interconnections for future inter/intra-chip applications.

In conclusion, we presented the performance of silicon photonic integrated circuits for off-chip optical interconnects ($PIC_{off\text{-}chip}$), where monolithically integrated PN depletion-mode MZ modulators and evanescent-coupled Ge waveguide PD on a SOI wafer demonstrated data transmissions up to 30 Gb/s. For the low-voltage drive of $1.2\ V_{pp}$, the integrated 1mm-phase-shifter modulator of the $PIC_{off\text{-}chip}$ demonstrated a phase shift efficiency of $V_\pi L_\pi$ ~1.59 V/cm with 10.5dB ER for 12.5 Gb/s modulation, 9.1dB ER for 20 Gb/s modulation and 7.2dB ER for 30 Gb/s modulation. The integrated Ge waveguide PD grown by RPCVD showed good eye diagram for 30 Gb/s operations with low dark current levels. Also, the silicon PIC for *intra-chip* optical interconnect ($PIC_{intra\text{-}chip}$), where the light signal modulated by the integrated modulator is detected by the monolithically integrated Ge *PD* in the same chip, exhibited *on-chip* optical interconnection up to 20 Gb/s. We also presented the silicon EPIC, where a silicon $PIC_{intra\text{-}chip}$ chip and 0.13μm CMOS interface circuit chips for modulator-driver and preamplifier IC were hybrid-integrated. Based on our results, further optimizations in the smaller *MZ* modulator with high efficiency and the integrated PD, and improvement in CMOS interface ICs can lead to more efficient silicon PICs and EPICs for future inter/intra-chip interconnect applications.

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