Low Power 60 dB Gain Range with 0.25 dB Resolution CMOS RF Programmable Gain Amplifier for Dual-band DAB/T-DMB Tuner IC

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***Abstract*- Low power CMOS RF digitally programmable gain amplifiers for dual-band (Band-III and L-Band) DAB/T-DMB receiver IC are implemented using 0.18 μm CMOS process. For a stable operation among large interference situation, it is required to have wide gain range and fine resolution in RF domain. In order to meet such requirements, various programmable gain amplifier architectures are proposed. Also employing a Differential Multiple Gated TRansistor (DMGTR) technique which is a differential circuit gm″ cancellation method, maximum 22 dB IIP3 improvement is obtained. The IC exhibits 60 dB gain range with 0.25 dB resolution, 2.7 dB NF, -14 dBm IIP3 and 42 dB voltage gain at 22 mW power consumption for L-Band case, 50 dB gain range with 0.25 dB resolution, 3 dB NF, -5 dBm IIP3 and 28 dB voltage gain for Band-III case at 16mW power consumption.**

***Index Terms*— CMOS, DAB, IIP3, PGA, Linearity.**

I. INTRODUCTION

Digital Audio Broadcasting (DAB) provides high quality audio broadcasting services and other multi-media broadcasting services in Europe and some other countries in the world. Especially, it gets a strong attention in mobile digital TV (D-TV) markets, because, Terrestrial Digital Multimedia Broadcasting (T-DMB) which is evolved from DAB and will provide its service in near future in Korea shares same physical layer with DAB. T-DMB is terrestrial mobile D-TV broadcasting which is newly tried in Korea.

In European Telecommunication Standards Institute (ETSI) standard, dual-band (Band-III, 174-245MHz and L-band, 1450-1492MHz) is required for the DAB service. And T-DMB uses Band-III only. For a wide market purpose, it is better to have dual-band for tuner IC to cover such a various environment.

Because Band-III exists among traditional terrestrial broadcasting band, there exist hundreds of other channels which play as interferers. To cope with those varying power interferers, it is better to have large gain range in RF domain. Also fine gain step help to relax following stage's linearity burden as shown in Fig. 1. Fig. 1 (a) shows gain control strategy of D-TV system which is composed of RF part and IF part. The difference between those two parts lies in the channel selection filter which removes other interferers exists between them. When a input signal power including interferer power is low level, the receiver performance is dominated by its sensitivity. Thus, the RF gain is set to its maximum and the IF gain covers input power variation. On the other hand, when a input power is high, for example, higher than some critical point (named take-over point), the receiver performance is limited by distortion products which are generated by multiple interactions between interferers. Thus, it is better to give attenuation in RF domain. Therefore, after take-over point, RF part takes over whole receiver gain control while IF gain holds its lowest value. Fig. 1 (b) explains the relationship between RF gain step and following block's linearity. If the RF gain step is finer, the following block's linearity burden can be relaxed as much. Therefore, it is important to give wide gain range with fine resolution attenuation in RF domain of D-TV system.

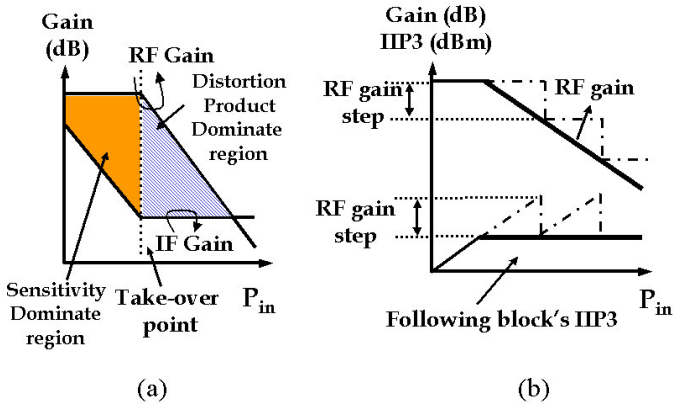

Fig. 1. (a) Gain control strategy in a DTV system and (b) Relationship between RF gain step and following block's IIP3.

In this paper, various new programmable gain amplifier architectures were designed and measured in order to provide wide gain range with fine resolution in RF domain. Also applying Differential Multiple Gated Transistor (DMGTR) [1] technique and above gain control techniques, we obtained dual band low power highly linear CMOS RF digitally programmable gain amplifier (RF PGA) having wide gain range with fine resolution gain step.

II. RF PROGRAMMABLE GAIN AMPLIFIER

In order to cover wide gain range with fine resolution in RF PGA, gain attenuation is divided into several parts as shown in Fig. 2. For Band-III RF PGA, it has 3 parts and for L-Band it has 4 parts. Because of gain reduction of high frequency application, L-Band has two more gain parts. It comprises of a dB-linear 50 dB gain range with 0.25 dB resolution for Band-III, 60dB for L-Band. Fig. 3 shows circuit

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diagram of proposed Band-III RF PGA. In L-Band RF PGA, cascode LNA at first stage and differential amplifier at third stage is added for high frequency gain.

In the first gain attenuation of Fig. 3, to attain a wide gain range, a resistive attenuator is used. Previous variable gain amplifiers use a single amplifier with switches [2] or multiple amplifiers without switches [3]. The first one requires an input switch even at the highest gain mode, which results in high NF. And the second one suffers from bandwidth limitation, because of the multi-amplifier configuration. Thus, we find a compromise between both structures using only two amplifiers. Here, we separate the high gain mode amplifier from the low gain mode amplifier, using same amplifier, and with the switch moved back after the amplifier as shown Fig. 3. One amplifier is for the highest gain mode, and the other is for lower gain mode with the switch place after the amplifiers. With this approach, we can obtain a low NF (which only matters in highest gain mode) and large bandwidth. Also each attenuator is isolated by different wells in a triple-well technology and bond wire for each attenuator is separated to guarantee enough attenuation as shown in Fig. 4.

The first stage amplifier is composed of Common Source (CS) and Common Gate (CG) configuration that supplies single-ended input to differential output as shown in Fig. 3, A. Also CG amplifier provides resistive 50 ohm over wide frequency. Second Amplifier employs DMGTR which will be discussed later in detail to improve linearity. The first and second amplifier uses load switching to cover 8dB with 4dB resolution and 4dB with 1 dB resolution respectively.

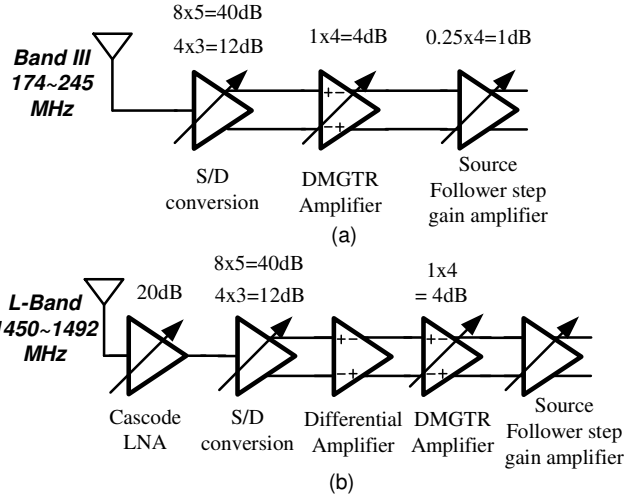

Fig. 2. Gain control strategy of (a) Band-III (b) L-Band and RF PGA.

III. SOURCE FOLLOWER STEP GAIN AMPLIFIER

Last stage in the RF PGA should have small impedance to deliver output voltage effectively to next stage, and should have a high linearity to cover preceding stage gain. To meet such requirements source-follower is the best configuration for last stage in RFPGA. Source follower has small output impedance (=1/gm) and its linearity can be boosted up by current feedback.

To attain fine gain step as well as low output impedance,

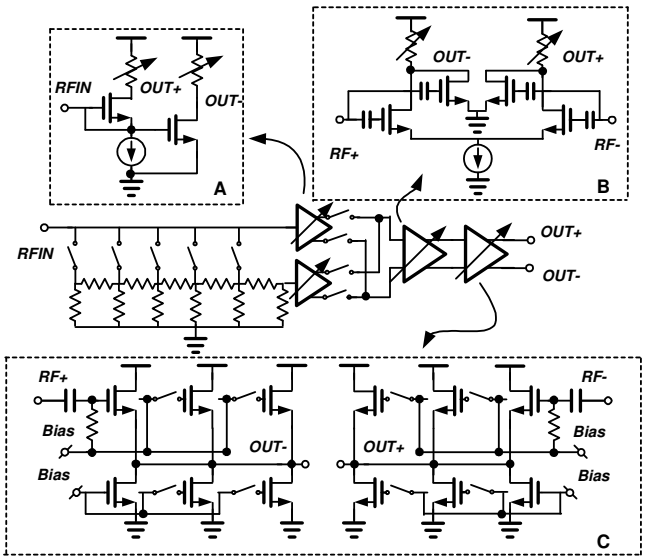

Fig. 3. Circuit diagram of proposed Band-III RFPGA.

source follower fine step gain controller is proposed as shown in Fig. 3, C. To make a simple explanation, let's think of only one gain control as shown in Fig. 5. A fine step gain amplifier is composed of source follower (M1, M3) whose gain is expressed with (1) and gain control block (M2, M4), where gm is transconductance and R_L is load resistance Both the RF signal and the DC bias are applied to the gate of M1 transistor (width: W1), and for the gain control block, only DC bias is applied to the gate of M2 transistor (width: W2). Also the current of M2 transistor is determined by the ratio W1/W2, by adjusting current source sizes with same ratio. Then, the gain is expressed by equation in (2). The relationship between gm_1 and gm_2 determines gain. Because gm is the function of width when same bias is applied as explained in (3) and (4), gain is adjusted by switching M2 transistor. With adding more gain control transistors, we can obtain more gain controllability.

The dB-linear relationship is approximately met, when W1>>W2, as explained in (5). Thus, the proposed method is appropriate for fine resolution gain control amplifier. Because this gain control method is the function of transistor width ratio, it is robust to possible mass production variations.

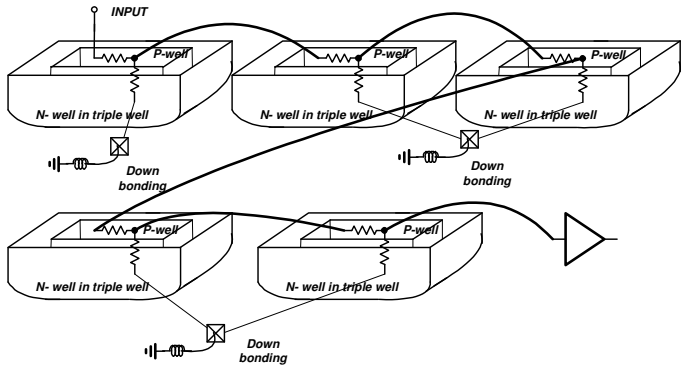

Fig. 4. Resistive attenuators are isolated by different well in triple well technology.

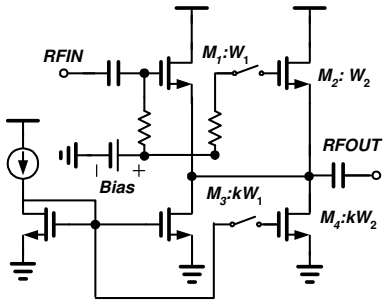

Fig. 5. Schematic diagram of source follower step gain amplifier

$$A_V = \frac{g_m \times R_L}{1 + g_m \times R_L} \tag{1}$$

$$A_V = \frac{\frac{1}{g_{m2}} // R_L}{\frac{1}{g_{m2}} // R_L + \frac{1}{g_{m1}}} \cong \frac{\frac{1}{g_{m2}}}{\frac{1}{g_{m1}} + \frac{1}{g_{m2}}} = \frac{g_{m1}}{g_{m1} + g_{m2}} \tag{2}$$

$$g_m = \mu_n C_{ox} \frac{W}{L}(V_{GS} - V_{TH}), \quad g_m \propto kW \tag{3}$$

$$A_V = \frac{g_{m1}}{g_{m1} + g_{m2}} = \frac{kW_1}{kW_1 + kW_2} = \frac{W_1}{W_1 + W_2} \tag{4}$$

$$\frac{\Delta dB(A_V)}{\Delta W} = \frac{\log\left(\frac{W_1}{W_1 + W_{n+1}}\right) - \log\left(\frac{W_1}{W_1 + W_n}\right)}{W_1 + W_{n+1} - (W_1 + W_n)}$$
$$= \frac{\log\left(\frac{W_1 + W_n}{W_1 + W_{n+1}}\right)}{W_{n+1} - W_n} = \frac{\log\left(1 + \frac{W_n - W_{n+1}}{W_1 + W_{n+1}}\right)}{W_{n+1} - W_n} \tag{5}$$
$$= \frac{\log\left(1 + \frac{-\Delta W}{W_1 + W_{n+1}}\right)}{\Delta W} \cong \frac{-\frac{\Delta W}{W_1}}{\Delta W} \cong -\frac{1}{W_1}$$

IV. DMGTR AMPLIFIER

A differential topology is one of the best ways to reject digital circuitry noise, which usually acts as common mode disturbance in a SOC. There are two kinds of differential circuits, Fully Differential Amplifier (FDA) and Pseudo Differential Amplifier (PDA). It is better for the SOC to use FDA which has a higher common mode noise rejection than a PDA. In FDA, the negative value of gm″ can not be moved to positive value by changing the bias condition as shown in Fig. 6 (a), (b). In the case of PDA, however, it can be moved to positive value by changing the bias voltage as shown in Fig. 6 (c), (d). Because in FDA, two branch currents (I+, I-) always meet at the center of the I-V curve irrespective of the bias condition of tail current source as shown Fig. 6 (a), (b). While in PDA, those two currents can meet at any point, depending on the bias voltage as shown Fig. 6 (c), (d). That means in

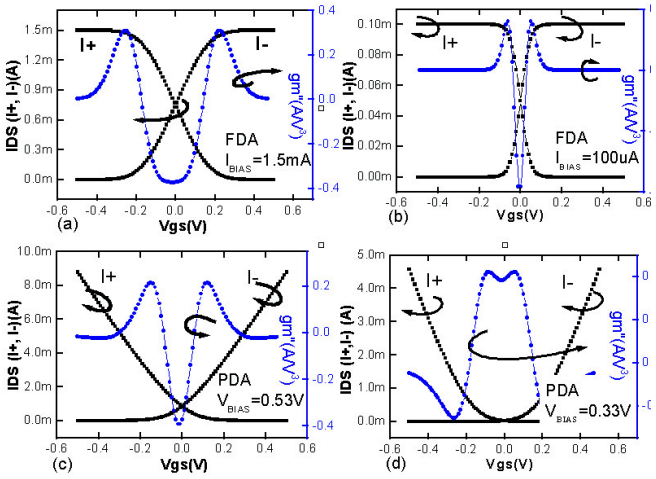

Fig. 6. (a) FDA current and gm″ at high current bias region. (b) FDA current and gm″ at low current bias region. (c) PDA current and gm″ at saturation region. (d) PDA branch current and gm″ at weak inversion region.

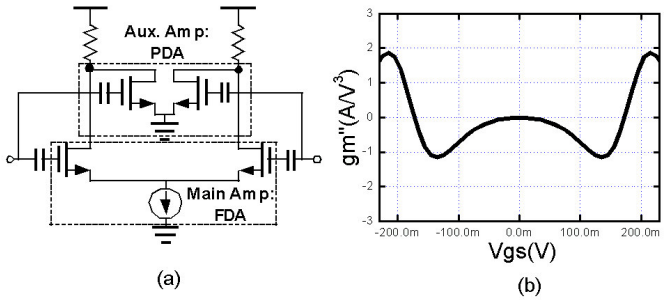

Fig. 7. (a) Proposed DMGTR amplifier schematic diagram (b) linearized gm″ range of DMGTR.

PDA, its negative value of gm″ of differential current can be moved to a positive value by changing the bias voltage. From the above consideration, the negative value of gm″ which degrades linearity in FDA can be compensated with a positive value of gm″ in PDA by adjusting the bias and transistor size of PDA. Here, we propose a high linearity differential amplifier, Differential Multiple Gated (DMGTR) amplifier using FDA as the main amplifier and PDA as the auxiliary amplifier as shown in Fig. 7, (a). Fig. 7, (b) shows the linearized gm″ of DMGTR. This method does not require extra power consumption, as the PDA for compensating gm″ is biased at near threshold voltage regime. Because most of the signal is amplified by main amplifier, the benefit of differential circuits like high CMRR, is still maintained. Also the RF characteristics, like NF, gain are not degraded in proposed amplifier.

V. MEASUREMENT RESULT

Proposed RF PGAs were fabricated by 0.18μm CMOS process. All pins are ESD protected. Fig. 8 shows the NF and voltage gain measurement result of L-Band RF PGA at its maximum gain setting. It shows 2.5 dB NF and 42 dB voltage

gain. For Band-III RF PGA shows 3 dB NF and 28 dB voltage gain. Fig. 9 shows the full range gain step measurement of Band-III RF PGA. It covered 50 dB gain range with 0.25 dB resolution, for L-Band RF PGA has 60 dB gain range with 0.25 dB resolution. Table 1 summarizes measurement results of proposed RF PGAs.

DMTR measurement result shows maximum 18 dBm IIP3, 5 dB NF, 10 dB voltage gain at 2.9 mA current consumption while conventional FDA shows -4.3 dBm IIP3, 5dB NF 9 dB voltage gain at 2.8mA. Measured frequency is 245MHz. Fig. 10 shows IIP3 improvement ($IIP3_{DMGTR}$-$IIP3_{FDA}$) over supply voltage (1.6~2.0V) and temperature variations(-40~80°C). It shows at least 10 dB IIP3 improvement over all variations.

Fig. 11 shows successful reception of live mobile D-TV using Low-IF tuner IC includes this work. The tuner IC also successfully received experimental broadcasting of T-DMB in Korea. It can handle more than 110 dB variation of RF input power by virtue of wide dynamic range of RF PGA.

VI. CONCLUSION

Low power high linearity CMOS RF PGAs for dual band DAB/T-DMB tuner IC was fabricated and measured. To obtain wide gain range with fine resolution, various new step gain amplifier architectures were proposed and verified by measurement which shows 60 dB gain with 0.25 dB resolution range for L-Band RF PGA and 50 dB gain range with 0.25 dB for Band-III RF PGA.

Also, a differential circuit linearity improvement technique, DMGTR was applied. Measurement results of DMGTR amplifier showed maximum 22 dB improvement of IIP3 without sacrificing other characteristics such as gain, NF and CMRR with wide linearization window. Thus, for possible mass production variations, such as supply voltage and temperature variations, it showed at least 10 dB IIP3 improvement without extra power consumption.

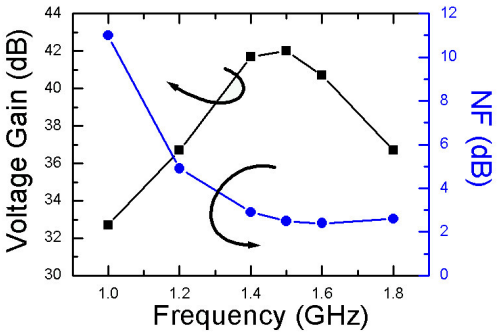

Fig. 8. NF and gain of L-Band RFPGA @ maximum gain

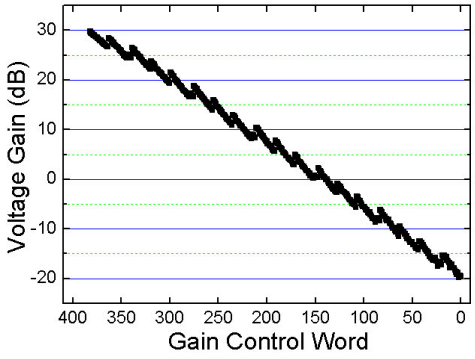

Fig. 9. Gain range measurement result of VHF RFPGA, it covers 50 dB with 0.25 resolution seamlessly. Measured frequency is 245MHz

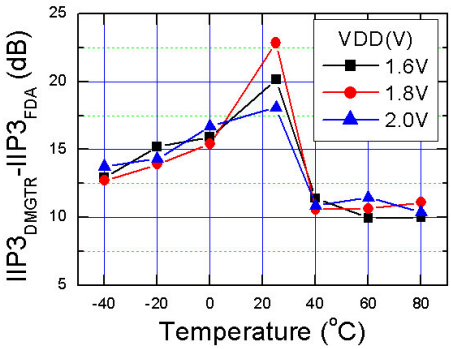

Fig. 10. IIP3 improvement over temperature and supply voltage variations.

Table 1. Measurement summary of Band-III and L-Band RF PGAs

Band	Gain	NF	IIP3	Gain range/ Gain step	Power
Band-III (174~245 MHz)	28dB	3dB	-5dBm	50dB/0.25dB	16mW
L-Band (1450~ 1492MHz)	42dB	2.7dB	-14dBm	60dB/0.25dB	22mW

Fig. 11. Successful reception of mobile D-TV using Low IF tuner IC includes this work.

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