Low power, tunable active inductor and its applications to monolithic **VCO** and **BPF**

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Abstract

A novel tunable active inductor for low power operation is presented. The DC power consumption of the proposed scheme is about 1/3 of conventional one with wider range of tunability and higher Q. The new bias scheme using the parallel and the series bias resistors reduces the number of bias pins and stabilizes the bias, effectively. This novel low power tunable active inductor is applied to wideband (35 % tuning ratio) monolithic VCO and wide tunable (14 % tuning ratio) monolithic BPF.

INTRODUCTION

In wireless, portable telecom equipment, the most bulky and expensive parts are VCO (Voltage Controlled Oscillator) and BPF (Band Pass Filter) which need high Q passive elements. This high Q stabilizes frequency characteristics of VCO and Filter and it reduces the loss. However, the spiral inductor on semiconductor and the varactor using FET have low Q because of the metallic loss and the limited substrate doping, respectively. Therefore, a considerable amount of interest has been shown in the use of high Q [1]-[4], tunable active inductors [3]-[4].

However, conventional tunable active inductors (TAI) had the problems that their DC power consumption is too high and their circuits require many bias pins. Low power operation becomes important in wireless, portable telecom equipment due to poor capacity of battery.

We suggest the new topology to consume the low DC power and the new bias scheme to reduce the number of bias pin and to have more stable bias. The previous tunable active inductor used in [4] had high Q and good performances among the existing topologies, so we compare the DC power consumption of ours with one of theirs [4]. Moreover, using our low power tunable active inductor (LPTAI), we apply to fully monolithic, wide tunable VCO and BPF.

DESIGN OF LOW POWER TUNABLE ACTIVE INDUCTOR

The principle of active inductor is almost the same as one of active gyrator [3]. This active gyrator can be realized by connecting inverting amplifier to non-inverting one in parallel and back-to-back. This gyrator converts the parallel-connected C//R into the serial-connected L-R. This series resistance plays the role to degrade the Q of inductor. The commonly used common-gate amplifier as non-inverting amplifier has the output impedance which is parallel-connected C//R due to g_{ds}. Thus, we use the common-gate cascode amplifier instead of common-gate one as non-inverting amplifier in our scheme. Although we consider the output transconductance (g_{ds}) in the transistor equivalent model, the output resistance of common-gate cascode amplifier is slightly negative.

To reduce the DC voltage drop, we adopt the common-source amplifier instead of common-source cascode one as inverting amplifier. The ac schematic of our new LPTAI is shown in Fig. 1. Here, R_{FB} and R_G are used to control the inductance and series loss.

Because all of the gate capacitance is small, that is, it has high impedance, the large bias resistors (> 6 KΩ) are required to access to each gate. Thus, it is difficult to use parallel resistor chain biasing and

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conventional TAI's require many pins [1], [4]. In order to reduce the number of bias pin, we insert the series choke resistors (R_{SB}) toward parallel resistor chain ($R_{1\sim5}$). This new bias scheme and the improved active-load [6] change bias currents easily and stabilize the bias, simultaneously. The designed schematic of LPTAI is drawn in Fig. 2.

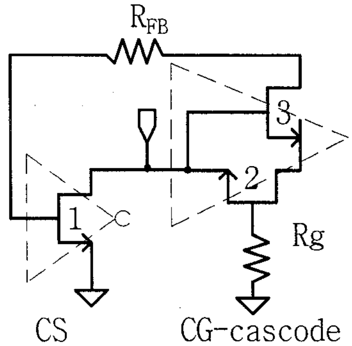

Fig. 1. The ac schematic of our low power tunable active inductor

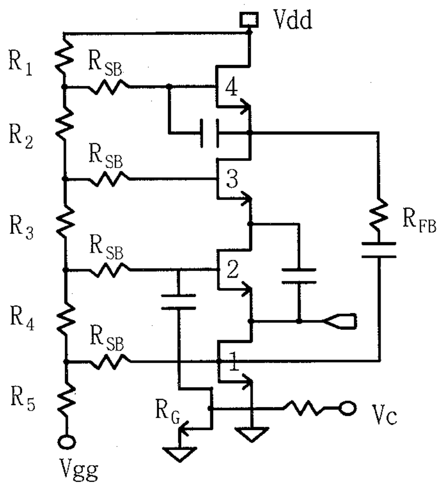

Fig. 2. The schematic of our LPTAI

MMIC REALIZATION AND MEASUREMENT

The GaAs MMIC was fabricated at the GEC-Marconi (Caswell) foundry, using their standard low-cost 0.5 μm MESFET foundry process. The fabricated chip of LPTAI is shown in Fig. 3. Fig. 4 shows the measured performance of LPTAI varying with tuning voltage and demonstrates ultrahigh Q at narrow band. At each tuning voltage, the consumed DC power and the calculated inductance in the equivalent models are summarized in table 1. The inductance can be controlled by Vgg & gate resistance (Rg) and Vdd & gate resistance (Rg). The calculated inductance is varied from 1.9 nH to 3.8 nH as shown in Table 1.

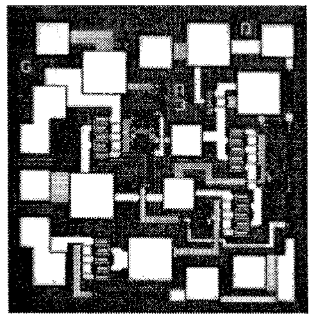

Fig. 3. Photograph of fabricated LPTAI (size: 0.85X0.92 mm^2)

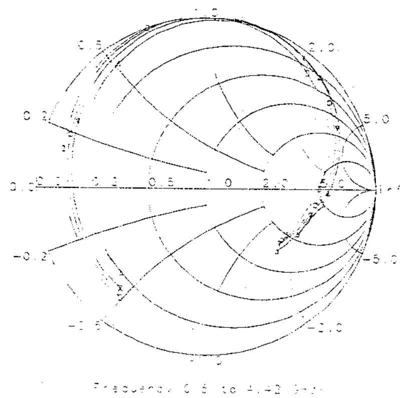

Fig. 4. Measured performances of LPTAI

	V_c [V]	P_{DC} [mW]	P_{DC}* ratio [%]	Calc. L [nH]
V_{gg}	-2.85	47.9	22.9	3.8
	-2.75	58.9	28.2	2.8
	-2.70	62.7	30.0	2.5
	-2.63	72.2	34.5	2.2
V_{dd}	8	66.0	31.6	2.4
	7	59.7	28.6	2.3
	6	54.7	26.2	2.1
	5	57.3	27.4	1.9

Table 1. Performances of LPTAI at each condition
* reference P_{DC}=209 mW [4] (=11V X 19mA)

APPLICATION TO VCO

The tunability of typical monolithic VCO is limited by the small range of capacitor variation at MMIC varactor. Thus, to get the wide tunability, we apply our LPTAI to fully monolithic, wide tunable VCO. The schematic and photograph of fabricated chip are shown in Fig. 5 and Fig. 6, respectively. The measured output characteristic of LPTAI-VCO is shown in Fig. 7. The measured characteristics of frequency and harmonics are shown in Fig. 8 and Fig. 9, respectively. The oscillation frequency is varied from 2.1 GHz to 3.0 GHz, that is, tuning ratio is 35 %. This amount is larger than measured one (12 %) of conventional varactor-type VCO which is implemented on the same chip and is larger than one (29 %) of the previous work [5]. The phase noise appears approximately -85 dBc/Hz at 1 MHz offset and it is not good because the bias drift and the increasing RF swing may degrade the phase noise characteristic.

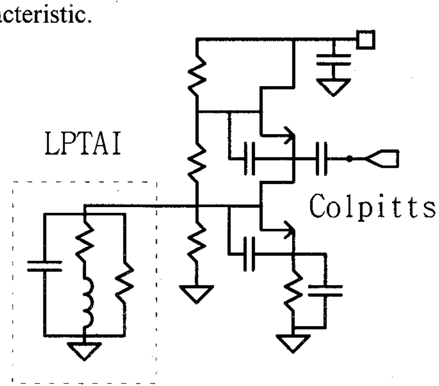

Fig. 5. The simplified schematic of active inductor VCO

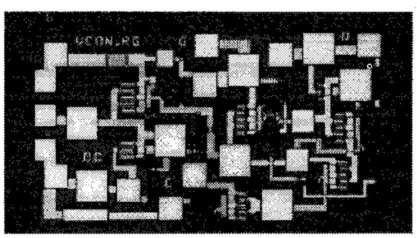

Fig. 6. Photograph of fabricated chip for active inductor VCO

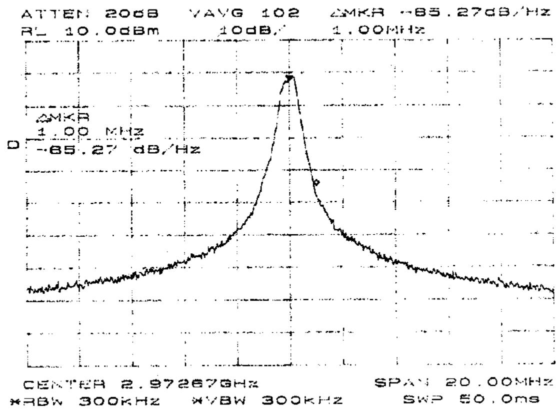

Fig. 7. Measured output power characteristic of active inductor VCO

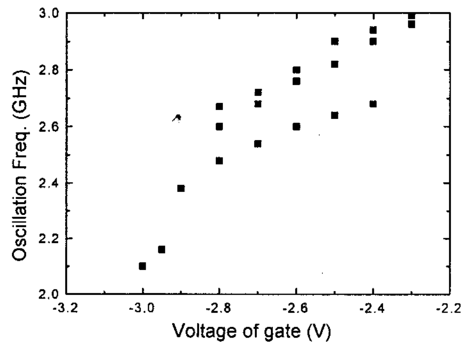

Fig. 8. Measured oscillation frequency characteristic of active inductor VCO

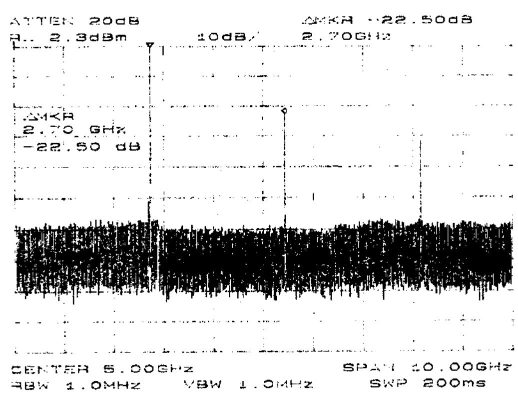

Fig. 9. Measured harmonics characteristic of active inductor VCO

APPLICATION TO BPF

Also, we make the fully monolithic, wide tunable BPF using LPTAI. Two shunts active L-C tuned circuits are passively coupled together with series capacitors in our 2nd-order filter. The fabricated chip and the characteristic of this filter are shown in Fig. 10 and Fig. 11, respectively. Fig. 11 shows good insertion loss and out-of-band rejections. By changing the tuning voltage (Vc), the center frequency can be controlled from 2.64 to 3.03 GHz, whose tuning ratio is 13.8 % and the DC power consumption of this filter is less than 115 mW.

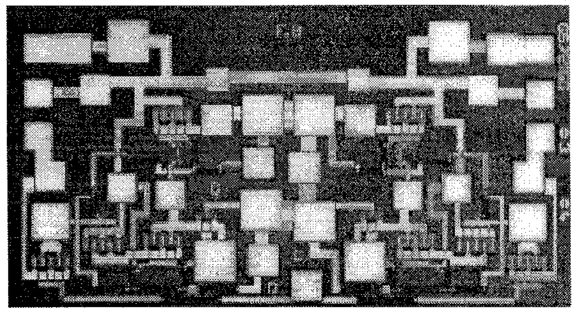

Fig. 10. Photograph of fabricated chip for active inductor 2nd-order BPF

CONCLUSIONS

We propose the novel tunable active inductor which consumes the low DC power that is at most 35 % of that of conventional one. Our novel topology uses common-gate cascode amplifier as non-inverting amp. and common-source one as inverting one. The new bias scheme using the parallel and the series bias resistors reduces the number of bias pins and stabilizes the bias, effectively. This novel low power tunable active inductor is applied to wideband monolithic VCO and wide tunable BPF.

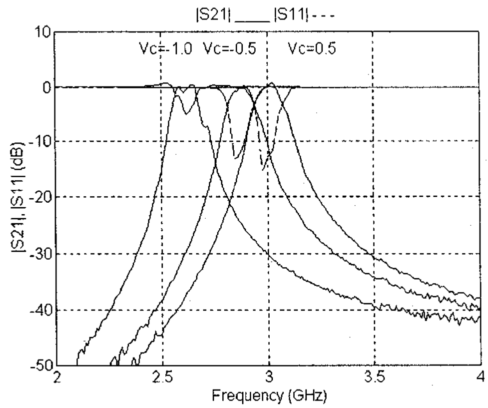

Fig. 11. Measured performances of 2nd-order active BPF

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