An Integrated Low Power Highly Linear 2.4-GHz CMOS Receiver Front-End Based on Current Amplification and Mixing

Ickjin Kwon, *Student Member, IEEE,* and Kwyro Lee, *Senior Member, IEEE*

***Abstract*—A low power 2.4-GHz complementary metal oxide semiconductor (CMOS) receiver front-end using highly linear mixer based on current amplification and mixing is reported. In the proposed mixer, linearity is greatly improved by using current mirror amplifier and trans-conductance linearization using multiple gated transistors. Single IF direct conversion receiver (DCR) architecture is used to achieve higher level of integration and to relax the problem of DCR. The fully integrated receiver front end is fabricated in 0.18-μm CMOS technology and IIP3 of -9 dBm with a gain of 32 dB and noise figure of 6.5 dB are obtained at 8.8 mW power consumption.**

***Index Terms*—Complementary metal oxide semiconductor (CMOS) receiver front-end, current amplifier, linearization, low power, single IF.**

I. Introduction

RECENTLY single chip low power complementary metal oxide semiconductor (CMOS) receivers operating in the 2.4-GHz band draw great attention due to the demand of longer battery life and lower cost solutions for applications as such IEEE802.15.4, Bluetooth, and IEEE 802.11b [1]. Among the various receiver architectures, the direct conversion receiver (DCR) is a viable candidate solution for low cost and low power. However, there are several problems in using DCR such as large dc offset, LO leakage, 1/f noise, and I/Q mismatch. To alleviate these problems, single IF DCR architecture has been proposed which combines the advantage of both the super-heterodyne and DCR architectures [2]. In a single IF DCR architecture, the input signal is down-converted to a first IF and then directly converted to baseband. With the use of relatively high IF, filter requirement for the image frequency can be relaxed and substantial filtering can greatly be achieved by the on chip image rejection filters.

The linearity performance requirement becomes more critical in modern RF communication systems. Especially, for the use at unlicensed 2.4-GHz ISM bands, a highly linear receiver is required for immunity to the various interferer signals of different standards. The linearity of the LNA and mixerare directly related to that of the receiver front end. The nonlinearity of the latter stages becomes more critical because the third-order intercept point (IP_3) of each stage is effectively scaled down by the total gain preceding that stage [3]. Usually, the nonlinearity of the receiver front-end is limited by that of the down-conversion mixer and, thus, a highly linear mixer is required. The linearity requirement of the mixer becomes more critical in single IF DCR because its gain in the preceding stages is larger than DCR. Since IIP3 is approximately proportional to the dc power consumption, it is a great challenge to achieve high linearity at low power [1].

In this letter, a highly linear low power CMOS receiver based on current amplification using current mirroring technique is proposed. This is based on single IF DCR and thus suitable for silicon integration. A receiver front end circuit operating at 2.4 GHz is designed and fabricated in 0.18-μm CMOS process. The circuit technique to improve the linearity of the receiver is explained in detail and the fabrication results are reported.

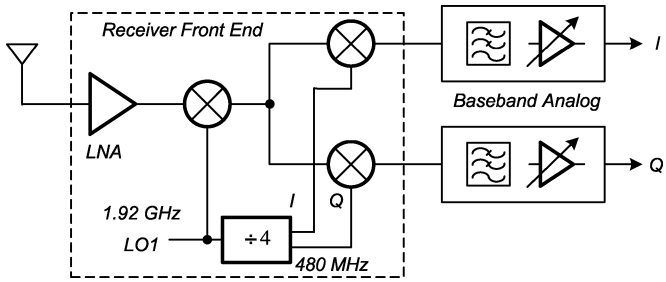

Fig. 1. Single IF DCR architecture using dual conversion to baseband with single local oscillator (LO).

II. Receiver Architecture

To achieve higher level of integration and to have immunity to dc offset, flicker noise and I/Q mismatch, single IF DCR architecture is used as shown in Fig. 1. The input signal at 2.4 GHz is amplified and then down-converted to an IF of 480 MHz. It is then directly down-converted to baseband by quadrature mixers. The quadrature LO signals required for the second mixer are generated by dividing the first LO signal by four. Both the dc offset caused by self mixing and I/Q mismatch are greatly reduced since the down-conversion of the signal in quadrature phase to baseband occurs at much lower LO frequency. Furthermore, the flicker noise at the output of the second mixer is less serious because of larger signal level.

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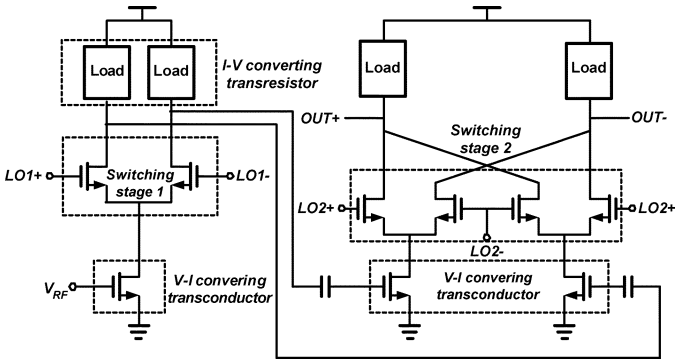

Fig. 2. Conventional mixer with two switching stages.

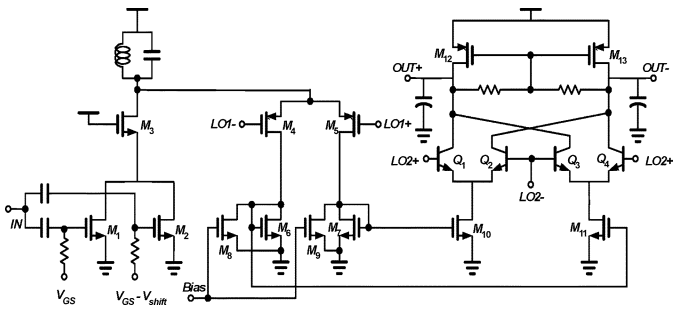

Fig. 3. Proposed highly linear mixer using current mirror amplifier between two switching stages and transconductance linearization using MGTR.

Selection of the IF frequency is an important issue in single IF DCR architecture. It is basically a compromise between the amount of the image rejection requirement and the I/Q mismatch of the second mixer. A good receiver should have immunity to the out of band interferers as well as in-band interferers. We chose the first down conversion of the receiver at an IF of 480 MHz, which, with low-side injection, leads image signal located in the range of 1.44$\sim$1.52 GHz. Following the analysis in [4], we found that this lower side band heterodyne system has strong immunity against various interference. This relatively high IF allows us to obtain on chip image rejection of as large as 32 dB by the input matching circuit and LC tuned load of the LNA and mixer.

III. Single IF CMOS Receiver Architecture Based on Current Amplification and Mixing

Fig. 2 shows a schematic diagram of a conventional mixer circuit. It consists of a cascade of two mixers, where each mixer is composed of a input voltage-to-current (V–I) converting transconductor, a Gilbert cell type switches, and a current-to-voltage (I–V) converting transresistor. This mixer operates as follows. The input voltage signal is converted to current by the V–I converter, which is steered by the mixer switch. Then the mixed current is down-converted to voltage signal by the I–V converter in the first mixer output. The down-converted IF voltage signal is then re-converted to current signal by V–I converter in the second mixer input, which is steered again by the second mixer switch and finally converted to voltage signal. This architecture has the advantage of large gain. However, its linearity is not good mainly because of the V–I converter nonlinearity, which becomes more serious especially at lower bias current. Therefore, we propose to replace I–V and V–I converter between the first and second mixer by current amplifier based on current mirror [5]. This is shown in Fig. 3. Because current mirror based current amplifier is highly linear in regardless of bias current, we expect much better linearity.

The gain of the current mirror amplifier can be easily set through appropriate scaling factor (N) in current mirror amplifier. The conversion gain of the mixer shown in Fig. 3 can be calculated as

$$\text{Gain} = g_{m1}\frac{2}{\pi}N\frac{2}{\pi}R_L \tag{1}$$

where g_{m1} is the input stage transconductance, R_L is the effective load resistance, and N is the scaling ratio of the two current mirrors. The use of current mirror, however, has one drawback, i.e., its operating frequency is limited approximately by f_{T}/N, where f_{T} is the transistor cut-off frequency. Therefore we cannot increase the gain much, especially at RF frequency. We do not, however, have to worry about this in the single IF architecture in Fig. 3 because current amplification is done at IF frequency.

In the single IF structure shown in Fig. 3, nonlinearity is limited by the RF input V–I converter. In this letter, we adopt multiple gated transistor (MGTR) to linearize it as proposed in [6]. The other nonlinearity distortion is originated from the nonlinearity of the switching pair. The optimum value of bias current and LO amplitude are determined for high IIP_3 of the switching pair following the previous approach [7]. Note, further that the optimum bias point for high linearity and low noise figure performance is different between transconductor and the switching stage. Using the folded structure, the bias current is separated between them and the optimum bias condition for each stage is obtained independently. In Fig. 3, RF open load such as LC load or RF choke is used to keep the current signal between input transconductor and first switching, which also functions as image rejection filter.

IV. CMOS Circuit Design Detail

In the receiver front-end circuit, cascode LNA with inductive source degeneration is used for best noise performance at low power consumption and a noise figure of 1.7 dB is obtained at the bias current of 1.5 mA by the circuit simulation. In this letter, we chose current gain of N =4, which provides enough gain and bandwidth at IF frequency of 480 MHz. One problem of the current mirrors is that the dc bias current should also be scaled. Here, we propose to adopt bypass transistor m_8 and m_9 for removing dc current from the current mirrors as shown in Fig. 3. In Fig. 3, the small signal current gain N is determined by the ratio of $\mathrm{M}_{10}/\mathrm{M}_7$. If we do not use M_9, the bias current at the second mixer should be larger by N times than that of the first mixer. In addition, this also allows us a freedom in separate bias optimization for the input transconductor and mixer switch circuits.

The flicker noise and dc offset are critical issues of the direct conversion receiver. Because of orders of magnitude smaller 1/f noise and better device matching characteristics of bipolar junction transistor (BJT) compared with metal oxide semiconductor field effect transistor (MOSFET), the parasitic vertical

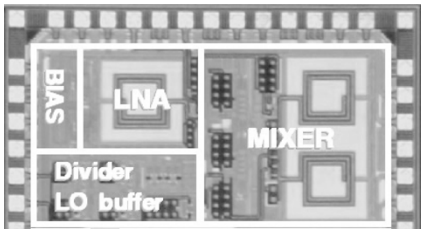

Fig. 4. Chip microphotograph of the receiver front-end.

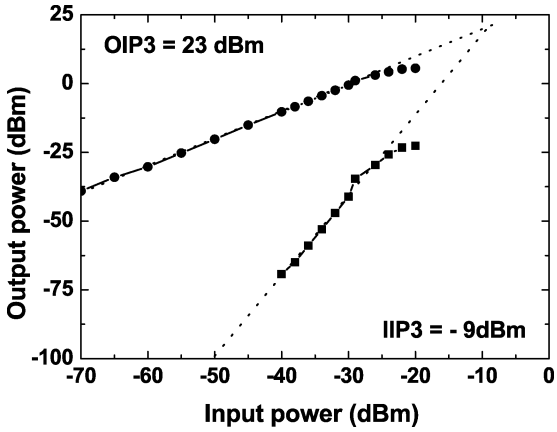

Fig. 5. Measured IIP3 of the receiver front-end.

NPN BJT available from triple well CMOS process is used for second down conversion switching stage as shown in Fig. 3 [8]. The frequency limitation of vertical NPN is high enough for the use at second LO of 480 MHz.

The divide-by-four circuit for quadrature 480 MHz LO signal generation is realized by cascading two stages of divided-by-two circuit. A divide-by-two circuit consisting of two latches in a negative feedback loop is used to high speed and low power dissipation. Each latch is implemented using a current steering topology, consisting of a differential pair and a regenerative pair [3].

V. Experimental Results

The receiver front-end has been fabricated in 0.18 μm 1-poly six-metal CMOS process. Fig. 4 shows the microphoto-graph of the receiver front-end. The size of front-end including LNA, mixer, dividers, LO buffers, and bias circuit is 1.3 mm $\times$ 0.65 mm. The measured maximum gain is 32 dB and measured noise figure is 6.5 dB at 300 KHz. The proposed mixer has very small 1/f noise characteristics due to the use of vertical NPN BJT switching pair for second down-conversion. An image rejection of 32 dB is achieved by on-chip circuitry.

The measured third-order nonlinearity of the receiver front-end is shown in Fig. 5. For IIP3 measurements, two tones at 2.4015 GHz and 2.4025 GHz are applied. An IIP3 of about -9 dBm and a gain of 32 dB are measured at 8.8 mW power consumption as shown in Fig. 5. The measured performances including linearity figures-of-merit (FOM) defined as $10\log(OIP3(\mathrm{mW})/P_{dc}(\mathrm{mW}))$ for this and other reported mixers are compared in Table I. In the proposed mixer, linearity is greatly improved by using current mirror amplifier and transconductance linearization using multiple gated transistors without additional power consumption. Its linearity FOM is higher than other reported mixers as shown in Table I, although it consists of dual conversion switching stages. The measurement results of the cascaded receiver front-end are summarized in Table II.

TABLE I
Performance Comparison of the Proposed Dual Conversion Mixer With Other Reported Mixers

Reference	*P.B.Khannur, RFIC 02*	*C.G.Tan, RFIC 03*	*F. Beffa, RFIC 02*	*V. Vidojkovic, RFIC 04*	***This work***
Frequency	2.4 GHz	2.4 GHz	2 GHz	2.4 GHz	**2.4 GHz**
Noise Figure	20 dB	16 dB	13.9 dB	13.9 dB	**11 dB**
Conversion Gain	23.7 dB	13.4 dB	21.4 dB	11.9 dB	**19 dB**
OIP3	16.7 dBm	12.4 dBm	3.4 dBm	8.9 dBm	**22 dBm**
Power Dissipation	31.2 mW	7.2 mW	6.48 mW	3.2 mW	**4.25 mW**
linearity FOM	1.8	3.8	-4.7	3.8	**15.7**
Technology	0.35 μm CMOS	0.18 μm CMOS	0.18 μm CMOS	0.18 μm CMOS	**0.18 μm CMOS**

TABLE II
Measured Performance Summary of the Receiver Front-End

Noise figure	6.5 dB
Gain	32 dB
IIP3	- 9 dBm
IIP2	30 dBm
On chip image rejection	32 dB
Power consumption	8.8 mW
Supply voltage	1.8 V
Technology	1P-6M, 0.18 μm CMOS

VI. Conclusion

A 2.4-GHz low power CMOS receiver front-end using highly linear mixer based on current amplification and mixing is reported. In the proposed mixer, linearity is improved by using current amplifier and transconductance linearization using multiple gated transistors. This is based on single IF DCR and thus suitable for silicon integration. The fully integrated 2.4 GHz receiver front-end is fabricated in 0.18 μm CMOS technology and IIP3 of -9 dBm with a gain of 32 dB and noise figure of 6.5 dB are obtained at 8.8 mW power consumption.

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