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Highly improved photo-induced bias stability of sandwiched triple layer structure in sol-gel processed fluorine-doped indium zinc oxide thin film transistor

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In order to improve the reliability of TFT, an Al_2O_3 insulating layer is inserted between active fluorine doped indium zinc oxide (IZO:F) thin films to form a sandwiched triple layer. All the thin films were fabricated via low-cost sol-gel process. Due to its large energy bandgap and high bonding energy with oxygen atoms, the Al_2O_3 layer acts as a photo-induced positive charge blocking layer that effectively blocks the migration of both holes and V_o^{2+} toward the interface between the gate insulator and the semiconductor. The inserted Al_2O_3 triple layer exhibits a noticeably low turn on voltage shift of −0.7 V under NBIS as well as the good TFT performance with a mobility of 10.9 $cm^2/V{\cdot}s$. We anticipate that this approach can be used to solve the stability issues such as NBIS, which is caused by inescapable oxygen vacancies. [http://dx.doi.org/10.1063/1.4944833]

Thin film transistors (TFTs) are important device elements that play a key role in driving modern sophisticated flat panel displays such as active-matrix liquid crystal displays (AMLCDs) and organic light-emitting diodes (AMOLEDs).[1,2] Since the 1980s, due to its process simplicity and cost-effectiveness, hydrogenated amorphous silicon (a-Si:H) have been the most widely-implemented active channel for the display TFT backplane. Currently, traditional a-Si:H based TFTs are being replaced by low temperature poly crystalline silicon (LTPS) and amorphous oxide semiconductor (AOS) because these emerging materials are capable of providing better device performance in terms of mobility. In particular, AOS TFTs have gained a great deal of attention owing to their high mobility, ease of large-area fabrication, cost-effectiveness, and optical transparency.[3,4]

Despite these promising features, however, AOS TFTs have a serious problem, namely stress-induced instability.[5] The major stress sources that exist inevitably under device operation conditions include prolonged application of negative gate bias (NBS), light illumination (NBIS), and elevated temperature (NBTIS).[6–8] In particular, NBIS and NBTIS provoke severe negative shifts of the turn-on voltage (V_{on}) that can cause malfunctioning of the TFT device; therefore, these are important technical issues that need to be resolved. Although the underlying origin of NBIS and NBTIS remains unclear, these phenomena are believed to be closely related to the oxygen vacancies (V_o) that intrinsically exist in typical AOS layers. In brief, a negative shift of V_{on} arises from photo-generated positive charges – ionized oxygen vacancies (V_o^{2+}) and other holes– that are accumulated or trapped at the gate-AOS interface.[9,10] So far, in an effort to improve the negative instabilities of typical AOS TFTs, numerous studies have been conducted to reduce the level of V_o. Major examples of the reported strategies include introducing a high oxygen-pressure annealing process,[11,12] implementing a UV-ozone annealing process,[13] and doping of a hetero-element with high bonding energy to oxygen.[14,15] As another approach, Oh *et al.*,[16] reported a novel method to effectively improve NBIS with only a slight expense of mobility by inserting a positive-charge-barrier in vacuum processed ZnO TFTs.

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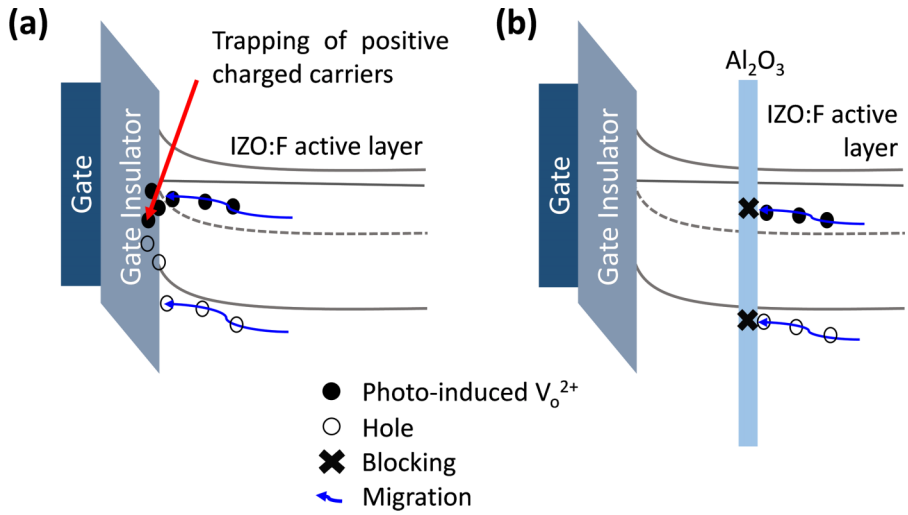

FIG. 1. Schematic illustrations of energy band diagram for (a) normal and (b) Al_2O_3-inserted structure.

In this study, we expand this strategy to the sol-gel processed, fluorine-doped indium zinc oxide (IZO:F) TFT. Doped-fluorine plays roles in generation of free electrons and reduction of V_O showing better electrical performance and stability characteristics than those of conventional IZO TFTs.[17,18] In order to further enhance the stability against illumination stress, solution-processed Al_2O_3 layer is introduced as a positive-charge-barrier. Figure 1 shows the effect of the blocking layer in a band structure. As can be seen in the diagram, when there is no blocking layer, the positively charged oxygen vacancies and hole due to photo generation in the channel bulk are trapped eventually after they are drawn towards the gate insulator layer by the applied gate bias. However, with the insertion of Al_2O_3 layer, the migration of positively charged oxygen vacancy (V_O^{2+}) from the IZO:F layer is stagnated at the Al_2O_3 layer because the Al-O bonding energy (~512 kJ/mol) is higher than that of In-O (~184 kJ/mol) and Zn-O (~ 159 kJ/mol). Also, the larger energy band gap of Al_2O_3 (8.4 eV) than the InZnO (3.1 eV)[19] leads to a high valence band offset acting as an effective hole barrier. Therefore, the all solution-processed, positive-charge-barrier inserted IZO:F (IZO:F-SPB) TFT features a high field effect mobility and notably stable characteristics against NBS, NBIS and NBTIS.

Figures 2(a) and 2(b) show the structure of the reference device (IZO:F) and of IZO:F-SPB (with Al_2O_3 SPB insertion layer), respectively. For the IZO:F film, the precursor solution is prepared by dissolving 0.15 M of indium fluorite trihydrate ($InF_3 \cdot 3H_2O$,Aldrich), and zinc fluoride (ZnF_2, Aldrich) in water and the composition is chosen as 1:1. To check the effect of Al_2O_3 thickness, we fabricated two different devices with varying the concentration of Al_2O_3 precursor

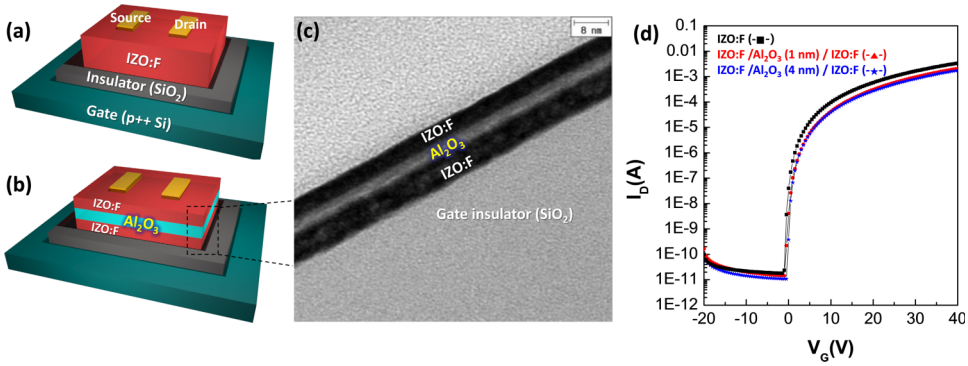

FIG. 2. Schematic structure of (a) normal and (b) Al_2O_3-inserted TFTs. (c) A TEM image of Al_2O_3-inserted TFT. (d) Transfer characteristics of normal structure, Al_2O_3 1 nm-inserted structure, and Al_2O_3 4 nm-inserted structure.

TABLE I. Electrical performance of IZO:F and Al_2O_3 barrier layer-inserted TFTs.

	μ $(cm^2/V \cdot s)$	$I_{on/off}$	$S.S$ (V/dec)
IZO:F	18.6	$\sim 10^8$	0.42
IZO:F-SPB1	12.7	$\sim 10^8$	0.50
IZO:F-SPB4	10.9	$\sim 10^8$	0.44

solution to 0.01M and 0.1M of aluminum nitrate nonahydrate [$Al(NO_3)_3 \cdot 9H_2O$, Aldrich] in water. The precursor solutions are spin coated at 5000 rpm for 30s onto a p-type wafer, which has 100 nm of SiO_2 layer on top. In the case of the active sandwiched structure, each layer was annealed for 1 h on a hotplate, and total annealing time is 3 h. After annealing, 100 nm of Al source/drain electrodes are deposited by e-beam evaporation through a shadow mask that defines the channel width (1000 μm) and length (100 μm). Thicknesses of the Al_2O_3 SPB layers are 1 and 4 nm, respectively and these devices are denoted IZO:F-SPB1 and IZO:F-SPB4. Figure 2(c) provides a cross-sectional

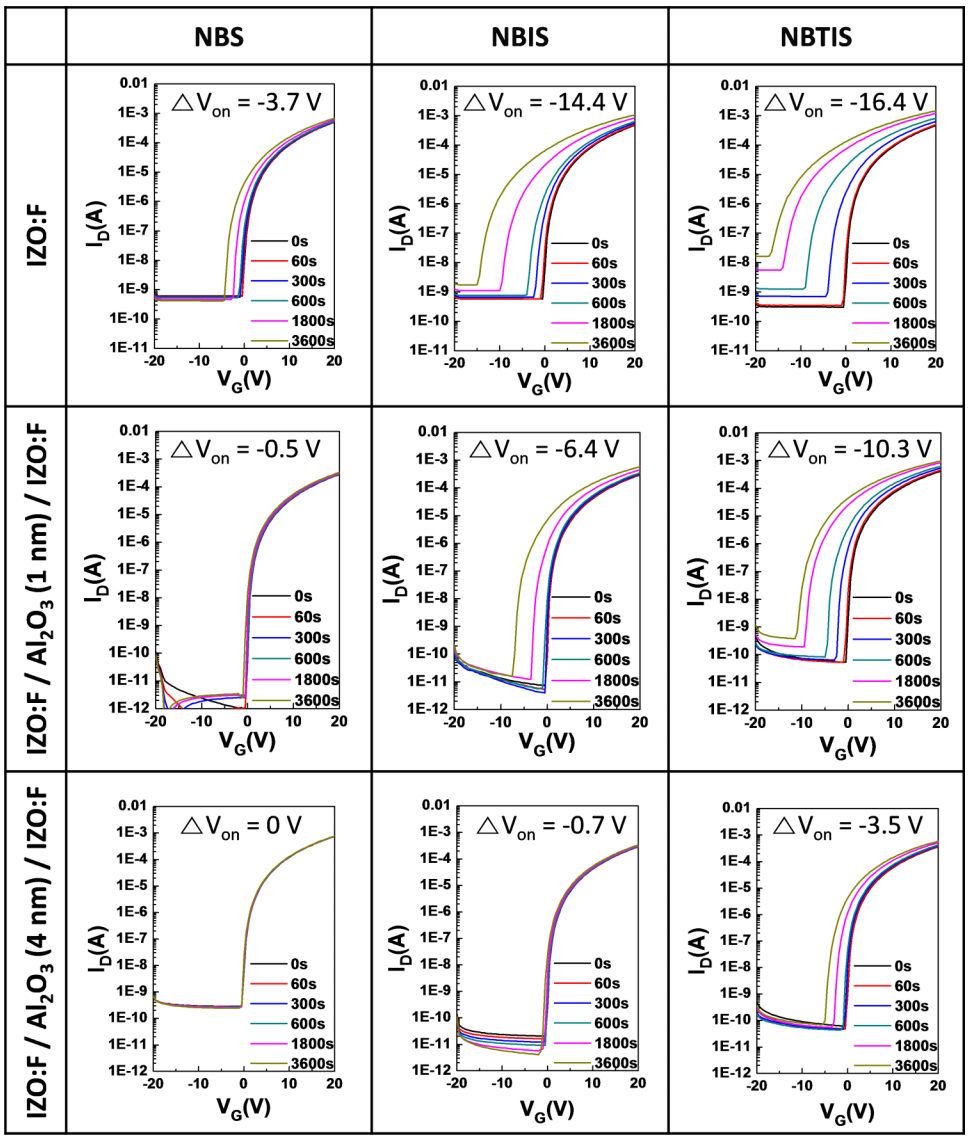

FIG. 3. Gate bias stability of IZO:F, IZO:F/Al_2O_3 (1 nm) M/IZO:F and IZO:F/Al_2O_3 (4 nm)/IZO:F TFTs of NBS, NBIS and NBTIS.

TABLE II. The bias stability of IZO:F, IZO:F/Al_2O_3 (1 nm) M/IZO:F and IZO:F/Al_2O_3 (4 nm)/IZO:F TFTs.

	NBS (ΔV_{on})	*NBIS* (ΔV_{on})	*NBTIS* (ΔV_{on})
IZO:F	−3.7 V	−14.4 V	−16.4 V
IZO:F-SPB1	−0.5 V	−6.4 V	−10.3 V
IZO:F-SPB4	~0 V	−0.7 V	−3.5 V

TEM image of the IZO:F-SPB4 device; this image confirms the structure of the Al_2O_3-inserted IZO:F channel. The electrical properties of the devices were characterized using transfer curves (Figure 2(d) and Table I). It is noteworthy that all TFT devices are turned on at 0 V and show excellent transfer characteristics. However, with increasing the thickness of the Al_2O_3 SPB layer, channel electrons are difficult to be collected to the drain top electrode leading to the decrease in mobility.

The most important issue on AOS TFTs is poor stabilities against bias, light-illumination, and thermal stress. To evaluate stability of IZO:F-SPB TFTs, we performed a series of stability tests with the following conditions: (i) NBS (V_{GS} = −20 V, V_{DS} = 0 V), (ii) NBIS (V_{GS} = −20 V, V_{DS} = 0 V, 0.3 mW/cm^2), (iii) NBTIS (V_{GS} = −20 V, V_{DS} = 0 V, 0.3 mW/cm^2, 60°C). All tests were carried out under N_2 atmosphere; test results are summarized in Figure 3 and Table II.

For the reference IZO:F device, −3.7 V of V_{on} shift (ΔV_{on}) is observed when negative bias is applied to the device (NBS). With the illumination stress, photo-generated V_O^{2+} and holes are trapped at the semiconductor/gate dielectric interface resulting in the increase in ΔV_{on} to −14.4 V. For NBTIS of the IZO:F TFT, the thermal stress accelerates the generation of positive charges and activates the migration of those charges leading to the further increase in ΔV_{on} up to −16.4 V. For the IZO:F-SPB1 TFT, V_{on} shifts of −0.5 V, −6.4 V and −10.3 V are observed under NBS, NBIS and NBTIS condition, respectively. This result is due to the insulating Al_2O_3 layer suppressing the migration of V_o^{2+} and holes in the active layer. The effect of Al_2O_3 insertion layer becomes more obvious as the thickness increases. In the case of the IZO:F-SPB4, V_{on} barely shifts under NBS condition and even for NBIS and NBTIS, ΔV_{on} is −0.7 V and −3.5 V, respectively, showing that the Al_2O_3 insertion layer is working properly according to the mechanism proposed in Figure 1.

Since all the transfer curves show parallel shifts without deformation, instabilities under stress conditions are originated from charge trapping mechanism. In such a case, the stress time dependence of the ΔV_{on} has to be in agreement with a stretched exponential equation, as follows.[20,21]

$$\Delta V_{on}(t) = V_0 \left\{ 1 - exp\left[-\left(\frac{t}{\tau} \right)^{\beta} \right] \right\} \quad (1)$$

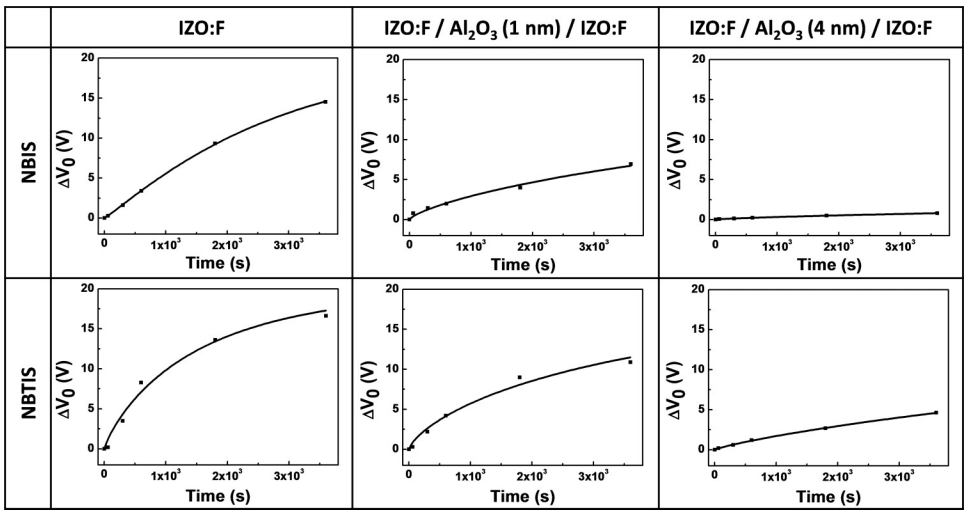

FIG. 4. ΔV_{on} versus stress time plots of the oxide TFTs under NBIS and NBTIS.

TABLE III. Relaxation Time, τ, and stretched-exponential exponent, β, for fabricated TFTs.

	NBIS		*NBTIS*	
	T (s)	B	T (s)	B
IZO:F	2810	1.08	1589	0.84
IZO:F-SPB1	11936	0.74	4461	0.83
IZO:F-SPB4	304979	0.71	17747	0.72

where $\Delta V_{on}(t)$ is the V_{on} shift, $V_0 = V_g - V_{on}$, β is the stretched-exponential exponent, τ represents the characteristic trapping time of positive charges, and t is the stress duration time.

Figure 4 shows the results of the V_{th} values as the thickness of the insulating Al_2O_3 layer was varied. In Table III, the IZO:F-SPB TFTs have carrier trapping time (τ) longer than that of the IZO:F-TFTs. Further, the IZO:F-SPB4 TFTs have carrier trapping time (τ) longer than that of IZO:F-SPB1 TFTs. The IZO:F-SPB1 TFT's τ values are 1 x 10^5 s (NBIS) and 4 x 10^4 s (NBTIS), while the IZO:F-SPB4 TFT's τ values are 3 x 10^6 s (NBIS) and 1 x 10^5 s (NBTIS). The τ value for IZO:F-SPB4 is longer than that of IZO:F-SPB1 indicating that for thicker Al_2O_3 layer, the positive charges take longer time to be trapped by defects at the semiconductor/gate dielectric interface. The trapping time also includes the time for charges to be drawn from the bulk of the channel to the interface by gate bias.[22,23] Therefore, the longer trapping time can be attributed to effective blockage of positive charge by Al_2O_3 layer. Additional thermal stress leads to the decrease in τ values due to the rapid migration of positive charges.[24]

In this work, the effect of Al_2O_3 insertion layer on stabilities of the IZO:F TFT against photo-induced negative bias stress was studied. Even though it contained the insulating Al_2O_3 layer sandwiched in channel, high mobility around 10 cm^2/Vs is achieved due to superior property of IZO:F semiconductor as TFT channel. Al_2O_3 layer acted as a blocking layer of positive charges such as V_o and holes and effectively improved stabilities against illumination and thermal stresses. The reference IZO:F TFT yielded an NBS of $V_{on} = -3.7$ V, an NBIS of $V_{on} = -14.4$ V, and an NBTIS of $V_{on} = -16.4$ V, while with the addition of the blocking layer yielded respective values of $V_{on} = 0$ V, $V_{on} = -0.7$ V, and $V_{on} = -3.5$ V. Using the stretched exponential model, it was also found that the charge carrier trapping time increased because the migration of positive charges toward the semiconductor/gate dielectric interface is effectively interrupted. In conclusion, the Al_2O_3 layer proved that it can be a decent solution for the light vulnerability of TFT devices considering that oxygen vacancies cannot be removed technically from oxide semiconductors.

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