A Transparent Logic Circuit for RFID Tag in a-IGZO TFT Technology

Byung-Do Yang, Jae-Mun Oh, Hyeong-Ju Kang, Sang-Hee Park, Chi-Sun Hwang, Min Ki Ryu, and Jae-Eun Pi

This paper proposes a transparent logic circuit for radio frequency identification (RFID) tags in amorphous indium-gallium-zinc-oxide (a-IGZO) thin-film transistor (TFT) technology. The RFID logic circuit generates 16-bit code programmed in read-only memory. All circuits are implemented in a pseudo-CMOS logic style using transparent a-IGZO TFTs. The transmittance degradation due to the transparent RFID logic chip is 2.5% to 8% in a 300-nm to 800-nm wavelength. The RFID logic chip generates Manchester-encoded 16-bit data with a 3.2-kHz clock frequency and consumes 170 μW at V_{DD}=6 V. It employs 222 transistors and occupies a chip area of 5.85 mm^2.

Keywords: a-IGZO, RFID, thin-film transistor, transparent.

I. Introduction

Radio frequency identification (RFID) technology is a key component of the ubiquitous computing era. The RFID system gives automation and physical flexibility in a wide variety of applications, such as inventory control systems and checkout operations, by enabling automatic detection and identification through radio waves. To broaden the application area of the RFID system, RFID tags have been fabricated with not only the conventional silicon VLSI process but also a diversity of thin-film transistor (TFT) materials [1]-[6].

Recently, transparent antennas, rectifiers, and oscillators for transparent RFID tags were developed [1]-[3]. The merit of invisibility can extend the RFID application area to mirrors, clothing, books, and military devices. Including a transparent antenna, rectifier, and oscillator in the front end of the RFID tag was previously proposed [1]. However, the full digital logic for the transparent RFID tag has not yet been developed. In this paper, we propose a transparent digital logic circuit for the RFID tag.

TFTs have been manufactured using hydrogenated amorphous silicon (a-Si:H), low-temperature polycrystalline silicon (LTPS), and organic material as the active layer. The a-Si:H TFTs have the advantage for integration on a large glass substrate for mass production, owing to long-range uniformity and lower manufacturing cost [7]. However, the a-Si:H TFT has a low field effect mobility (~1 cm^2/V·s), so it is difficult to form high-speed circuits, such as digital logic blocks. The organic TFT (OTFT) has the complementary-MOS (CMOS) structure, but it is difficult to operate digital circuits due to its low field effect mobility [8]. Meanwhile, the LTPS TFTs, which can form CMOS devices, have a relatively high field

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effect mobility and desirable current operation ability. However, the laser annealing process to form a crystal grain is not completely developed for large glass substrates [9]. In addition, an inevitable non-uniformity problem is a significant consideration in attempting to ensure successful circuit operation [10]. On the other hand, oxide TFTs have the same advantages as a-Si:H TFTs. Oxide TFTs show even higher field effect mobility (>10 $cm^2/V{\cdot}s$) than a-Si:H TFTS and desirable current operation ability for high-speed digital circuits [11]. Therefore, the oxide TFT is the best candidate for integrated digital circuits. Additionally, its active layer shows transparent characteristics owing to the high bandgap energy [12], so it is suitable for various transparent products.

In this paper, we propose a transparent digital logic circuit for the RFID tag composed of amorphous indium-gallium-zinc-oxide (a-IGZO) TFTs. The RFID logic circuit is simulated using the fitted model parameter of a-IGZO TFTs and is realized on glass substrates at ETRI, Daejeon, Republic of Korea. The transparent RFID logic circuit is designed to combine the previous work on transparent antennas and rectifiers [1].

The rest of the paper is organized as follows. Section II describes the proposed transparent RFID logic circuit. Section III shows the measurement results of the fabricated chip. Finally, the conclusion is drawn in section IV.

II. Transparent RFID Logic Circuit

1. Transparent a-IGZO TFT Technology

Figure 1(a) shows the cross-sectional structure of the fabricated top-gate oxide TFT. The fabrication process is conducted as follows. A buffer layer (15-nm SiO_2) is deposited on a glass substrate. First, a transparent indium-tin-oxide (ITO) is deposited and patterned as the source/drain (S/D) electrodes. Then, an active layer (20-nm a-IGZO) and a protection layer (10-nm Al_2O_3) are deposited by sputtering. After the patterning of the active and protection layers, a gate insulator (GI) is deposited. Then, metal contact holes are formed for the connection between the S/D and the gate. On the gate insulator, a 150-nm gate electrode (ITO) is deposited and patterned.

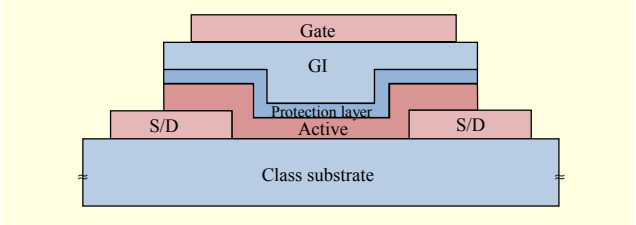


Fig. 1. Cross-sectional structure of fabricated oxide TFTs.

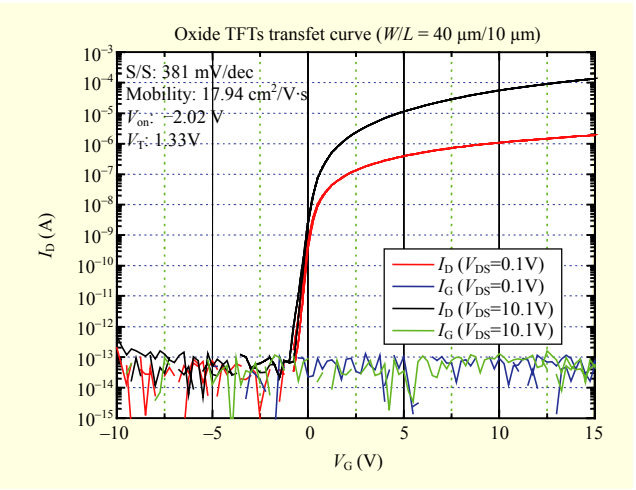


Fig. 2. Transfer curves of fabricated oxide TFTs.

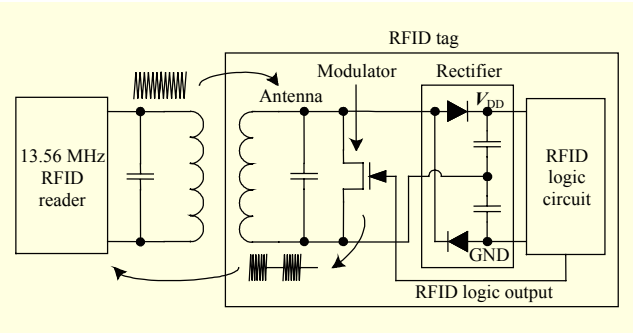


Fig. 3. RFID system.

Figure 2 shows the transfer characteristics of a-IGZO TFTs for extracting simulation model parameters. The on/off ratio is about 10^7 at V_{DS} = 0.1 V, and the field effect mobility is 17.94 $cm^2/V{\cdot}s$. The threshold voltage (V_T) and on-voltage (V_{ON}) are 1.33 V and –2.02 V, respectively. The gate capacitance is about 0.95 $fF/\mu m^2$. The measured model parameters are extracted to an HSPICE model for the RFID logic circuit simulations.

2. RFID Tag Architecture

Figure 3 shows the RFID system, including a 13.56-MHz RFID reader and an RFID tag. The RFID tag consists of an antenna, a modulator (a modulation transistor), a rectifier, and an RFID logic circuit. The antenna receives 13.56-MHz RF signals. The rectifier generates the supply voltage (V_{DD}) from the RF signals. The RFID logic circuit makes the Manchester-encoded RFID tag data. The modulation transistor modulates the amplitude of the RF signals on the antenna to send the RFID tag data to the RFID reader.

In [1], the transparent antenna and rectifier were implemented

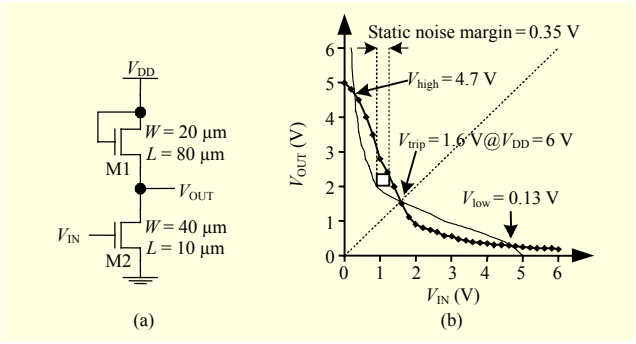


Fig. 4. (a) Schematic and (b) measured transfer characteristic of inverter.

for the transparent RFID tag. In this paper, the transparent RFID logic circuit is implemented in the transparent a-IGZO TFT technology. The transparent RFID tag can be implemented by combining the transparent antenna and rectifier [1] and the proposed transparent RFID logic circuit.

3. Logic Gates

All logic circuits are designed in a pseudo-CMOS logic style [13], as shown in Fig. 4(a), because all fabricated transparent oxide TFTs are N-type MOS (NMOS) transistors. Each logic gate consists of a diode-connected NMOS transistor for pull-up and several NMOS transistors for pull-down. Figures 4(a) and 4(b) show the schematic and measured transfer characteristic of an inverter, respectively. The W/L ratio of the pull-up transistor (W/L_1=20 μm/80 μm) to the pull-down transistor (W/L_2=40 μm/10 μm) is selected to be 1/16 for wide output voltage and low static current under 1 μA. The measured input-output characteristic of the inverter shows the stable logic low and high values (V_{low}=0.13 V and V_{high}=4.7 V), the trip voltage (V_{trip}=1.6 V), and the static noise margin (V_{SNM}=0.35 V). The static noise margin is defined as the size of the largest square between the input-output characteristic and its mirror characteristic [4]. The static noise margin is important to design the circuits including such memory elements as the cross coupled latch made of two NAND gates in the data flip-flop (DFF), as shown in Fig. 5(a).

Figures 5(a) and 5(b) show a DFF and an XOR gate for circuit examples, respectively. All circuits are the static logic gates in a pseudo-CMOS logic style. No dynamic circuit is used for the stable operation. The number of series-connected pull-down NMOS transistors is limited to three to keep enough current driving capability in the pull-down transistors. In all circuits, as shown in Fig. 4(a), the sizes of W/L for the pull-up transistors and pull-down transistors are 20 μm/80 μm and 40 μm/10 μm, respectively. The DFF is made of two or three input NAND gates (NAND-2 or NAND-3). The XOR gate

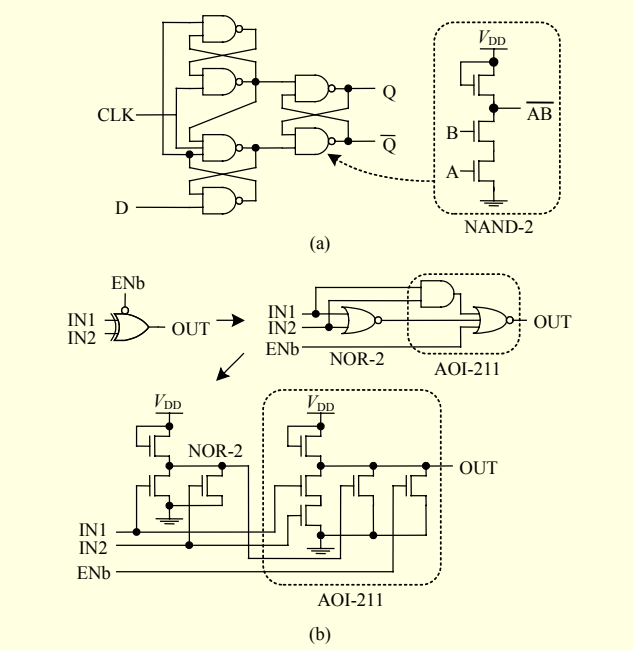


Fig. 5. Pseudo-CMOS logic examples: (a) DFF and (b) XOR gate with an enable pin.

with an enable pin is composed of a NOR gate and an AOI-211 gate (and-or-inverter with two, one, and one inputs), as shown in Fig. 5(b).

The parameters of a-IGZO TFTs are changed due to the fabrication process variations. The parameter drift of a-IGZO TFTs causes delay variations of the logic gate, resulting in a change in the operating frequency of the RFID tag. However, the parameter drift of a-IGZO TFTs does not affect the robustness of the logic gate because the pull-up transistor and the pull-down transistor in the pseudo-CMOS logic are made of the same NMOS transistors. The trip voltage and the static noise margin of the pseudo-CMOS logic are not affected by the parameter changes.

4. RFID Logic Circuit

Figure 6 shows the RFID logic circuit for 16-bit code generation. The clock generator makes three clock signals (CLK #1 to CLK #3) with 120-degree phase differences. The 5-bit counter generates a 4-bit address (ADD<4:1>) to read the 16-bit read-only memory (ROM) data sequentially. The most significant bit output of the 5-bit counter (ADD<5>) is used for the output enable signal in the Manchester encoder. Two 2-to-4 decoders select a word line (WL) and a bit line (BL) according to the address (ADD<4:1>). The ROM data is sequentially accessed out, and it is encoded to the RFID logic output in the Manchester encoder.

The clock generator shown in Fig. 7 is based on a ring

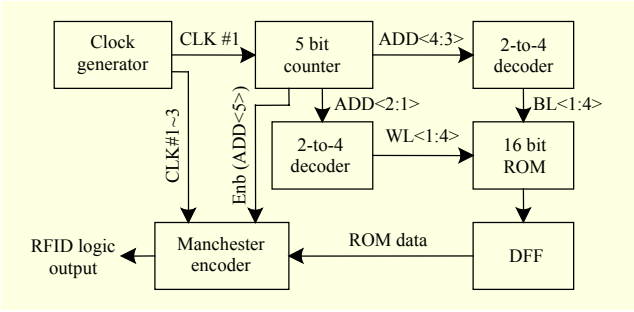


Fig. 6. Block diagram of RFID logic circuit for 16-bit code generation.

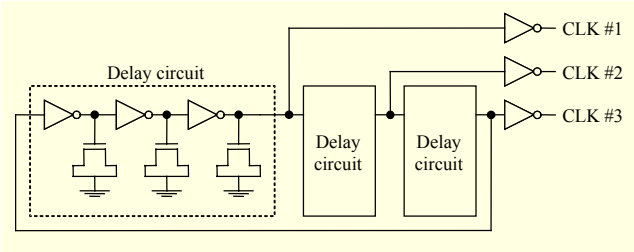
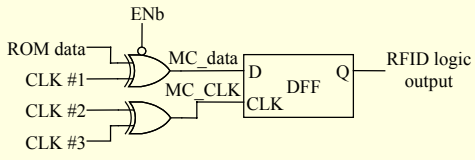


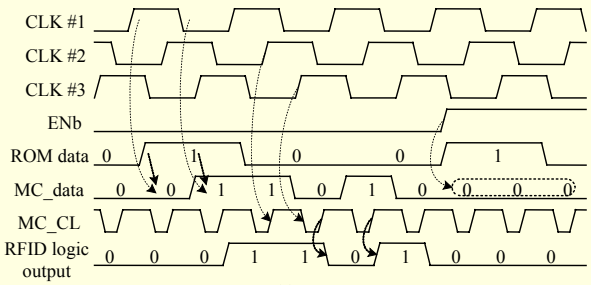
Fig. 7. Clock generator.

ROM data	Manchester encoding	RFID logic output	
		EN=0	EN=1
0	10	00	10
1	01	00	01

(a)



(b)



(c)

Fig. 8. Manchester encoder (a) RFID logic output, (b) circuit, and (c) operation.

oscillator. The ring oscillator consists of nine inverters for low area and low power consumption. Instead, the NMOS capacitors (W/L=40 μm/100 μm) are added to each output of the inverters, to set the proper clock frequency for the Manchester encoder, as shown in Fig. 8, and the 16-bit code generation circuit, as shown in Fig. 9. Three clock signals (CLK #1 to CLK #3) with 120-degree phase differences are used for the Manchester encoding operation shown in Fig. 8(c).

In wireless RFID communication, three types of RFID logic outputs are used. When the RFID tag receives energy through radio waves for generating the supply voltage (V_{DD}), the 13.56-MHz RF signal in the antenna of the RFID tag is not modulated and keeps its magnitude by turning off the modulation transistor, as shown in Fig. 3. At this time, the output enable signal (EN) is "0" and the RFID logic output becomes "0." In contrast, when the RFID tag data is transmitted to the RFID reader, the 13.56-MHz RF signal in the antenna is modulated according to the RFID logic output, as shown in Fig. 3. At this time, the EN is "1" and the RFID logic output becomes "10" or "01" according to the data stored in the ROM, as shown in Fig. 8(a). The Manchester encoder circuit is made of two XOR gates and a DFF, as shown in Fig. 8(b). Figure 8(c) shows the Manchester encoding operation with three 120-degree phase-shifted clocks. If the enable bar signal is "0," the RFID logic output becomes "10" or "01." If not, the RFID logic output remains at "0" to turn off the modulation transistor.

Figure 9 shows the 16-bit code generation circuit. The 16-bit

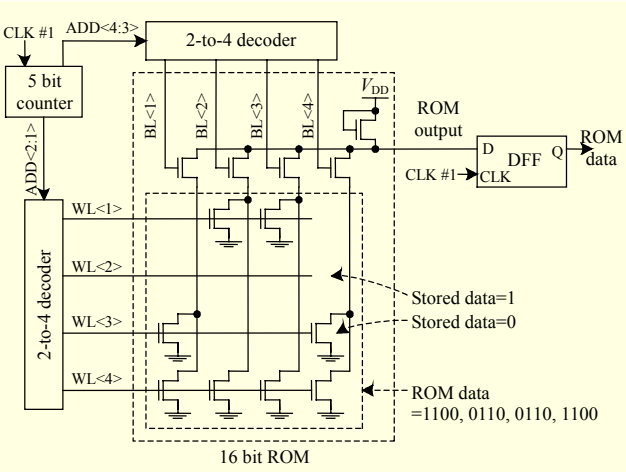


Fig. 9. 16-bit code generation circuit.

ROM stores 16-bit data with "1100,0110,0110,1100." If the stored data is "0," a pull-down transistor exists. The transistor is selected by a WL and a BL and then the ROM output becomes "0." If not, no pull-down transistor exists and the ROM output becomes "1" by the diode-connected pull-up transistor. The 5-bit counter with 5-bit address output (ADD<5:1>) increases one by one. Two 2-to-4 decoders select a WL and a BL according to ADD<2:1> and ADD<4:3>, respectively. The 16-bit ROM data is sequentially accessed out by the selected WL and BL. The stored ROM data is easily changed by positioning the pull-down NMOS transistor. The DFF

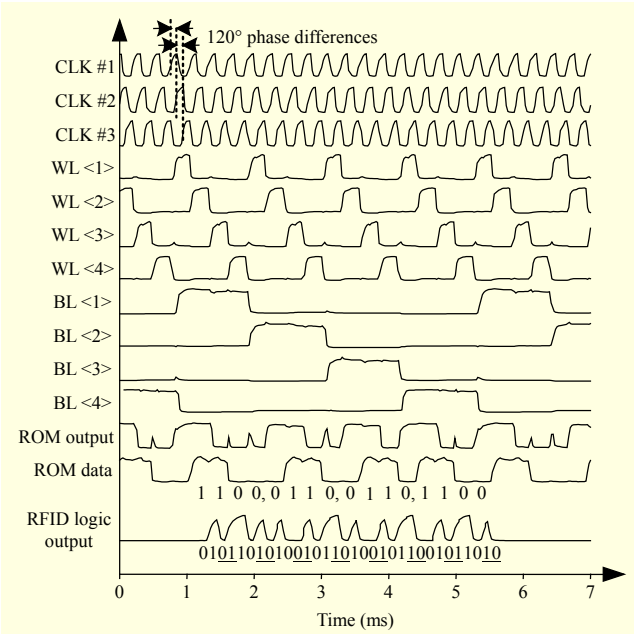


Fig. 10. Simulated waveforms of RFID tag.

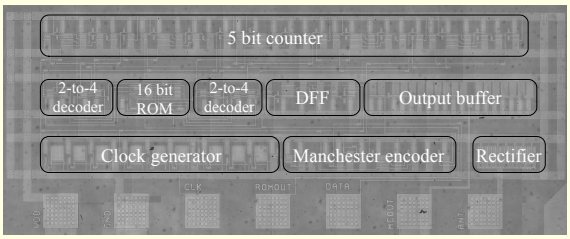


Fig. 11. Microphotograph of RFID logic chip.

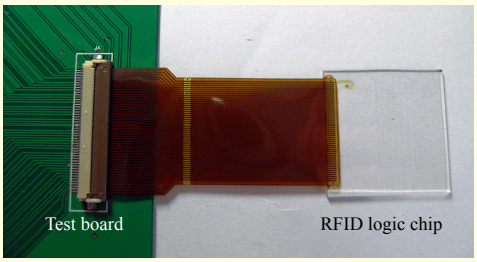


Fig. 12. Photo of transparent RFID logic chip.

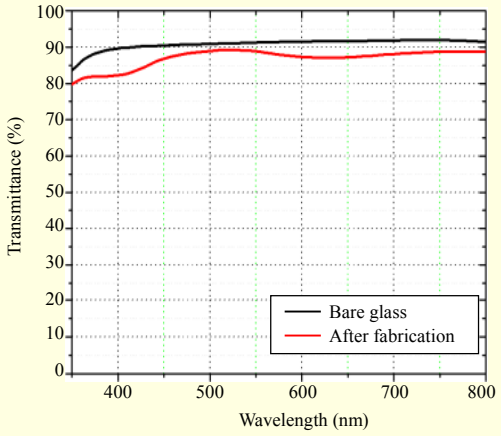


Fig. 13. Transmittances of transparent RFID logic chip.

synchronizes the ROM data with CLK #1 for the Manchester encoding.

Figure 10 shows the simulated waveforms of the RFID logic circuit. The simulation is performed with the HPSICE simulation models extracted from the measured model parameters of a-IGZO TFTs. The three clock signals (CLK #1 to CLK #3) are generated from the clock generator. The counter makes the address (ADD<4:1>) for the 16-bit ROM. The ADD<4:1> sequentially selects a WL and a BL among four WLs and four BLs (WL<1:4> and BL<1:4>) to read the ROM data. The noisy ROM output signal is changed to the clear ROM data signal in the DFF. The ROM data is encoded to the RFID logic output in the Manchester encoder.

III. Measurement Result

The transparent RFID logic circuit is implemented in the transparent a-IGZO TFT technology. Figure 11 shows a microphotograph of the RFID logic chip. The contrast of the microphotograph is enhanced for clear layout. The area of the RFID logic chip is 5.85 mm^2. The total number of transistors is 222. Figure 12 shows a photo of the transparent RFID logic chip and its test board connections. Figure 13 exhibits the transmittances of the RFID logic chip. The transmittances of the bare glass and after the gate fabrication are 91.2% and 88.8% at a 550-nm wavelength, respectively. The transmittance degradation due to the RFID logic chip is only 2.5% at a 550-nm wavelength. The transmittance after the gate fabrication is 80% to 89% in a 300-nm to 800-nm wavelength. The transmittance degradation due to the RFID logic chip is 2.5% to 8%.

Figures 14(a) and 14(b) show the measured operating clock frequency and the measured power consumption of the RFID logic chip according to the supply voltage (V_{DD}), respectively. The operating clock frequency and power consumption are 3.2 kHz and 170 μW at V_{DD}=6 V, respectively. The minimum supply voltage is 5.4 V. Figure 15 shows the measured waveforms of the RFID logic chip. The digital output of the RFID logic chip is the Manchester encoded signal of the ROM data. The features of the RFID logic chip are summarized in Table 1.

The simulation waveforms shown in Fig. 10 and the measured waveforms shown in Fig. 15 reflect the same RFID

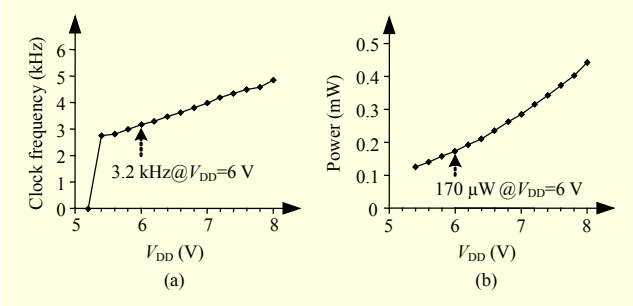


Fig. 14. (a) Measured operating clock frequency and (b) measured power consumption of RFID logic chip.

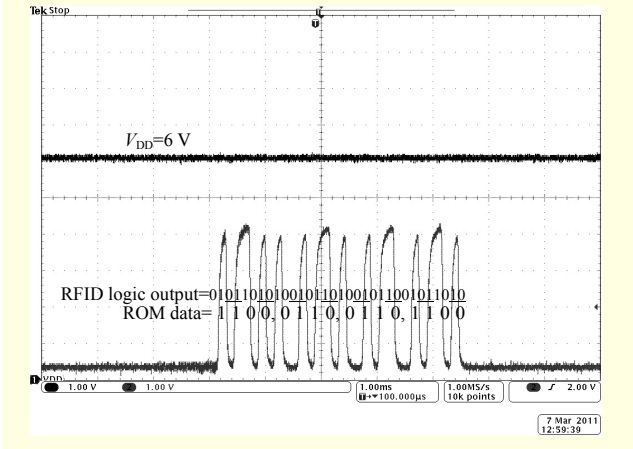


Fig. 15. Measured waveforms of RFID logic chip.

Table 1. Features of transparent RFID logic chip.

Technology	Transparent a-IGZO TFT technology
Transmittance	84% to 92% in bare glass 80% to 89% after gate fabrication @ 300-nm to 800-nm wavelength
Transmittance degradation	2.5% to 8% due to RFID logic chip @ 300-nm to 800-nm wavelength
Data length	16 bit
Encoding	Manchester encoding
Min. V_{DD}	5.4 V
Frequency	f_{CLK} = 3.2 kHz @ V_{DD} = 6 V
Power	170 μW @ V_{DD} = 6 V
Number of transistors	222
Area	5.85 mm^2 (3.9 mm × 1.5 mm)

logic outputs. However, the operation clock frequencies of the simulation and measurement results are 3.6 kHz and 3.2 kHz at V_{DD}=6 V, respectively. The difference comes from the fabrication process variations of a-IGZO TFTs, the HSPICE modeling errors, and the parasitic capacitance due to wire interconnections.

IV. Conclusion

A transparent logic circuit for the RFID tag was implemented in a-IGZO TFT technology. The RFID logic circuit generated 16-bit code programmed in read-only memory. All circuits were implemented in a pseudo-CMOS logic style using transparent a-IGZO TFTs. The transmittance degradation of the RFID logic chip was 2.5% to 8% in a 300-nm to 800-nm wavelength. The RFID logic chip generated Manchester encoded 16-bit data with a 3.2-kHz clock frequency and consumed 170 μW at V_{DD}=6 V. It employed 222 transistors. The area of the RFID logic chip was 5.85 mm^2.

References

[1] S.H. Cho et al., "Oxide Thin Film Transistor Circuit for Transparent RFID Applications," *IEICE Trans. Electron.*, vol. E93, no. 10, Oct. 2010, pp. 1504-1510.

[2] N.J. Kirsch et al., "Optically Transparent Conductive Polymer RFID Meandering Dipole Antenna," *IEEE Int. Conf. RFID*, Orlando, FL, USA, Apr. 27-28, 2009, pp. 278-282.

[3] C.C. Serra et al., "Mirror-Integrated Transparent Antenna for RFID Application," *IEEE Antennas Wireless Propag. Lett.*, vol. 10, 2011, pp. 776-779.

[4] E. Cantatore et al., "A 13.56-MHz RFID System Based on Organic Transponders," *IEEE J. Solid-State Circuits*, vol. 42, no. 1, Jan. 2007, pp. 84-92.

[5] K. Myny et al., "A 128b Organic RFID Transponder Chip, Including Manchester Encoding and ALOHA Anti-collision Protocol, Operating with a Data Rate of 1529 b/s," *IEEE ISSCC Dig. Tech. Papers*, San Francisco, CA, USA, Feb. 8-12, 2009, pp. 206-207.

[6] K. Myny et al., "Unipolar Organic Transistor Circuits Made Robust by Dual-Gate Technology," *IEEE J. Solid-State Circuits*, vol. 46, no. 5, May 2011, pp. 1223-1230.

[7] H.-S. Shin et al., "Novel a-Si:H TFT V_{th} Compensation Pixel Circuit for AMOLED," *Proc. ASID*, New Delhi, India, Oct. 2006, pp. 466-469.

[8] M. Halik et al., "High-Mobility Organic Thin-Film Transistors Based on α,α'-didecyloligothiophenes," *J. Appl. Phys.*, vol. 93, no. 5, Mar. 2003, pp. 2977-2981.

[9] A.T. Voutsas, "A New Era of Crystallization: Advances in Polysilicon Crystallization and Crystal Engineering," *Appl. Surface Sci.*, vols. 208-209, Mar. 2003, pp. 250-262.

[10] B.-T. Chen et al., "New Pixel Circuits for Driving Active Matrix Organic Light Emitting Diodes," *Solid-State Electron.*, vol. 50, no. 2, 2006, pp. 272-275.

[11] M.K. Ryu et al., "High Performance Thin Film Transistor with Cosputtered Amorphous Zn–In–Sn–O Channel: Combinatorial Approach," *Appl. Phys. Lett.*, vol. 95, no. 7, Aug. 2009, pp. 072104_1-072104_3.
[12] C.-S. Hwang et al., "Oxide TFTs for Transparent AMOLED," *IMID Dig.*, Seoul, Rep. of Korea, Oct. 2011, pp. 64-65.
[13] T.-C. Huang et al., "Pseudo-CMOS: A Design Style for Low-Cost and Robust Flexible Electronics," *IEEE Trans. Electron. Dev.*, vol. 58, no. 1, Jan. 2011, pp. 141-150.

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Min Ki Ryu received his BS and PhD from Pusan National University, Busan, Rep. of Korea, in 1998 and 2005, respectively, both in solid-state physics. Since he joined ETRI, Daejeon, Rep. of Korea, in 2006, he has been involved in oxide electronics, including oxide TFTs and memory devices.

Jae-Eun Pi received his BS and MS in electronics engineering from Konkuk University, Seoul, Rep. of Korea, in 2009 and 2011, respectively. In 2011, he joined the Oxide Electronics Research Team of ETRI, Daejeon, Rep. of Korea. His research interests include transparent electronics and flat panel display circuits.