A Broadband Digital Step Attenuator with Low Phase Error and Low Insertion Loss in 0.18-μm SOI CMOS Technology

Moon-Kyu Cho, Jeong-Geun Kim, and Donghyun Baek

This paper presents a 5-bit digital step attenuator (DSA) using a commercial 0.18-μm silicon-on-insulator (SOI) process for the wideband phased array antenna. Both low insertion loss and low root mean square (RMS) phase error and amplitude error are achieved employing two attenuation topologies of the switched path attenuator and the switched T-type attenuator. The attenuation coverage of 31 dB with a least significant bit of 1 dB is achieved at DC to 20 GHz. The RMS phase error and amplitude error are less than 2.5° and less than 0.5 dB, respectively. The measured insertion loss of the reference state is less than 5.5 dB at 10 GHz. The input return loss and output return loss are each less than 12 dB at DC to 20 GHz. The current consumption is nearly zero with a voltage supply of 1.8 V. The chip size is 0.93 mm × 0.68 mm, including pads. To the best of the authors' knowledge, this is the first demonstration of a low phase error DC-to-20-GHz SOI DSA.

Keywords: Wideband, phased array antenna, low phase error, SOI, digital step attenuator, SPDT, DPDT switch.

I. Introduction

The wideband digital step attenuator (DSA) is an essential component of the T/R modules for wideband phased array antennas and beamforming systems [1]-[3]. The key issues in designing a DSA are achieving low phase error, low amplitude error, and low insertion loss. Despite considerable technical progress, it is still challenging to design a DSA with both low phase error and low insertion loss [4], [5]. A T/R module must be equipped with an additional phase correction circuit if a DSA does not have low phase error. Also, a DSA with high insertion loss entails an additional gain compensation circuit. Eventually, both the power consumption and the size of the T/R modules increase.

The multibit DSA can be designed by duplicating the attenuators illustrated in Fig 1. Among the various attenuator topologies, the switched path attenuator in Fig. 1(a) provides the lowest number of phase errors with the highest operating bandwidth [6]. The amount of attenuation is determined by the insertion loss difference between the reference path and the attenuation path. The loss difference is simply made by a π or T-type resistive network, usually composed of three resistors in the attenuation path. In this topology, the single pole double through (SPDT) switches are separated by a resistive network, making it easy to design the attenuator with low phase error and wide operating bandwidth. However, the switched path attenuator shows high insertion loss at the reference state because of the accumulated switch loss of the SPDT switches in a multibit attenuator. This occupies a large chip area due to the multiple times the SPDT switches are used. Therefore,
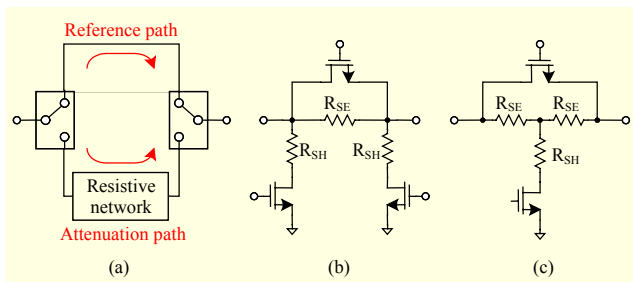
Fig. 1. Topologies of digital attenuators: (a) switched path attenuator, (b) switched π-type attenuator, and (c) switched T-type attenuator.

Fig. 2. Block diagram of 5-bit SOI DSA.

to decrease the insertion loss in the switched path attenuator, the number of SPDT switches and the insertion loss of the SPDT switch itself must be reduced.

On the contrary, the switched T-type or π-type resistive attenuators occupy a small chip area and have low insertion loss since the SPDT switches are integrated with the resistive network, as shown in Figs. 1(b) and 1(c) [7], [8]. However, these topologies generally show high phase error and a limited operating bandwidth due to the variation of the parasitic elements in the switch transistors in on and off states. Therefore, a small switching transistor with low parasitics should be used, which means the attenuation with high attenuation coverage cannot be realized without deteriorating bandwidth and phase error.

Compared with the GaAs technology, the silicon-on-insulator (SOI) CMOS technology applied in the T/R modules for the wideband phased array antennas has drawn more attention lately for three reasons: low cost, small chip area, and high integrability [9]. Nonetheless, SOI DSAs that only operate at less than 6 GHz have been reported. Furthermore, because these DSAs have high phase error, they are not appropriate for application in the phased array antennas [10], [11].

In this paper, a broadband 5-bit passive DSA using commercially available 0.18-μm SOI technology is presented. The proposed attenuator achieves low insertion loss and low phase error simultaneously at DC to 20 GHz by combining two attenuator topologies and introducing double pole double through (DPDT) switches. The proposed attenuator performs better than or comparably to the GaAs DSA in respect to the insertion loss, the RMS phase error and amplitude error, and the chip size.

II. Design of 5-Bit SOI Digital Step Attenuator

The proposed 5-bit DSA is shown in Fig. 2. It is composed of two SPDT switches, two DPDT switches, T-type resistive networks, and a digital switch controller. The digital switch controller controls the SPDT switches (S_1, S_4), the DPDT
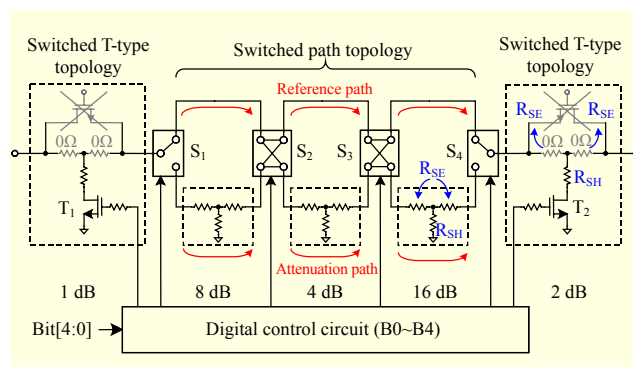
switches (S_2, S_3), and the switching transistors (T_1, T_2) to obtain the required attenuation states according to five input control bits. The DSA uses only passive devices; thereby, the step attenuator can operate bidirectionally.

In the proposed DSA, two different attenuator circuit topologies are used at the same time: one is the switched path topology using the DPDT and SPDT switches, and the other is the switched T-type topology. The switched path topology is employed for the high attenuation states of 4 dB, 8 dB, and 16 dB. This topology can suppress the phase variations in all attenuation states and ensure wideband operating bandwidth since the parasitic elements of the switch transistors are nearly identical in each attenuation state. However, it has a high insertion loss problem due to a number of SPDT switches and its accumulated losses. This loss problem is overcome by reducing the number of series switch transistors by introducing the DPDT switch. Two SPDT switches used in the conventional attenuator are substituted with a single DPDT switch. Furthermore, by choosing the switched T-type topology, which does not need any switches for low attenuation steps of 1 dB and 2 dB, the required number for the SPDT switches is cut down. Eventually, since the input signal passes through only four series switch transistors, the insertion loss and the chip size are reduced considerably. Additionally, the limited bandwidth in the switched T-type attenuator is successfully dealt with by applying this topology to low attenuation steps only.

The series resistance (R_{SE}) values and parallel resistance (R_{SH}) values of the T-type resistive networks for each attenuation step are summarized in Table 1. The high attenuation states of 4 dB, 8 dB, and 16 dB are controlled by steering the signal paths between the reference path and the T-type resistive network path using the SPDT and DPDT switches. The low attenuation states of 1 dB and 2 dB are controlled by directly switching the parallel resistances on or off. The series resistances of the T-type resistive networks for 1-dB and 2-dB attenuations are about 3 Ω and 6 Ω, which is

Table 1. Series and shunt resistance values of T-type networks.

	1 dB	2 dB	4 dB	8 dB	16 dB
$R_{SE}(\Omega)$	0 (3*)	0 (6*)	11	22	36
$R_{SH}(\Omega)$	433	215	105	47	16

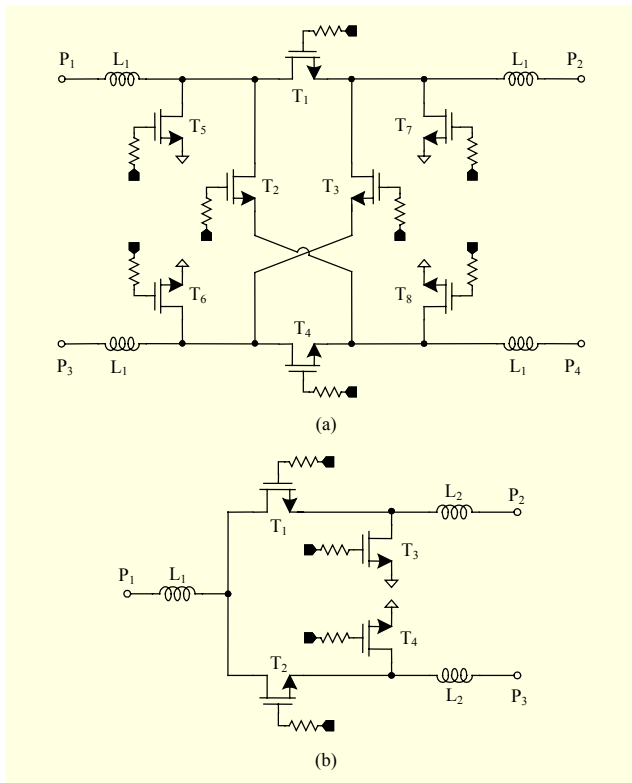*Theoretical values of T-type resistive networks for 1-dB and 2-dB attenuations.

Fig. 3. Schematic circuits of (a) DPDT switch and (b) SPDT switch.

low enough to be removed without performance degradation of the input return loss and output return loss. The series switching transistors are also eliminated. The parallel resistances for 1-dB and 2-dB attenuations are 433 Ω and 215 Ω, respectively. These resistors are turned on or off to achieve the required attenuation.

Figure 3(a) shows the absorptive DPDT switch, in which the series transistors are used for signal switching and the shunt transistors are employed for improving port-to-port isolations. All the transistors are implemented with floating-body FETs to reduce the substrate leakage. Four cross-connected series transistors with 12 fingers and a 120-μm gate width (T_1-T_4) and four shunt transistors with 11 fingers and a 66-μm gate width (T_5-T_8) are used in the DPDT switch. Only one cross-connected transistor turns on and links the input port to the output port, which means that a low insertion loss can be achieved. The shunt transistors (T_5-T_8) improve the isolation

to prevent unwanted leakage signals. The series inductors (represented by L1) of approximately 200 pH each are included to improve the matching characteristic at a high frequency.

The low attenuation states of 1 dB and 2 dB are located at the input and output ports to reduce the chip size and the insertion loss, respectively. The 16-dB attenuation state is positioned at the end of the attenuator among the three-stage switched-path attenuators, since the higher attenuation bit has the lowest power-handling capabilities [4]. Considering the bidirectional operation, the 8-dB attenuation state is placed at the first position. The final bit order is 1 dB, 8 dB, 4 dB, 16 dB, 2 dB.

The simulated insertion losses and the isolations are less than 1.2 dB and greater than 30 dB, respectively, up to 20 GHz. The SDPT switches with the absorptive configuration are used at the input and output ports, as illustrated in Fig. 3(b). Since the input signal passes through only four series transistors in the proposed 5-bit DSA configuration as opposed to six series transistors, the insertion loss can be improved by using only the SPDT switches. The top metal of the AM layer and the metal of the MT layer are employed for the vertically stacked spiral inductors to reduce the chip size. The inductors and interconnection lines are carefully characterized using the electromagnetic simulator of SONNET. In the proposed attenuator, the switching elements and T-type resistive networks are separated from one another; therefore, each design can be optimized independently.

III. Measured Results

The 5-bit DSA is fabricated using 0.18-μm IBM 7RF SOI technology. A microphotograph of the fabricated attenuator is shown in Fig. 4. The chip size is 0.93 mm × 0.68 mm, including all pads. The on-wafer measurement is performed with SOLT calibration. The S-parameters are obtained using a PNA of Agilent 8563C. The P1dB is characterized using a
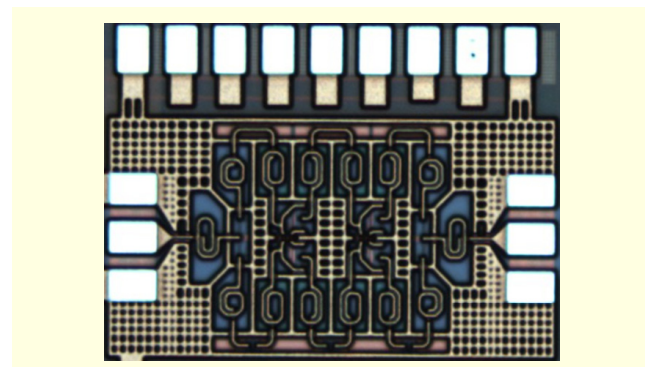

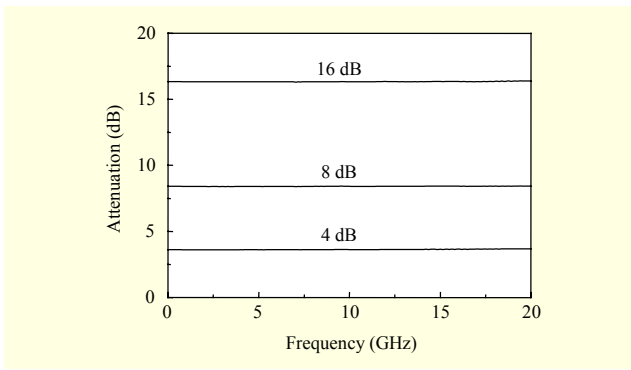Fig. 4. Microphotograph of 5-bit SOI DSA.

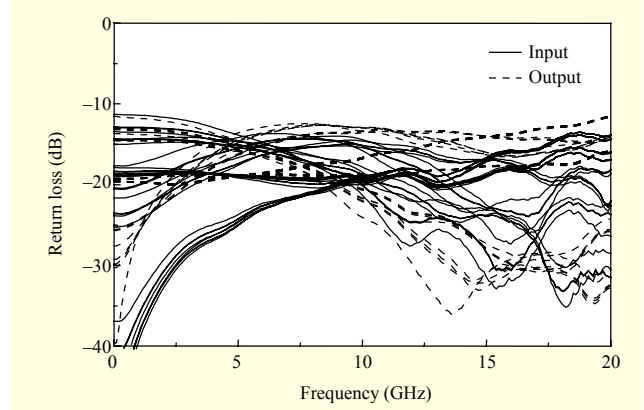Fig. 5. Measured attenuation of T-type resistive attenuators.
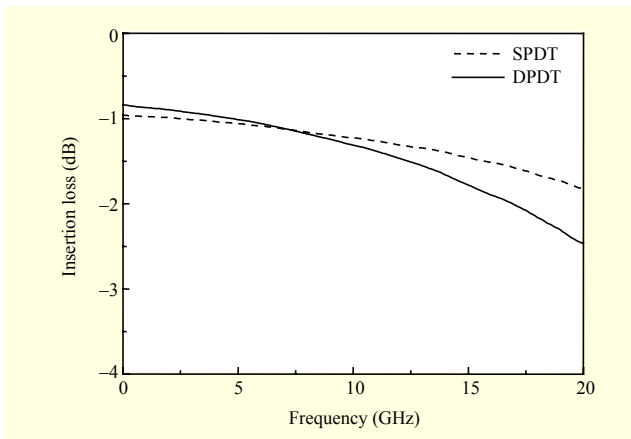

Fig. 6. Measured insertion losses of SPDT and DPDT switches.

Fig. 7. Measured insertion loss of attenuator (all states).

Fig. 8. Measured input and output return losses (all states).

Fig. 9. Measured RMS phase error and amplitude error of attenuator.
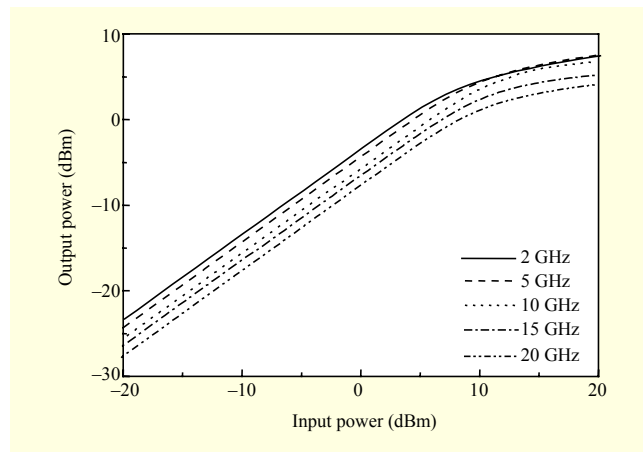

Fig. 10. Measured P1dB of attenuator.

PXG of Agilent E8257D and a PSA of Agilent E4440A.

Figure 5 shows the measured attenuations of the test patterns for the T-type resistive networks for 4 dB, 8 dB, and 16 dB. The measured results show flat attenuation performances up to 20 GHz. The measured insertion losses of the SPDT and the DPDT switches are less than 1.2 dB and less than 1.3 dB up to 20 GHz, respectively, as shown in Fig. 6. The measured

insertion losses of the proposed DSA in all states are shown in Fig. 7. The measured insertion losses of the reference state are less than 7.6 dB at DC to 20 GHz. The maximum attenuation of 31 dB with a least significant bit (LSB) of 1 dB is achieved. As shown in Fig. 8, the input and output return losses are less than 12 dB at DC to 20 GHz. A measured RMS amplitude

Table 2. Comparison of DSAs.

	[1]	[3]	[4]	This work
Technology	GaAs	GaAs	0.18-µm CMOS	0.18-µm SOI
Number of bits	5	6	6	5
Attenuation range (dB)	27.9	31.5	31.5	31
Frequency (GHz)	DC-18	1-15	8-12	DC-20
Insertion loss (dB)	3-7	3-6.2	9.8-11.3	3.1-7.6
Return loss (dB)	> 17	> 13	> 11	> 12
RMS amplitude error (dB)	0.5	0.25	0.4	0.5
RMS phase error (deg)	10	5	2.2	2.5
Input P1dB (dBm)	24	20	13	10
Size (mm²)	2.40×1.60	2.60×1.20	0.67×0.50*	0.93×0.68

*Size of pads is excluded.

error of less than 0.5 dB and RMS phase error of less than 2.5° are achieved at DC to 20 GHz, as shown in Fig. 9. The measured input P1dB of the attenuator is greater than 10 dBm at 10 GHz, as shown in Fig. 10. The total DC power consumption is nearly 0 mW with a 1.8-V supply voltage.

Table 2 shows a performance comparison of the previously published DSAs. The proposed attenuator shows excellent performances in respect to the insertion loss, the RMS amplitude error and phase error, and the chip size.

IV. Conclusion

This paper presented a DC-to-20-GHz 5-bit DSA using commercial 0.18-µm SOI CMOS technology. Two attenuator topologies of the switched path topology and the switched T-type topology were combined to achieve low insertion loss, low RMS phase error, and low amplitude error simultaneously. Also, a small chip size was obtained by reducing the number of switches and using on-chip vertically stacked inductors. The maximum attenuation range was 31 dB with an LSB of 1 dB. The measured insertion loss was less than 7.6 dB at DC to 20 GHz. The RMS phase and amplitude errors were less than 2.5° and less than 0.5 dB, respectively, at DC to 20 GHz. The current consumption was nearly zero with a 1.8-V supply voltage. The chip size was 0.93 mm × 0.68 mm. The proposed DSA showed excellent performances in respect to the insertion loss, the RMS amplitude error and phase error, and the chip size. The attenuator can be applied to a low cost wideband phased array antenna.

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