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Research Article

High-Electron-Mobility SiGe on Sapphire Substrate for Fast Chipsets

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High-quality strain-relaxed SiGe films with a low twin defect density, high electron mobility, and smooth surface are critical for device fabrication to achieve designed performance. The mobilities of SiGe can be a few times higher than those of silicon due to the content of high carrier mobilities of germanium (p-type Si: 430 $cm^2/V{\cdot}s$, p-type Ge: 2200 $cm^2/V{\cdot}s$, n-type Si: 1300 $cm^2/V{\cdot}s$, and n-type Ge: 3000 $cm^2/V{\cdot}s$ at 10^{16} per cm^3 doping density). Therefore, radio frequency devices which are made with rhombohedral SiGe on *c*-plane sapphire can potentially run a few times faster than RF devices on SOS wafers. NASA Langley has successfully grown highly ordered single crystal rhombohedral epitaxy using an atomic alignment of the [111] direction of cubic SiGe on top of the [0001] direction of the sapphire basal plane. Several samples of rhombohedrally grown SiGe on *c*-plane sapphire show high percentage of a single crystalline over 95% to 99.5%. The electron mobilities of the tested samples are between those of single crystals Si and Ge. The measured electron mobility of 95% single crystal SiGe was 1538 $cm^2/V{\cdot}s$ which is between 350 $cm^2/V{\cdot}s$ (Si) and 1550 $cm^2/V{\cdot}s$ (Ge) at $6 \times 10^{17}/cm^3$ doping concentration.

1. Introduction

The clock frequency of conventional silicon based chipset has achieved several gigahertz' levels by increasing line resolution of microcircuit. Time after time, critics have claimed that silicon transistors of smaller dimensions will soon come to the end of shrinking. Also, further speed enhancement faces intrinsic limit by the material properties, such as electron charge mobility. Pure single crystal of silicon has electron charge mobility slightly above 1000 $cm^2/V{\cdot}s$. To build fast chipsets, a different kind of materials that exhibit higher electron charge mobility than silicon's but is still compatible with silicon based fab technology is clearly required. In this regard, previously, many efforts had been carried out to develop single crystal SiGe which is compatible with the current silicon based fab lines and offers higher mobility, but without success [1]. We developed a rhombohedrally aligned silicon-germanium (SiGe) on *c*-plane sapphire substrate. This lattice-matched SiGe widely opens a possibility of chipset speed improvement without the costly efforts to reduce feature size. A lattice-matched SiGe has its own oxide as an insulator, SiO_2, unlike the arsenide, antimonide, or other compound semiconductors. Such an oxide with a proper insulator existing, SiGe, allows mass fabrication of several hundreds of chips on wafer basis.

The attainable speed of silicon-germanium chipsets is based on the gate length and the charge mobility which is related to a defect pattern such as twin population and crystal structure. Lattice-matched SiGe has very high mobility for a possibility of chipset speed improvement. The film surface morphology, number of twins, and dislocations will directly affect the wafer surface topography which sets the limits on yielding rate through device fabrication process. The surface roughness of wafers affects submicron photolithography, wafer bonding [2], edge loss [3, 4], and overall yielding rate. For CPU and memory, the generally known required root

mean square (rms) surface roughness is 0.5 nm~1 nm. The most tolerant case of surface roughness is for the solar cell fabrication requirement which varies from 1 nm to 100 nm. The defect densities on wafer are the key issue for sustaining high yield of nanofab devices [5]. To keep manufacturing costs low, the amount of epitaxy should be kept minimum both for lower consumption or source materials and for increased throughput.

SiGe on sapphire is one of the most important approaches to build silicon-germanium on insulator (SGOI) devices such as a high mobility transistor for K-band and higher frequency applications up to 116 GHz [6–8]. Because sapphire is one of the best insulators, the high frequency parasitic capacitance between the semiconductor layer and the substrate can be alleviated for better performance at high frequency. Many epitaxial growths in this regard utilize silicon on sapphire (SOS) and silicon-germanium on sapphire (SGOS, SGOI) technologies to take advantage of the rectangular r-plane of sapphire aligned with the square-faced (001) plane or rectangle-faced (110) plane of the Si and Ge diamond structure. However, it was reported that this approach often shows 90° rotated twin defects [9]. On the other hand, growth of SiGe layers on the trigonal (0001) plane, that is, c-plane of sapphire, has not been utilized for device fabrication so far due to the formation of 60° rotated twin defects.

In this paper, we present a possibility that rhombohedrally oriented single crystal SiGe could be a candidate material of next generation chipset by showing that electron mobilities of SiGe grown on c-plane sapphire substrate are higher than those of Si. And we investigated the effect of twin density on room temperature (RT) electron mobilities in SiGe grown on c-plane sapphire substrate. Also, our report includes the results of crystalline defects with chemical etching of SiGe film in order to determine the failure analysis required to produce useful SiGe layer for device.

2. Experimental

2.1. Film Growth. The epitaxial layer growth of SiGe was carried out in a magnetron sputtering system. The 2-inch sapphire substrate was cleaned with acetone, isopropanol, and deionized water before being placed onto the wafer holder within vacuum chamber. The back sides of the sapphire substrates were coated with carbon for effective heating of sapphire substrate to a desired level of epigrowth temperature. The sapphire wafer is transparent to infrared (IR) and visible light, and most of the heating due to IR light passes directly through the sapphire wafer without heating it up. Therefore, the actual temperature of the sapphire wafer surface was much lower than the temperature measured by the thermocouple of the substrate heater. In order to solve this problem, backside carbon coated sapphire wafers were prepared before the actual SiGe growth. The substrates were then baked under infrared heat at 200°C for 1 hour. The chamber temperature was then increased to 1000°C for a short time to remove any volatile contaminants. 95% single crystal SiGe film was grown at 890°C growth temperature, a 5-sccm of high-purity argon gas, and 5 mTorr chamber pressure. The rhombohedral alignment of cubic SiGe depends on the growth conditions, especially the growth temperature and the surface termination of the c-plane sapphire wafer. The number of twins was controlled by film deposition temperature during the SiGe deposition and sapphire wafer treatment before the SiGe deposition.

2.2. Film Characterization. The epilayer grown on sapphire substrate was characterized by several XRD methods developed by NASA Langley. The vertical atomic alignment was measured with a symmetric 2θ-Ω scan, which probes the surface normal direction. The prominent SiGe (111) peak at $2\theta \sim 27.5°$, which appears next to the sapphire (0006) and (00012) peaks, shows [111] oriented SiGe. The horizontal atomic alignment is measured with phi (ϕ) scan of the SiGe (220) peaks. Three strong peaks in the ϕ scan indicate the majority single crystalline SiGe and three small peaks indicate the 60° rotated SiGe twin crystal.

Phi (ϕ) Scan Method [10]. When the sample is tilted by angle χ, the sample normal n is tilted by angle χ with respect to the z-axis of the XRD goniometer. This situation is indicated in Figure 1. For example, when we grow SiGe (111) on c-plane sapphire (0001), the growth direction is aligned to [111] = n, while the asymmetric SiGe (220) planes are contained on the green plane with the angle $\chi = \beta = 35.264°$, which is the interplanar angle between (111) and (220) planes of SiGe. If we consider all of the {220} planes of the single crystal SiGe, there will be a total of 12 planes. However, 6 of these are located at the backside of the substrate, while the three planes, (02-2), (20-2), and (2-20), are oriented 90° with respect to the sample normal [111] and hence do not diffract X-rays. Only the three planes, (022), (202), and (220), strongly diffract. When SiGe layer contains twin defects comprised of both bulk domain and microtwin defects, the defects align as the 60° rotated twin crystal along [111]-axis. Therefore, the {220} reflections of twin crystal will be 60° off in the ϕ plane from the original crystal's {220} reflections. The twin crystal's {220} reflections are now shown as blue dots in Figure 1. Therefore, the ϕ scan with the angle $\chi = \beta = 35.264°$ shows the {220} peaks from both the original crystal and the 60° rotated twin crystal.

The y-axis is plotted in a log-scale and the twin crystal's peak is very weak compared with the majority single crystal's peak. And the untilted symmetric phi scan of SiGe {440} reflections shows three strong single crystal peaks and three weak twin defect peaks. By setting the sample's azimuthal ϕ angle to the desired peak (one of the strong single crystal peaks or one of the weak twin defect peaks) and translating the wafer in the X and Y directions, we obtain the X-Y mapping image of the SiGe film on c-plane sapphire wafer. The majority single crystal map shows a uniformly strong signal over the entire wafer surface with a small concentrated region of twin defects at the edge. The twin defects on edge were developed due to both the shadow by the wafer holder and the temperature gradient at the edge.

Atomic force microscope (AFM) measurements show the surface topographic variation and root mean square (rms) roughness of the SiGe layer. The crystal structure and layer thickness of the SiGe thin film were characterized using TEM

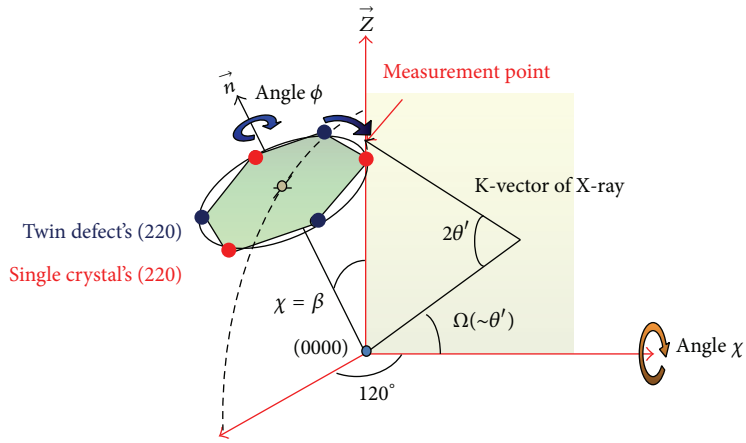

Figure 1: Phi (ϕ) scan with tilted χ for twin crystal detection.

Table 1: Etchant composition for etch-pit density tests and its effects.

Etch	Composition (Mol %)			Results on {100}	
	Solvent*	HF	Oxidizer**	Line defects	"Point" defects
Secco	67.6	32.2	0.17	Pits	Shallow pits or hillocks
Sirtl	71.2	26.3	2.5	Pits or mounds	—
Wright	78.5	16.1	5.4	Pits	Shallow pits
Seiter	78.5	5.9	15.6	Mounds	Mounds

*H_2O + CH_3COOH (HAc); **CrO_3 + HNO_3.

(FEI, Tecnai G2 F30, 300 KV). The room temperature electron mobilities and carrier densities of the SiGe films were measured using the Hall effect measurement system. To obtain reproducible results, the films were cut into several pieces of a standard sized square. Each corner of the square-cut SiGe film with specific doping concentration was soldered onto the four arms of the sample test platform to ensure ohmic contacts. The ohmic contacts can be also checked during the measurement process of Hall mobility.

To reveal the crystalline defects on fab silicon wafer, some chemical etching methods such as Wright [11], SECCO [12], Sirtl [13], and Dash [14] etches have been widely used in failure analysis of semiconductor. SECCO etch is a very useful chemical etching method for the characterization of defects on surface of bare silicon wafer [15].

SECCO etch uses an etchant composition of solvent, hydrofluoric acid (HF), and $K_2Cr_2O_7$ oxidizer as tabulated in Table 1. SECCO etch compositions are as follows [12]: hydrofluoric acid (HF), 67% by volume, and 0.15 M $K_2Cr_2O_7$ in H_2O, 33% by volume. When mixing the solution, 14.52 g of $K_2Cr_2O_7$ should be dissolved in 330 mL of H_2O. Then, the $K_2Cr_2O_7$ solution is poured into 670 mL of HF. After mixing, the total volume of the solution is kept in plastic chemical bottle. The defect area is under higher stress; hence, it will etch more quickly in SECCO etchant than the bulk semiconductor. In most of the cases, the result appears as an elliptical pit on substrate at the location of the defect. Optical microscopy is performed to inspect the crystalline defects pitted by SEC-CO etch.

3. Results and Discussion

Figure 2 shows the quality of crystalline SiGe film on c-plane sapphire through TEM and XRD. XRD normal scan data shows very strong SiGe (111) peak (Figure 2(a)). In order to check the distribution of SiGe crystal in azimuthal in-plane angles, we used the phi scan method for SiGe {220} peaks and sapphire {10–14} peaks. The phi scan of SiGe {220} peaks shows a large difference in alignment and ratio of majority single crystal. The majority peaks and minority primary-twin peaks that are rotated by 60° are noted as (i) and (ii) in Figure 2(b), respectively. The area ratio of the peaks is 95 : 5. In the mapping, a point X-ray source with a 5 nm beam mask was used: (c) shows that almost complete single crystalline SiGe layer was fabricated on the basal plane of trigonal sapphire. Three {10–14} peaks show the trigonal space symmetry of a sapphire crystal (Figure 2(d)). From the SAED pattern in the upper inset of Figure 2(e), the epitaxial relationship between majority SiGe film and sapphire substrate was found to be $(111)_{SiGe}//(0001)_{sapphire}$ and $[-112]_{SiGe}//[01\text{-}10]_{sapphire}$. These results demonstrate that the [111]-oriented rhombohedral heterostructure epitaxy of a cubic single crystalline SiGe layer on trigonal c-plane sapphire has been achieved. The SiGe layer was grown in layer-by-layer mode with few micrometers of thicknesses and a smooth interface (Figure 2(f)).

The charge mobility in semiconductor materials is determined and limited by several factors, such as alloy composition, interface roughness, interface charge scattering, lattice

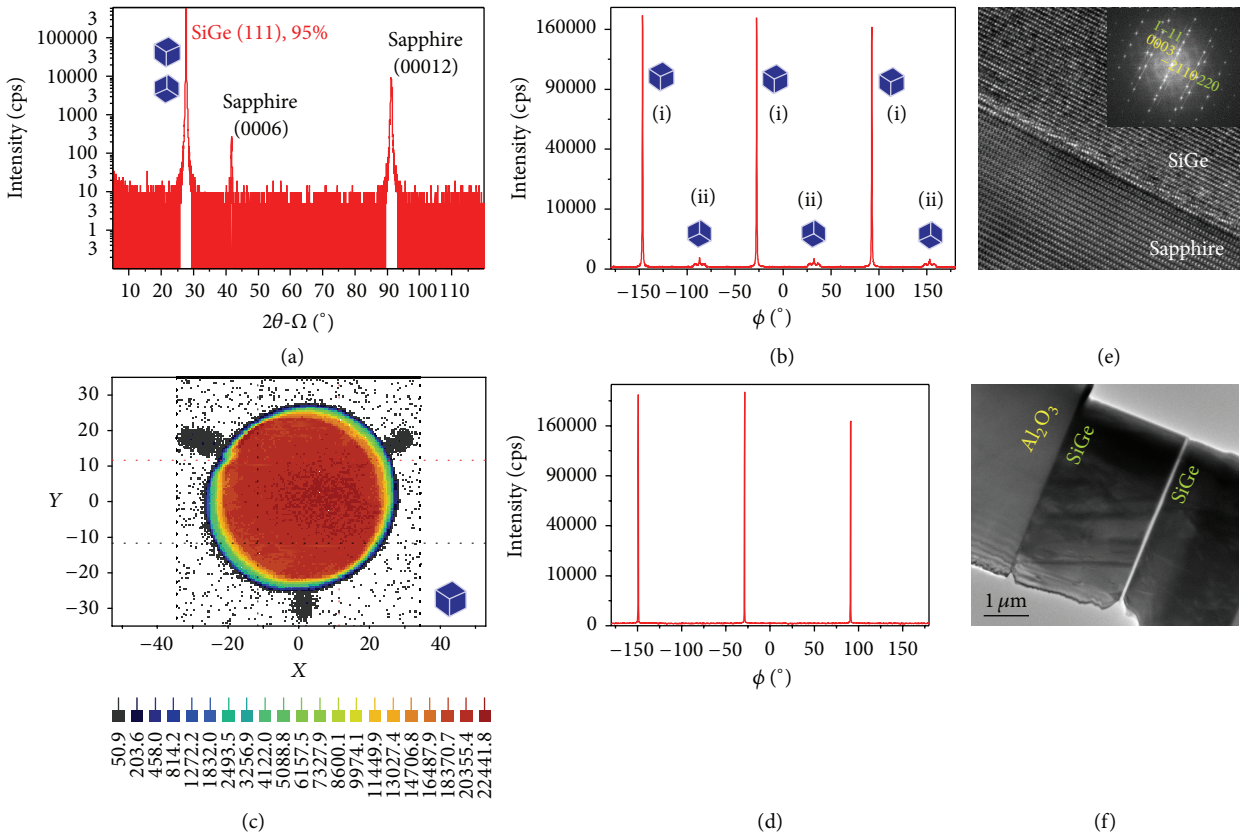

FIGURE 2: Analysis of the 95% single crystal SiGe film. Plot (a) shows θ-2θ scan in the direction normal to the surface, graph (b) shows phi scan of SiGe peaks for the relative atomic alignment, (c) X-Y wafer mapping with majority {440} peak shows the distribution of a single crystal, (d) shows phi scan of sapphire {10–14} peaks for relative atomic alignment, (e) shows HRTEM and its SAED result of the SiGe (green)/sapphire (yellow) interface, and (f) shows low magnification TEM image after the ion milling process.

mismatch or segregation, and strain relaxation of strained SiGe layers with large Ge content and layer width, as discussed in a recent review by Whall and Parker (2000) [18]. The results by Hall effect measurements indicate that the density of twin lattices is correlated with the electron mobility in the SiGe films. Figure 3(a) shows the calculated electron mobility for relaxed SiGe alloys as a function of their Ge content. As shown in Figure 3(a), relaxed SiGe alloys exhibit drastic decline in mobility mainly due to alloy interface scattering in dislocation populated polycrystal region, except for varying high Ge content (>0.85), where they start behaving like Ge [16, 17]. In Figure 3(a), the left side y-axis indicates the pure Si with $\mu_{n,\mathrm{Si}} = 1{,}400\ \mathrm{cm}^2/\mathrm{V{\cdot}s}$ and the right side y-axis the pure Ge with $\mu_{n,\mathrm{Ge}} = 4{,}000\ \mathrm{cm}^2/\mathrm{V{\cdot}s}$ [19, 20]. When epitaxial layer is grown on Si or Ge substrate, in either case alloy composition from pure Si or pure Ge lowers the electron carrier mobility rapidly and they often become polycrystal with many defects in the middle SiGe composition. In spite of the high mobility of Ge, the mobility of SiGe layer is substantially lowered due to the formation of strain caused dislocation defects. The strain caused dislocation defects occur mainly due to the lattice mismatch between Si whose lattice constant is 5.431 Å and Ge with 6.657 Å [21]. However, if a substrate allows growing a lattice-matched SiGe layer on it, these defect formation problems can be avoided and the mobility can be drastically enhanced beyond that of Si. Of course, not only is the growth of lattice-matched SiGe layer guaranteed by the crystal symmetry of substrate, but also the growth conditions, such as epilayer speed, substrate temperature, and pressure of processing gases, will dictate the formation of lattice-matched crystalline structures. We observed that the electron mobility is also strongly correlated with the dopant electron density. In Figure 3(b), we figured out the dependence of room temperature electron mobilities on defect density and dopant density in SiGe films. The measured dopant electron densities in three SiGe films are $2.21 \times 10^{17}/\mathrm{cm}^3$, $6.02 \times 10^{17}/\mathrm{cm}^3$, and $1.46 \times 10^{18}/\mathrm{cm}^3$. On the other hand, the defect density measurements were made by the XRD phi scan. The electron mobilities of the tested samples are between those of single crystal Si ($\mu_{n,\mathrm{Si}} = 1{,}400\ \mathrm{cm}^2/\mathrm{V{\cdot}s}$) and Ge ($\mu_{n,\mathrm{Ge}} = 4{,}000\ \mathrm{cm}^2/\mathrm{V{\cdot}s}$). The measured electron mobility of a 95% single crystal SiGe was $1538\ \mathrm{cm}^2/\mathrm{V{\cdot}s}$ which is between $350\ \mathrm{cm}^2/\mathrm{V{\cdot}s}$ (Si) and $1550\ \mathrm{cm}^2/\mathrm{V{\cdot}s}$ (Ge) at $6.02 \times 10^{17}/\mathrm{cm}^3$ dopant concentration. And the electron mobility of 99.5% single crystal SiGe is $1552\ \mathrm{cm}^2/\mathrm{V{\cdot}s}$ at the $6.02 \times 10^{17}/\mathrm{cm}^3$ dopant concentration. Figure 3(a) shows that the room

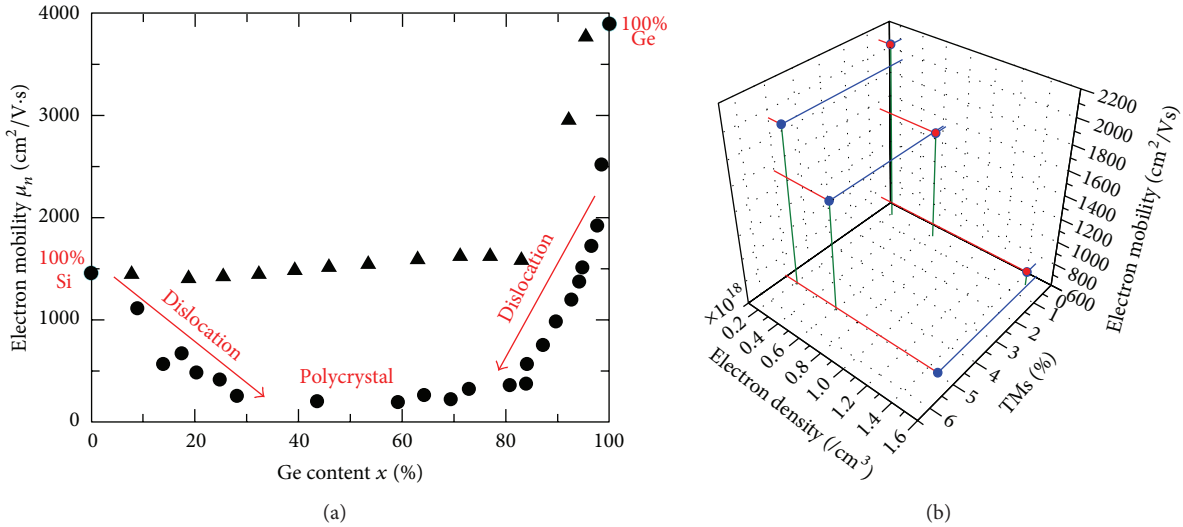

FIGURE 3: (a) Calculated phonon-limited 300 K electron low-field mobility in relaxed $Si_{1-x}Ge_x$ alloys. Results with (circle) and without (triangle) the inclusion of alloy scattering are shown [16, 17]. (b) Three pairs in three-dimensional (3D) plot for room temperature electron mobilities in SiGe films as a function of twin density (TM) and dopant concentration. Red and blue dots show the data points for 99.5% and 95% single crystal SiGe samples grown on c-plane sapphire substrates, respectively.

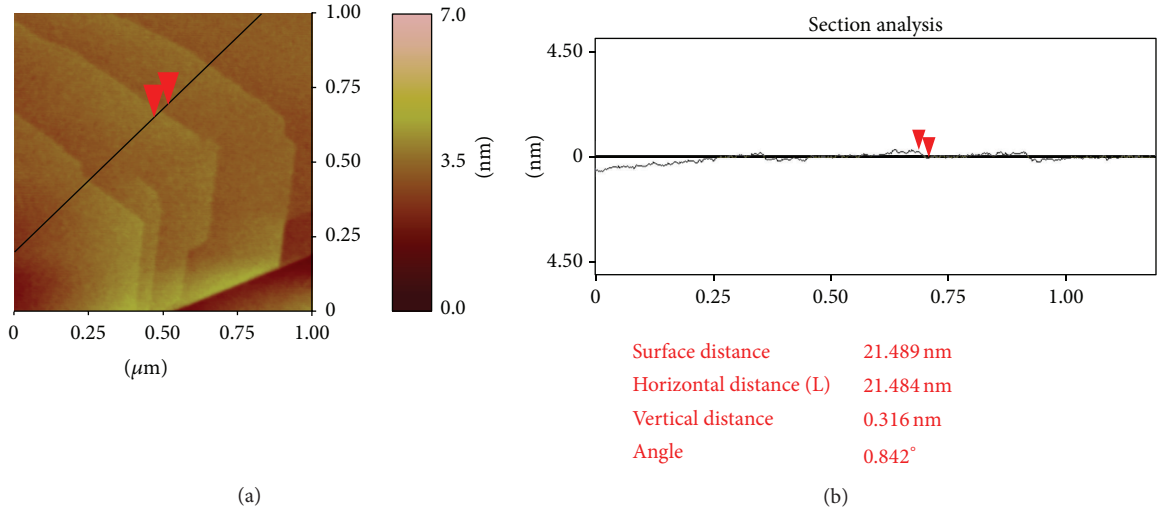

FIGURE 4: AFM image of SiGe layer on c-plane sapphire: (a) 1 μm × 1 μm area of a SiGe and (b) line profile of cross-section measured along the dark line in (a).

temperature electron mobility in the SiGe films grown on sapphire substrates becomes slightly higher as defect densities are decreased.

Since the topographical and morphological properties of the layer directly influence the charge carrier properties and the channel carrier transport characteristic of the device, the layer needs to be flat in atomic level. The SiGe layer shows a root mean square (rms) roughness of 2 nm for 1×1 μm^2 scan. The AFM analysis shows that the epitaxial layer grows in a layer-by-layer growth mode [22, 23], as shown in Figure 4(a). Figure 4(b) shows a line scan profile along the line indicated, which was selected to pass through a step. It is important to control the SiGe composition to reduce the lattice mismatch with the c-plane sapphire, maintain an appropriate molecular beam flux rate to ensure flat smooth layer-by-layer growth, and have 2D layer-by-layer growth in electronic microdevice fabrication.

Fine and delicate growth control of SiGe epitaxy to alleviate crystalline defects is a serious matter that directly affects yield in device fabrication. In particular, the collective effect of threading dislocations (TDs) attributed to performance degradation has been observed when other types of crystal defects exist individually [24]. In MOSFET, interface misfit dislocations (MDs) which extend between the source and

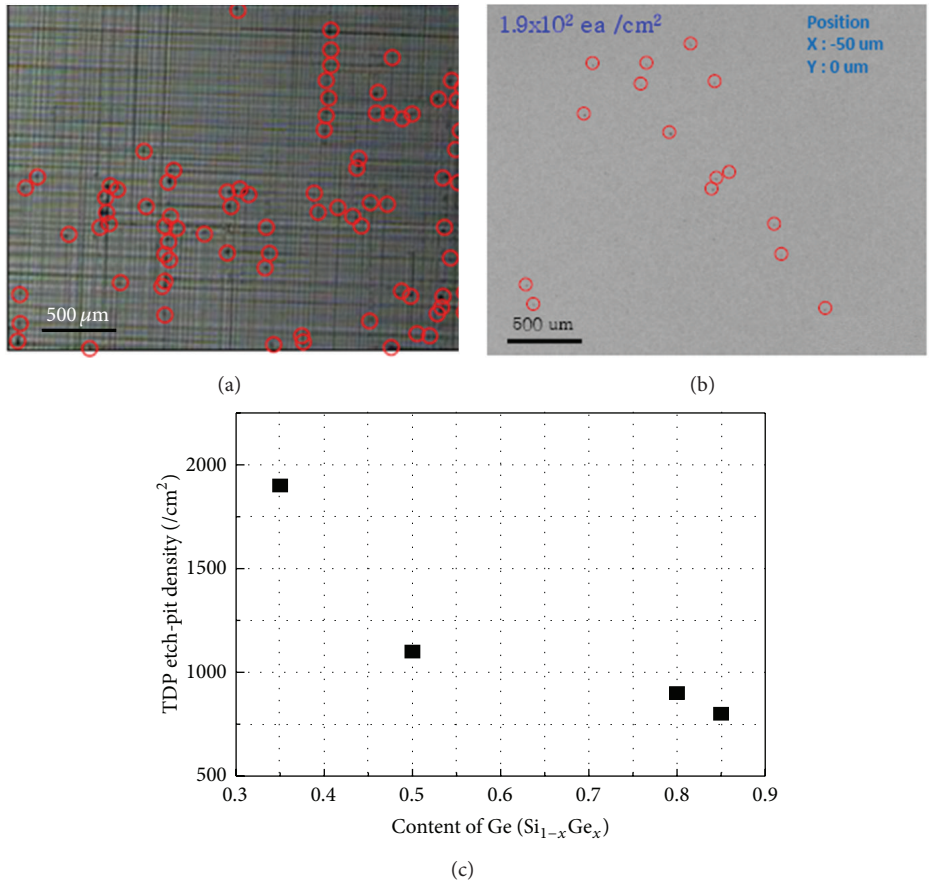

FIGURE 5: Etch-pit test results of (a) typical SiGe on Si(100) wafer with Ge content = 35% and of (b) rhombohedral SiGe on *c*-plane sapphire with Ge content = 35% (c) threading dislocation etch-pit density of $Si_{1-x}Ge_x$ on sapphire substrate based on the Ge content.

the drain may become electrically active, resulting in increased off-state leakage [25]. The electrical impact of stacking faults (SFs) on device operation can be seen as a combination of the individual effects of misfit and TDs. A single SF in the strained Si channel can degrade the device operation at both off- and on-state conditions [26]. SECCO etch is a chemical etching method used to delineath crystalline defects on silicon substrate and SiGe film. When SECCO etch is used directly, crystalline defects are revealed on silicon substrate or SiGe film after 2 minutes at some areas. Industry standard SECCO etch-pit density measurements were performed on a conventional SiGe layer on Si and 95% single crystalline SiGe layers with 35% Ge content on *c*-plane sapphire. A typical SiGe layer with 35% Ge content on a Si(100) wafer shows a high density of dislocation line and etch pits (see Figure 5(a)). On the other hand, the rhombohedral SiGe grown on *c*-plane sapphire with 35% Ge composition ratio shows two orders of magnitude less etch pits and no dislocation lines after performing the SECCO etching (see Figure 5). The conventional SiGe on a Si(100) wafer reveals a threading dislocation pit (TDP) density of $3.9 \times 10^4/cm^2$, line defect density of $1.73 \times 10^4/cm^2$, and a lot of cross-hatch patterns as shown in Figure 5(a). The rhombohedral SiGe grown on *c*-plane sapphire has only a TD etch-pit density of $1.9 \times 10^2/cm^2$, no visible line defects, and no cross-hatch patterns as shown in Figure 5(b). Therefore, the rhombohedral SiGe shows a 200 times less defect density than conventional SiGe on Si(100) wafer under the SECCO etching tests. Conclusively, we confirmed that a new SiGe film growth technique of fully relaxed SiGe alloy layers yields low TD density epitaxially grown on sapphire substrate [27]. The TD etch-pit density of SiGe on sapphire decreases to $800/cm^2$ as Ge content increases (see Figure 5(c)). The SiGe films with low TDP density, high electron mobility based on the high Ge content like 85%, and smooth surface were grown on *c*-plane sapphire substrate. These kinds of films are sufficiently qualified for the fabrication of the ultrafast chipsets like bipolar junction transistors.

The SGOI structures are currently fabricated mainly by two methods, layer transfer [28] and Ge condensation [29, 30]. In the layer transfer method, hydrogen implantation is employed in order to separate a thin SiGe layer from graded SiGe substrates. In the Ge condensation method, a SiGe layer with a low Ge concentration grown on a silicon-on-insulator (SOI) substrate is thermally oxidized, where Ge atoms in the SiGe layer are ejected from the oxide interface resulting in a SiGe layer with a high Ge concentration. However, these methods require complex processing routines and do not always

Table 2: Comparison of Si, SOI, and SiGe on Si and LM-SGOI technologies.

Technology	Si	SOI/SGOI	SiGe on Si	SiGe on sapphire (NASA LaRC)
Fabrication	Single crystal ingot	Hydrogen crack	Gradient layer, super lattice	**Lattice-matched growth**
Growth method	Czochralski	Wafer bonding	Epitaxial growth	**Epitaxial growth**
Lattice-matched Ge content	0%	0%	0%	**85% with sapphire substrate**
Ge content in strained layer before defects	0%	Usually 0~8%	Usually 0~8%	**85% achieved**
Ge content in relaxed layer	0% (not available)	Up to 25% with severe defects	Up to 25% with severe defects	**85% achieved with 0.2% defects**
Parasitic capacitance reduction	No	Yes	No	**Yes**
Device	Bipolar junction transistor (BJT), CMOS	BJT, CMOS/heterojunction bipolar transistor (HBT), CMOS	HBT	**HBT, CMOS**
Improvement	Conventional technology	High speed with insulating substrate	High speed (ultrathin SiGe lower collector voltage of HBT)	**High speed with thick and thin SiGe layer with insulating substrate, higher device yield with lower defects**

produce high-quality fully relaxed SiGe layer [31]. A different approach reported is an amorphous SiGe layer deposited on SOI substrate and then annealed above the melting point of SiGe after the formation of the SiO_2 capping layer [32]. This process has the advantage of simplicity. However, it is difficult to obtain the SiGe layer with high Ge concentration by this process, because the annealing temperature must be reduced below the melting point, resulting in the unusually long annealing time. Rapid thermal annealing (RTA) was also proposed in order to obtain the homogeneous SiGe layer [16]. However, high-quality and uniform SiGe layers were not obtained in the previous study.

We demonstrated the fabrication of high-quality SiGe layers on sapphire substrate by sputtering. The ideal of this process is that a fundamental governing relationship exists in rhombohedral epitaxy process, that is, the growth of ⟨111⟩-oriented cubic crystals on the basal *c*-plane of trigonal sapphire crystals [33–35]. One of the concerns with this epitaxy relationship is that two crystal structures tend to be formed which exhibit a twin lattice structure. This atomic alignment allows polytype crystalline structures with stacking faults on the (111) plane. Rhombohedral alignment, that is, aligning the [111] direction of a cubic structure to the [0001] direction of a trigonal structure, can have two possible azimuthal configurations. Two crystals are twin to each other and they can be formed by a stacking fault during the crystal growth process. We gained an experience to control the amount of the twins based on the growth conditions, especially the growth temperature and deposition power. Our process enables the forming of the SiGe layer of high Ge concentration (85%). For semiconductor device applications, high carrier mobility SiGe layers can be made by reducing stacking faults and microtwin defects. The measurement and control of stacking faults and twin crystals are, therefore, important in the microelectronics applications.

Table 2 illustrates the key features of lattice-matched SiGe on insulator (LM-SGOI) currently under development at NASA Langley [36–42] compared to existing products or technologies. The far right column of Table 2 shows the NASA Langley developed SiGe material that is compatible with the conventional insulator silicon oxide. The new rhombohedral epitaxy allows new lattice matching condition of SiGe on sapphire insulator with 85% Ge content and 0.5% defects. While the carrier mobilities of silicon-on-insulator (SOI) are limited by the silicon material, the mobilities of SiGe on *c*-plane sapphire can be a few times higher than those of silicon due to the high carrier mobilities of germanium. The silicon-on-sapphire (SOS) became crucial in devices using SOI wafers because sapphire is one of the best insulators. The SOS wafer provides electrically separated regions because of the insulating properties of the sapphire itself, as opposed to other typical devices where the regions are electrically separated using reverse bias between the substrate and device area. The space charge region (carrier depletion region) in the reverse bias case is very thin, in the micrometer range, and the capacitance between a device and the substrate is high and causes the device to have a leakage current at high frequency operating speeds. On the contrary, sapphire is very thick and has an ultrasmall capacitance, thereby reducing parasitic capacitance and leakage currents at high operating frequencies. The lattice-matched SiGe is also complemented by silicon oxide as an insulator and stable gate oxide with SiO_2 can make short gate length for RF device. Therefore, RF devices like heterojunction bipolar transistor (HBT) that

are made with rhombohedral SiGe on *c*-plane sapphire can potentially run a few times faster than RF devices on SOS wafers at high frequencies up to several hundred GHz.

4. Summary and Conclusions

In summary, we have experimentally demonstrated the fabrication of high-quality SiGe layers with a high Ge concentration of more than 85% on sapphire wafer by sputtering. We also report that the defect dependence of the electron mobility by the twinning of SiGe thin films on sapphire (0001) substrates was measured. Currently, a standard SiGe technology uses only ultrathin (30~100 nm) layer of SiGe for base layer of heterojunction bipolar transistor (HBT) to avoid dislocation defects. With the lattice-matched SiGe layer we developed, a thin or thick SiGe layer can be also fabricated for any designated applications, since the lattice-matched materials do not have a critical thickness limit. In rhombohedral SiGe on *c*-plane (0001) sapphire, the SiGe layer can be also grown in layer-by-layer mode from sub-100 nm to few micrometers of thicknesses. Therefore, thin rhombohedral SiGe on *c*-plane sapphire has many commercial application potentials as do SOI wafers in addition to solar cell applications. Typically, a rhombohedral single crystal SiGe has 2 or 3 times higher carrier mobility than monocrystalline silicon. The high Ge-content SiGe film shows high mobility, low cost, and simple structure when grown directly on sapphire substrate with sputtering process. If the defects in SiGe can be removed, transistors with higher operational frequencies can be fabricated for a new generation of ultrafast chipsets because of the high mobility of SiGe film.

Conflict of Interests

The authors declare that there is no conflict of interests regarding the publication of this paper.

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