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Latch-up based bidirectional npn selector for bipolar resistance-change memory

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A vertically integrated latch-up based n-p-n bidirectional diode, which is analogous to an open-base bipolar junction transistor, is demonstrated for bipolar resistance-change memory selector application. A maximum current density of $>50 \text{ MA/cm}^2$ and a selectivity of $>10^4$ are observed at a fast switching speed of within 10 ns. The high selectivity as a consequence of the sudden latch-up process is feasible owing to the positive-feedback process initiated by impact ionization. The optimization of the turn-on voltage is comprehensively investigated by numerical device simulation, which ensures the promising potential of the latch-up based selector device.

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Resistance-change memory (RRAM) has promising attributes in terms of usability in high-speed, nonvolatile electronic memory systems, and is therefore considered to be a potential replacement for the conventional flash memories.^{1,2} A crossbar-type RRAM array has been proposed and evaluated as a means of achieving high-density storage, owing to its simple architecture and 3D stacking potential.³ However, the intrinsic drawbacks of a passive RRAM crossbar array architecture including parasitic leakage paths through unselected cells and series interconnect resistance are unavoidable, which cannot be completely alleviated through optimization with an operational bias scheme.⁴ Although the use of transistors as selector devices would represent a near-perfect solution to such problems, they are difficult to fabricate with cell sizes below $6F^2$,⁵ thus, eliminating the advantages of the crossbar-type array in terms of high scalability.⁶

In light of these problems, tremendous technological effort has been devoted to developing a selector device that is integrable into a 1 selector-1 RRAM (1S-1R) configuration crossbar array. Several researchers have proposed various types of selector devices, including complementary resistive switches (CRSs),⁷ metal-insulator transition materials,⁸ mixed ionic electronic conduction materials (MIECs),⁹ Schottky diodes (Ni/TiO₂/Ni),¹⁰ and varistor-type bidirectional diodes (Pt/TaO_x/TiO₂/TaO_x/Pt).¹¹ For meeting the requirements of the high-density 1S-1R crossbar arrays, the maximum on-current density (J_{max}) of a selector device should exceed 10^7 A/cm^2 because the reset current of an RRAM is typically greater than $10 \mu\text{A}$.¹² In addition, the selectivity (defined as the ratio of the currents at the full-read (V_{READ}) and half-read voltages ($V_{READ}/2$)) are crucial in determining the readout margin where higher selectivity is demanded as far as possible.

Recently, another type of an n-p-n punchthrough-diode-based selector device has been proposed.¹³ As an advantage of the epitaxial Si layer, improved J_{max} performance could be achieved when compared with a polysilicon-based n-p-n diode.¹⁴ However, the reported selectivity value is limited to 10^3 , which is not greater than those of the other types of selector devices. In this study, an improved n-p-n diode is proposed by introducing a latch-up phenomenon. The proposed structure in this study is analogous to that of the aforementioned punchthrough diode; however, higher selectivity can be achieved as a consequence of the sudden latch-up phenomenon. Moreover, the proposed selector device can be fabricated by using conventional dry etching, and its scalability is confirmed up to the size of 22 nm.

Figure 1(a) shows the schematic of the proposed latch-up based n-p-n diode and its process flow. First, a three-step ion implantation process is carried out to form n⁺(doped by phosphorus)-p(doped by boron)-n⁺(doped by phosphorus) stacks. The secondary ion mass spectrometry (SIMS) profile confirms the doping concentration and thickness of each of the stacks as shown in Fig. 1(b). Next, a Si pillar is etched vertically by using an oxide hard mask (Fig. 1(c)), and the diameter of the Si pillar (D_{pillar}) is further reduced by the sacrificial oxidation process down to 22 nm. An oxide (SiO₂) is deposited by chemical-vapor-deposition (CVD) as an interlayer dielectric (ILD) and flattened by the chemical-mechanical polishing (CMP) process. Further, a via hole is patterned by conventional photolithography. *In situ* doped n⁺ poly Si is deposited as a top contact, and forming gas anneal is performed as the last step of the device fabrication.

The operation of the proposed latch-up diode can be understood by means of the positive-feedback system, as shown in Fig. 1(d). The latch-up behavior is analogous to the self-latch state in an open-base n-p-n bipolar junction transistor.^{15,16} When a specific voltage is applied to the collector terminal, excess holes are generated by impact ionization and accumulated in the floating p-type base region. These

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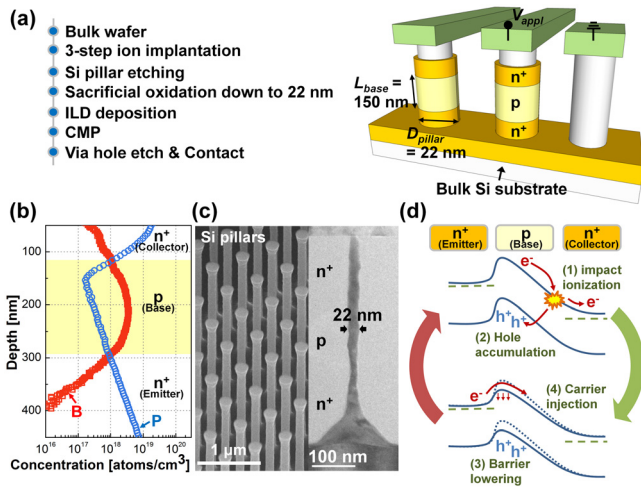


FIG. 1. (a) Process flow for the latch-up based n-p-n diode and schematic of the vertically integrated proposed device. (b) The SIMS profile is depicted in the vertical direction. The doping concentration is controlled by the ion implantation process (three-step implantation). The base length (L_{base}) is approximately 150 nm. (c) Tilted scanning electron microscope (SEM) image of as-fabricated vertical Si pillars and transmission electron microscopy (TEM) images of a latch-up diode. Diameter (D_{pillar}) and height of the Si pillar are 22 nm and 500 nm, respectively. (d) Schematic explaining the latch-up conditions. The base current (I_B) originating from impact ionization leads to a positive-feedback process.

generated holes contribute to the effective base current and consequently trigger the emitter-current injection. In other words, the positive-feedback system can be activated by the magnitude of the generated hole current (I_B). The collector current can be described by considering the common-emitter current gain (β) and multiplication factor (M),¹⁶ that is

$$I_C = \frac{M \cdot \beta}{1 - (M - 1) \cdot \beta} I_B.$$

In this system, instability occurs when the denominator $1 - (M - 1) \cdot \beta$ approaches zero.

Figure 2(a) shows the typical current-voltage (I - V) characteristics of the proposed latch-up diode. The current flow is suppressed at the low voltage regime because the proposed latch-up diode has higher doped base region than previously reported punchthrough diode. When the voltage level satisfies $(M - 1) \cdot \beta = 1$, the system becomes unstable and causes an abrupt increase in the current, that is, resulting in a latch-up phenomenon. The latch-up phenomenon consequently exhibits a symmetrical (i.e., bidirectional) behavior at both the positive and the negative voltages, because the proposed device has a symmetrical n-p-n structure. In addition, it can be noted that the measured data demonstrate a hysteresis; the latch-up voltage (V_{on}) for a forward bias sweep is higher than the latch-down voltage (V_{off}) for a reverse bias sweep. The device remains latched-up with a large amount of current for as long as the positive-feedback process continues; therefore, the device does not turn off until the voltage falls below V_{off} .

The clear distinction between the previously reported punchthrough diode and the proposed latch-up diode is shown in Fig. 2(b). The maximum selectivity of the punchthrough diode is approximately 10^3 with 1 MA/cm^2 of J_{max} . The proposed latch-up diode outperforms the punchthrough

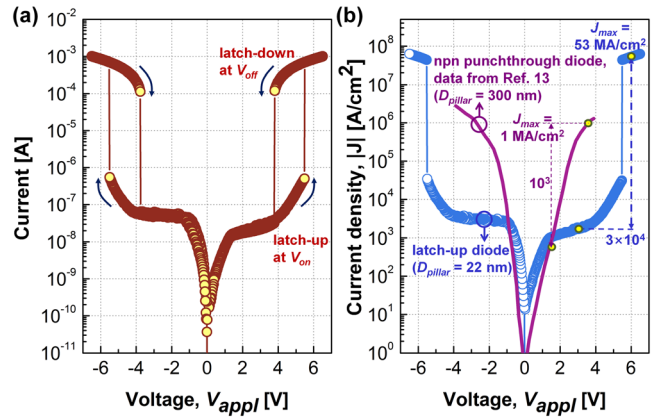


FIG. 2. (a) Hysteric I - V characteristics measured with a latch-up diode. The structural symmetry is attributed to the symmetrical and bidirectional characteristics. The hysteric loop is in the counterclockwise direction, which means that the latch-up voltage (V_{on}) is higher than the latch-down voltage (V_{off}). (b) The overlay curves of both the previously reported punchthrough diode and the proposed latch-up diode. The notable distinction between them is the selectivity and maximum current density.

diode. Its maximum selectivity is 3×10^4 with 53 MA/cm^2 of J_{max} , which are approximately 10 times greater than those of the punchthrough diode. The latch-up phenomenon allows a sudden increment in the current at a specific voltage (V_{on}), which facilitates a higher selectivity. Furthermore, higher J_{max} is feasible, when compared with the punchthrough diode, owing to the amplified current by the current gain (β). Consequently, excellent performance of the n-p-n diode can be achieved by adjusting the latch-up mechanism without an elaborate epitaxial process; the Si-based n-p-n latch-up diode, which is fabricated by using the conventional CMOS process, can be a promising candidate for the 1S-1R crossbar array. In addition, Fig. 3(a) shows the time-resolved latch-up behavior of the proposed device as well as the schematic of the measurement system. As can be observed from Fig. 3(a), the latch-up process occurs within 10 ns corresponding to an input pulse (rising/falling times = 3 ns, pulse width = 10 ns). At $V_{appl} = 6\text{ V}$ (for on-state), a turn-on current response at a switching speed 10 ns is observed, while no response is

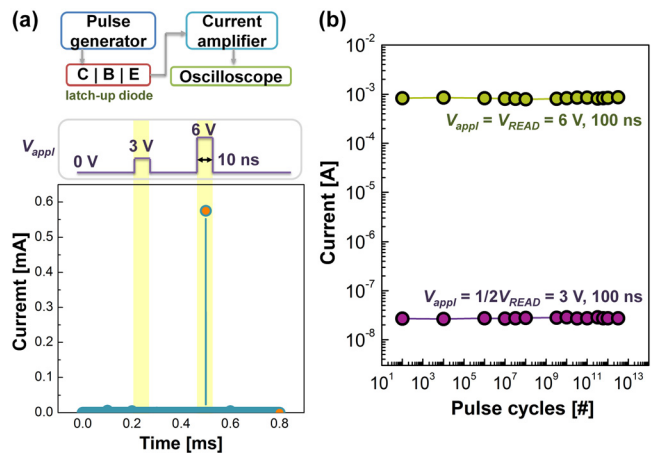


FIG. 3. (a) Time-resolved latch-up behavior of the proposed selector device and schematic of the measurement system. A serially connected current amplifier is used to produce the transient response measurements readable by an oscilloscope. (b) Pulse endurance test of selector device.

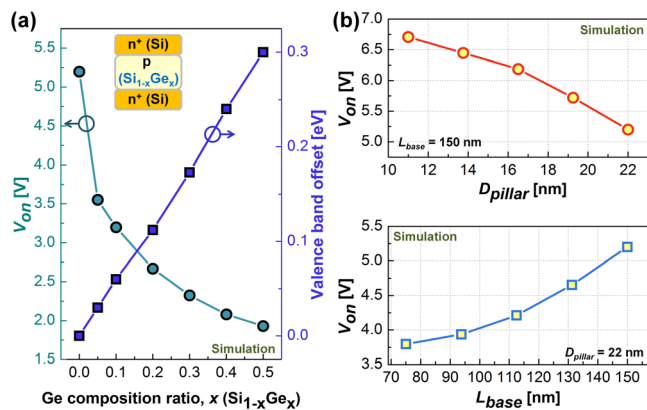


FIG. 4. (a) Concept of bandgap engineering. V_{on} decreases as the Ge composition in the base region increases, because β increases as the valence-band offset increases and M increases at the smaller bandgap. (b) V_{on} versus D_{pillar} and L_{base} . Increments of M and β contribute to lowering V_{on} at shorter L_{base} . However, V_{on} increases as D_{pillar} is reduced owing to decreases in M and β (i.e., non-local effect).

measured at $V_{appl} = 3$ V (for off-state). Moreover, excellent pulse endurance property is confirmed, as shown in Fig. 3(b). A negligible degradation of current at V_{READ} and $1/2V_{READ}$ during the successive 10^{12} pulse endurance test indicates a highly reliable selection property of the proposed device.

One challenging issue with the proposed latch-up diode is its high operating voltage because the latch-up mechanism is governed by impact ionization. Nevertheless, the latch-up voltage (V_{on}) can be reduced by optimizing the latch-up condition. If the common-emitter current gain (β) and multiplication factor (M) are increased, V_{on} can be reduced. Current gain (β) is increased when the hole diffusion current is suppressed by the valence-band offset at the emitter-base junction. Moreover, the smaller energy bandgap of the base enhances the impact ionization rate at the given voltage. Therefore, a higher valence-band offset at the emitter-base junction with a smaller bandgap of the base can decrease V_{on} . Figure 4(a) shows the numerical device simulation (TCAD) results when Si_{1-x}Ge_x is introduced as a base material. As the Ge fraction in the Si_{1-x}Ge_x alloy increases, the bandgap of the base region reduces. Accordingly, the required latch-up voltage can be reduced by the enhancement of both M and β . In addition, V_{on} is analyzed for different device dimensions, as shown in Fig. 4(b). A shortened base length (L_{base}) reduces V_{on} by virtue of the enhanced β ; however, the narrowed D_{pillar} acts adversely on the decrement of V_{on} because the non-local effect can decrease the impact ionization rates (i.e., M value), even though a narrow pillar causes reduction in the hole diffusion current.^{17,18}

In conclusion, a vertical latch-up based n-p-n diode was proposed for a bipolar RRAM selector. J_{max} of >50 MA/cm² and a selectivity of 3×10^4 were observed, which are attributed to the introduction of the latch-up phenomenon. These values were higher than those observed in the previously reported n-p-n punchthrough diode. The performance of the latch-up diode was measured with a size of 22 nm, which

confirms the scalability of the proposed device. The optimization of the turn-on voltage was investigated by numerical device simulation, which ensures the promising potential of the proposed selector device. In comparison with the other types of selector devices, the proposed latch-up based n-p-n selector device achieved excellent performance, particularly high selectivity and maximum current density.

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