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Unusual instability mode of transparent all oxide thin film transistor under dynamic bias condition

Himchan Oh,[a] Chi-Sun Hwang, Jae-Eun Pi, Min Ki Ryu, Sang-Hee Ko Park, and Hye Yong Chu

Next Generation Display Research Department, Electronics and Telecommunications Research Institute, Daejeon 305-700, South Korea

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We report a degradation behavior of fully transparent oxide thin film transistor under dynamic bias stress which is the condition similar to actual pixel switching operation in active matrix display. After the stress test, drain current increased while the threshold voltage was almost unchanged. We found that shortening of effective channel length is leading cause of increase in drain current. Electrons activate the neutral donor defects by colliding with them during short gate-on period. These ionized donors are stabilized during the subsequent gate-off period due to electron depletion. This local increase in doping density reduces the channel length. © *2013 AIP Publishing LLC*. [http://dx.doi.org/10.1063/1.4821365]

Amorphous oxide semiconductor (AOS) is the one of the most versatile materials in thin film and nano-electronics.[1,2] Among the various applications, AOSs have been intensively researched and developed as a promising active material for thin film transistor (TFT) backplane due to their superior properties compared with amorphous Si (a-Si) and organic semiconductors.[3–5]

Reliability of the device thus has been intensively studied to make those fine features of oxide TFTs meaningful. One of reliability issues remaining is the negative bias instability (NBI) under illumination.[6] Even in this case, many studies have been done to understand the degradation mechanism.[7–9] Several effective methods to improve the stability under this condition have also been reported.[10–12]

However, the switching TFTs are subjected to periodic gate pulse to be turned on and off during the actual operation of active matrix (AM) displays.[13] Reliability issues which are very different from those caused by the static bias stress could occur under this dynamic bias condition. Figure 1(b) shows the typical gate pulse of AM displays. The duty cycle is about 0.01–1% depending on the screen size and resolution of display, and the frequency ranges from 60 to 240 Hz or higher depending on the refresh rate. Thus, the switching TFTs are being turned off most of the time except when they get very short ($\sim\mu$s) on pulse periodically. For example, t_{on} of switching TFTs in the display having 1024 lines and 60 Hz refresh rate is calculated as follows: $t_{on} = (1/60)/1024 = 16.3\ \mu$s.

In this paper, we report unusual instability mode of oxide TFT under the aforementioned pulsed bias stress which mimics the gate line signal in AM displays. The degradation behavior discussed in this letter is quite different from the one observed under the static bias stress.

A top gated amorphous In-Ga-Zn-O (a-IGZO) TFT was fabricated for this study as illustrated in Figure 1(b). The fabrication procedure has been reported in detail.[1,8] All the I-V and C-V measurements and stress test were carried out at room temperature using an Agilent B1500A precision semiconductor parameter with a pulse generator unit.

Prior to the dynamic stress test, effects of the static gate bias stress were investigated. The V_{th} shifts were below 0.3 V by both positive (20 V) and negative (−20 V) gate bias stresses with the identical drain to source voltage (V_{DS}) of 10 V for 10 000 s at room temperature in the dark, meaning that our devices are fairly stable under the bias stress compared with those of other research groups or companies.

Figure 2(a) shows the changes in transfer characteristic with the time while the periodic gate pulse similar to Figure 1(b) (60 Hz frequency, duty cycle = 0.05%, $t_{on} = 8.3\ \mu$s, turn-on voltage (V_{on}) = +20 V, and turn-off voltage (V_{off}) = −20 V) and V_{DS} of 10 V as a data signal were applied. This stress condition was used as the basic case throughout this study and will be called as "dynamic stress" or "pulse stress" without description unless stated otherwise. At first glance, there seem to be no changes in the device characteristics before and after the dynamic stress test. The V_{th} and subthreshold swing are almost same. Only a negligible shift of V_{th} was observed. Thus, one can conclude that the gate line signal does not degrade the switching TFTs. However, we found that the drain current increased with the stress time. The increment in drain current exceeds the level that is expected when considering the negative shift of V_{th}. The plot of field effect mobility in saturation region (μ_{sat}) makes this clear as shown in Figure 2(b). This phenomenon has never been observed when we applied the static gate bias stress.

We can point out three causes for increase in drain current without changes in sub-threshold characteristics: (1) actual increase in bulk mobility of a-IGZO, (2) reduction in parasitic resistance (R_p), including contact resistance between a-IGZO and source/drain electrodes, (3) decrease of effective channel length.

To evaluate the R_p, we used gated-transmission line method (TLM). The total drain to source resistance (R_{tot}) of a TFT operated in a linear region can be expressed as follows:[14]

[a]Author to whom correspondence should be addressed. Electronic mail: fullchan@etri.re.kr

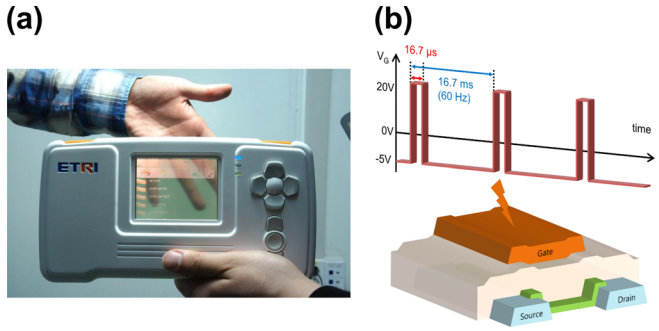

FIG. 1. (a) Augmented reality device adopting see-through display. (b) Gate line signal in active matrix displays and schematic diagram of a top gated staggered type a-IGZO TFT tested in this study.

$$R_{tot} = R_{ch} + R_p, \tag{1}$$

$$= \mu_{FEi} C_g \frac{L}{W}\left(V_{GS} - V_{th} - \frac{V_{DS}}{2}\right) + R_p, \tag{2}$$

where L, W, μ_{Fei}, and C_g are channel length, channel width, intrinsic mobility, and gate capacitance per unit area, respectively. Figure 3(a) shows the R_{tot} values before and after the stress test for various L (40, 80, and 160 μm) measured under the same bias condition ($V_{GT} = V_{GS} - V_{th} = 10$ V, $V_{DS} = 0.1$ V) and identical channel width of 160 μm. By fitting a line to this plot of R_{tot} versus L, we can obtain R_p according to the Eq. (2). The extracted R_p was 6690 Ω for the pristine state and this is comparable with the reported value. We also performed the same procedure to evaluate the R_p of the device which was subjected to dynamic stress. After the pulse stress test, the R_{tot} decreased for all channel lengths as shown in Figure 3(a). However, no positive y-intercept was found unlike the pristine device. Such behavior is often found if effective S/D areas exceed the mask channel length and expand to the center of channel region under gated area like the field effect transistor (FET) having lightly doped drain (LDD). In this case, the reduced channel length should be considered and Eq. (2) becomes

$$R_{tot} = \mu_{FEi} C_g \frac{L - \Delta L}{W}\left(V_{GS} - V_{th} - \frac{V_{DS}}{2}\right) + R_{pg} \tag{3}$$

where R_{pg} is the parasitic resistance in the presence of the doped region under or near the gate, at a certain V_{GS} and ΔL is the difference between mask channel length and effective channel length. We can use the "paired V_{GS}" method to get the ΔL and R_{pg} which was originally proposed for FETs with LDD.[15]

The extracted ΔL and R_{pg} of the stressed device were 4.7 μm and 3085 Ω, respectively, as shown in Figure 3(b). This means that effective channel length became shorter than the mask channel length by 4.7 μm. Note that, this ΔL is averaged value rather than the exact value for the TFT with specific length because we use R_{tot} values of the TFTs with the different channel lengths. The degree of channel shortening is higher in shorter channel TFT due to the larger lateral field, if the bias condition and stress time are same.

Reduction in effective channel length is also confirmed by the capacitance-voltage (C-V) measurements. Figure 2(c) shows the channel capacitance-voltage (C_{ch}-V) curve measured by sweeping the gate voltage while the both source and drain terminals are grounded. After pulse stress test, the capacitance in off region rose significantly while the

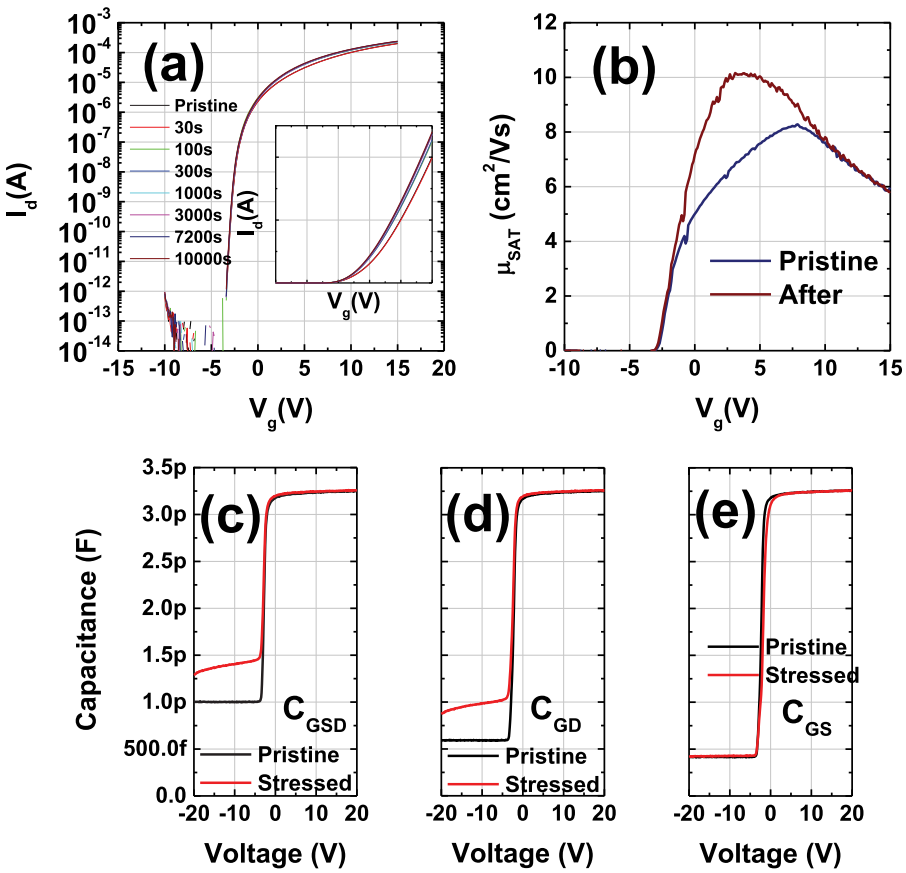

FIG. 2. (a) Evolution of transfer characteristic as a function of the dynamic stress time. The inset shows the same transfer curves in linear scale. (b) Field-effect mobility before and after the stress test. (c) C_{CH}-V, (d) C_{GD}-V, and (e) C_{GS}-V curves before and after the stress test.

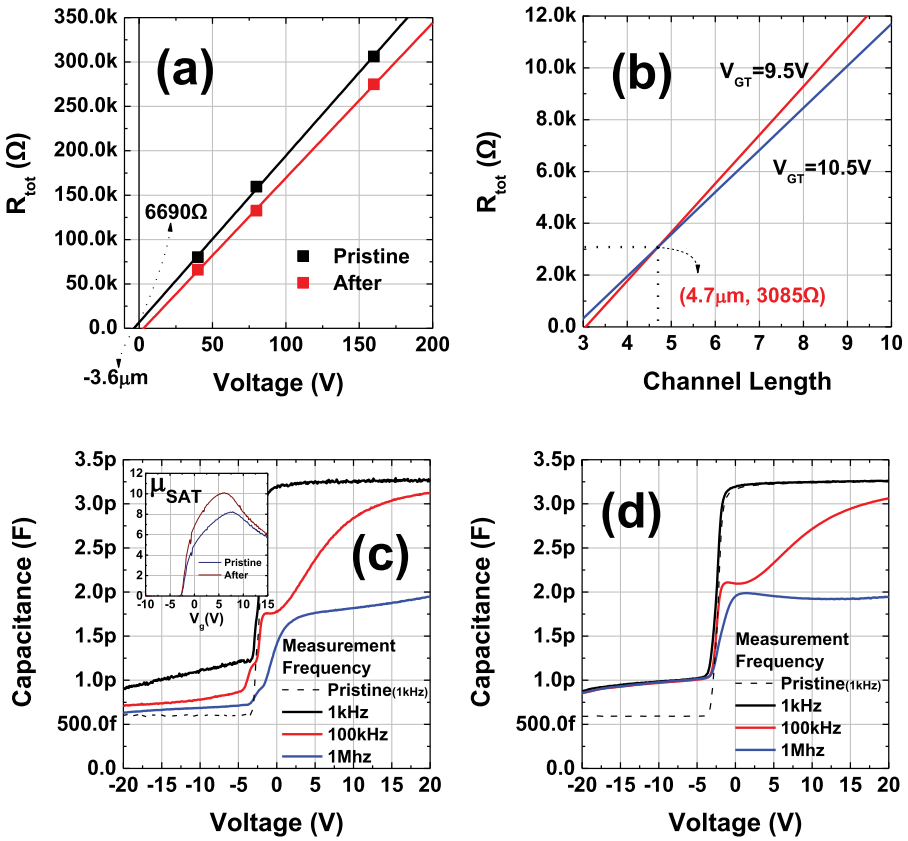

FIG. 3. (a) R_{tot} before and after stress test for various L (40, 80, and 160 μm) measured under identical bias condition ($V_{GT} = V_{GS} - V_{th} = 10$ V, $V_{DS} = 0.1$ V). (b) ΔL and R_{pg} by paired V_{GS} method. (c) C_{GD}-V curves after static drain bias stress ($V_{GS} = 0$ V, $V_{DS} = 20$ V) test, measured at various frequencies and (d) those for the dynamic stress case. The inset in (c) shows the field-effect mobility before and after the static drain bias stress test.

accumulation capacitance was not altered. Figures 2(d) and 2(e) show the gate to drain capacitance-voltage (C_{GD}-V) and the gate to source capacitance-voltage (C_{GS}-V) curves of the TFT with the W/L of 160 μm/40 μm, respectively. The similar change was only observed for C_{GD}-V while C_{GS}-V remained unchanged which means that the degradation started from drain terminal.

The lower level in C_{ch}-V curve comes from the small overlap capacitance between the gate and source/drain electrodes when the a-IGZO is depleted by the gate bias.[16,17] Therefore, the increased C_{GD} in off region means that overlap between gate and drain was extended to channel area under gate. That is, carrier density in a-IGZO near the drain side rose and this resulted reduction in effective channel length. It is noteworthy that such increase in overlap capacitance will cause problems related to the dynamic operation of pixel arrays.[16]

We can calculate the extended overlap area (A_{ext}) from the capacitance in off region which can be expressed as follows, if we assumed that whole initial overlap area (A_{ov}) between gate and drain became metallic after the stress test:

$$A_{ov} = L_{ov}W \tag{4}$$

$$C_{GD,off} = C_g(A_{ov} + A_{ext}) \tag{5}$$

$$A_{ext} = \left(\frac{C_{GD,off}}{C_g}\right) - A_{ov} \tag{6}$$

where L_{ov} and $C_{GD,off}$ are overlap length and C_{GD} in off region after stress test, respectively. The L_{ov} is 5 μm for all the tested devices. Then, the calculated A_{ext} from $C_{GD,off}$ (at $V_{GD} = -20$ V) in Figure 2(d) is 1330 μm^2. As the simplest case, if the overlap area was extended evenly along the width direction, then the extended length is given by $A_{ext}/W = 1330\ \mu m^2/160\ \mu m = 8.3\ \mu m$.

The ratio between the drain currents before and after the stress test ranges from 1.2 to 1.4 for V_{GT} from 2 V to 10 V. Meanwhile, the ratio of effective channel length before and after is $40/(40 - 8.3) = 1.3$ using the calculated reduced channel length. Both ratios are very similar to each other. Thus, it can be said that the increase in drain current mainly comes from reduction in effective channel length.

Two mechanisms can be responsible for channel shortening phenomenon: (1) actual increase of doping concentration, (2) induction of free electrons by trapped holes at the a-IGZO/gate insulator (GI) interface. We found that the first one is the case for this study, which has never been reported so far. The latter one was reported by Seo *et al.* and Huang *et al.* with totally different stress conditions from that of this study.[17,18] They applied high drain bias (+20 V) and low gate bias (0 V) statically. Similar increases in C_{GD} and μ_{sat} were observed by this stress condition as illustrated in Figure 3(c). In contrast, a clear difference between the two mechanisms is found by measuring the C-V characteristic with varying the AC frequency. Figures 3(c) and 3(d), respectively, show the C_{GD}-V curves measured at different frequencies after the static drain bias stress and the dynamic stress. Large frequency dispersion is found for drain bias stress case as also reported by Seo while there is negligible change along the frequency variation in the dynamic stress case.

When the frequency is so low (~1 kHz), that the capture-emission rates of holes at interface traps can keep up with the small-signal AC variation, the interface trap charge can be exchanged with the a-IGZO.[19] Consequently, the trapped holes and electrons induced by them can contribute

to the C_{GD}. At higher frequencies, interface traps cannot follow up the small-signal AC change. Contribution of trap charges to capacitance hence reduced in this case. Therefore, it is plausible that the channel shortening phenomenon by the large drain bias stress is caused by the positive charge trapping according to the large frequency dispersion in C_{GD}. On the other hand, unlike the interface traps, donors (shallow centers) and electrons from them are insensitive to AC frequency because they are situated close to conduction band minimum (CBM) or above it. Thus, C_{GD} after the dynamic stress test remained raised level even at 1 MHz frequency.

We believed that current flow to drain terminal by short on pulse provides energy to activate deep donor states. To clarify the role of current flow, two different types of pulsed drain bias were applied during the dynamic stress test as shown in Figures 4(a) and 4(b). One is the synchronized to gate signal, that is, when the gate voltage rises, drain bias goes up to 10 V at the same time and down to 0 V while the gate is turned off. The other is the desynchronized case as also depicted in Figure 4(b). The increase in μ_{sat} is only observed for the synchronized configuration while there is no change in the desynchronized case due to the lack of current as shown in Figure 4(b).

Meanwhile, the high electrical field near drain terminal due to the large gate and drain bias can be regarded as a reason for increase in carrier density. For example, one can think that holes could be injected to GI from drain, and they might induce additional electrons. In order to verify whether this is the case or not, the dynamic stress is applied to metal-insulator-semiconductor-metal (MISM) planar stack fabricated on the same glass substrate together with the TFTs as depicted in Figure 4(c). This MISM stack has identical configuration with the drain part of the TFT. The gate signal and static drain bias were applied to top and bottom electrode, respectively. As a result, there was no change in the C-V characteristics as shown in Figure 4(c) proving that the high field only cannot increase the carrier density and current flow is essential to bring such change. Note that this is also confirmed from the negligible change in μ_{sat} by the desynchronized drain pulse with gate signal because only high vertical electric field is induced in the gate off period without current flow during the gate on-pulse.

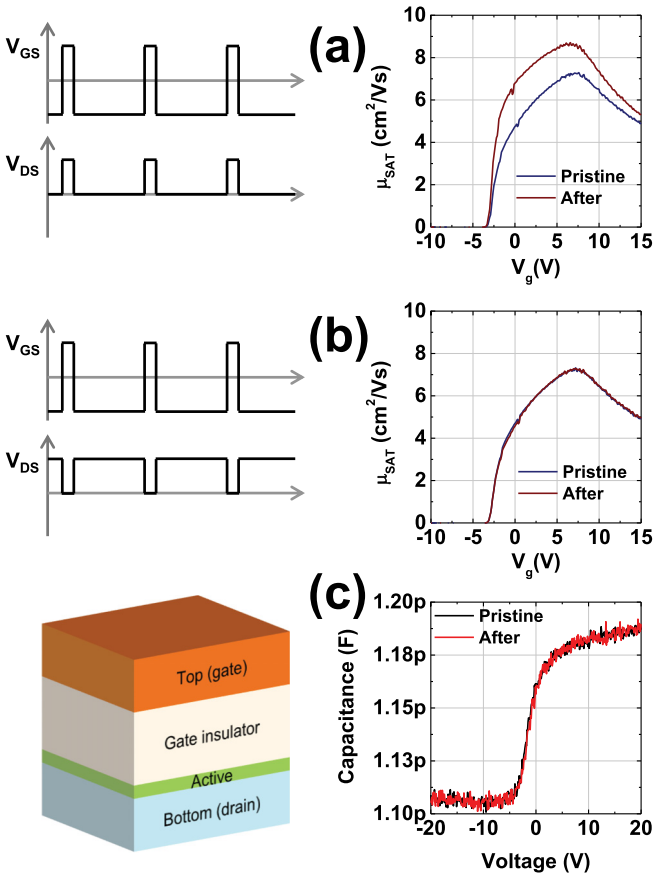

FIG. 4. (a) Diagram of pulsed drain bias synchronized to gate signal and change in field-effect mobility under this stress condition. (b) Those for desynchronized configuration. (c) Schematic diagram of MISM stack and C-V curves before and after the dynamic stress test.

We believe that oxygen vacancies (V_O) are the main defects respond to dynamic bias stress. It is well known that V_O form deep donor states in high density due to low formation energy, which has been underpinned by the first principle calculation and the experimental results.[20–22] Because most V_Os are situated in deep energy level, thermal excitations of electrons from these states to conduction band are hard to occur at room temperature or at device operating temperature. Thus, donation of free electrons to channel is insignificant. However, the ionizations of V_Os to V_O^{2+}s of upper energy level close to CBM or above it are possible by additional energy like photon.[7,8,20] In this study, such energy can be provided to V_Os by the collisions of fast electrons with them during the short on pulse. Ryu *et al.* suggested that V_O^{2+}s can survived without electron capture, maintaining the shallow level due to amorphous nature of a-IGZO after negative bias illumination stress (NBIS) test.[7] We believe that similar transition of donor defects happens during the dynamic stress test and V_O^{2+} donates the electron to conduction band.

Although V_Os are once ionized by the impact of electrons, they tend to be neutralized by capturing the electrons unless the Fermi-level is kept lowered. Namely, V_O^{2+} can be further stabilized under electron depletion condition.[8,9] We expect that V_{off} subsequent to on pulse in gate signal stabilizes the V_O^{2+} by depleting the electrons. The necessity of off pulse is clearly confirmed by raising the V_{off} from −20 V to 0 V. Increment of μ_{sat} is decreased as V_{off} reaches close to 0 V, and finally, there was no change when we applied V_{off} of 0 V. Because the gate bias controls the Fermi level of a-IGZO, the Fermi level is raised as the gate bias reaches to 0 V. Then, V_O^{2+}s become more unstable than V_Os due to their formation energy elevated close to that of their neutral state. Consequently, local increase of carrier density cannot be observed.

Figure 5 illustrates the degradation mechanism of the dynamic bias stress based on the discussions so far. At first, accelerated electrons by the drain bias collide with V_O to ionize them as V_O^{2++} (Figure 5(b)). The V_O^{2++}s are remained its charged state by virtue of the lowered Fermi level in the subsequent off period (Figure 5(c)). Repetition of these two steps causes the local increase in doping density near drain side (Figure 5(d)).

In conclusion, we report the degradation behavior of transparent TFT under the dynamic bias stress which mimics the gate line signal in active matrix displays. Through the TLM method and the C-V analyses, it is found that effective

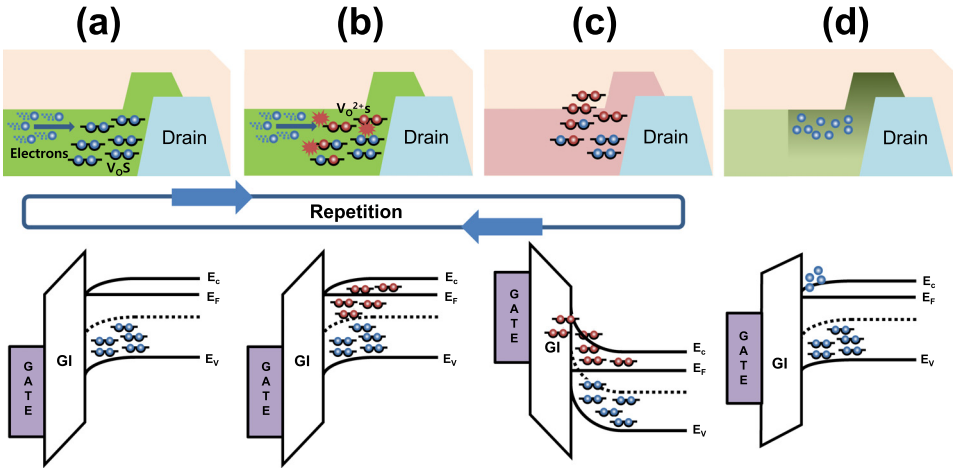

FIG. 5. Diagrams illustrate proposed degradation mechanism by the dynamic stress. (a) Electrons that flow to drain terminal. (b) Collisions between electrons and V_OS which cause ionization of V_OS to V_O^{2++}. (c) Stabilization of V_O^{2++} during the off period. (d) Local increase in doping density near drain side after the stress test.

channel length is shortened from the original channel length after the stress test. The local increase in carrier density occurs by the actual rise in doping concentration rather than by the holes trapped at the a-IGZO/GI interface, which is confirmed through the different frequency dependencies in C_{GD} according to degradation mechanism. The current flow is essential to activate the deep donors by supplying the external energy through the collision of accelerated electrons with donor defects.

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