A 6 bit 2 GS/s Flash-Assisted Time-Interleaved (FATI) SAR ADC with Background Offset Calibration

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***Abstract*— A power-efficient and speed-enhancing technique for time-interleaved (TI) SAR ADCs that is assisted by a low-resolution flash ADC is presented. The 3 b MSBs achieved from a flash ADC at every clock save two decision cycles from every SAR ADC channel, resulting in a reduced number of time interleaving channels with a total 27% energy saving compared with the energy consumption of a conventional TI SAR ADC . A prototype 6 b 2 GS/s ADC in a 45 nm CMOS consumes 14.4 mW under a 1.2 V supply and achieves 5.2 ENOB$_{Nyq}$ with a background offset calibration.**

I. Introduction

Apart from the trend that TI SAR ADCs have a high conversion rate with low power consumption, the linearly increasing number of channels proportional to the conversion speed increases the power consumption as well, and also raises the issue of calibration of a complicated mismatch between channels [1], which makes the design and debugging difficult. The pipeline-based speed enhancement of a single channel [2] can reduce the number of TI channels, but the power consumed by residue amplifiers can be a considerable overhead. The proposed design in this paper reduces the number of TI channels as well as the total power consumption by utilizing a power-efficient, low-resolution flash ADC based on the concept introduced in [3].

While the offsets of every comparator in flash and SAR ADCs are calibrated in the background to track the temperature-dependent slowly-varying component, the gain and timing mismatches are taken care of by simple circuit techniques to reduce the circuit complexity considering the target specification.

II. Flash-Assisted Time-Interleaved SAR ADC

Fig. 1 demonstrates the architecture of the proposed 6 b 2 GS/s Flash-Assisted Time-Interleaved (FATI) SAR ADC and its timing diagram. For simplicity, the architecture is described with a single-ended version. The ADC is basically composed of a 3 b 2 GS/s flash ADC and four channels of 6 b SAR ADCs. Upon the 3 b MSBs from the flash ADC, each SAR ADC resolves the remaining 3 b LSBs at a 500 MS/s rate. In order to maximize the conversion speed, no redundancy was utilized between the flash and SAR ADCs. Instead, the offset of every comparator was calibrated in the retire-and-replace manner [4]. Thus, a total of five channels of SAR ADCs are involved for TI

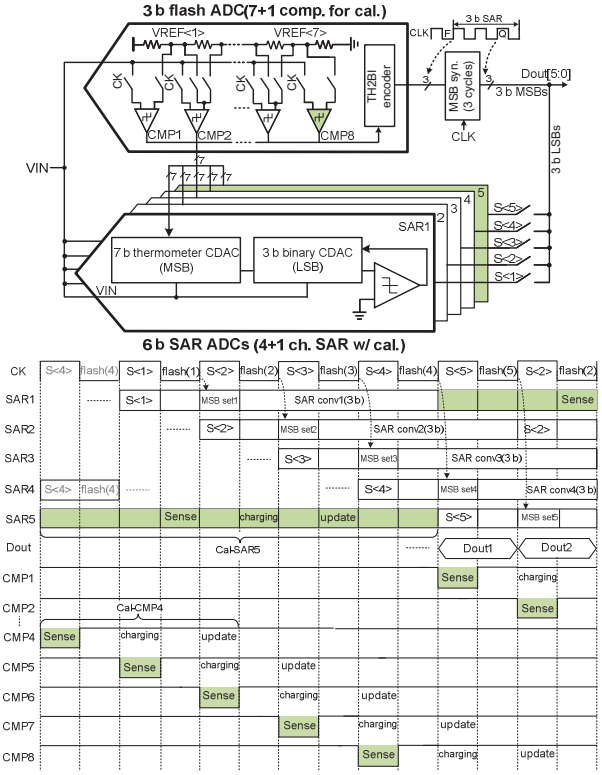

Fig. 1. The proposed FATI-SAR ADC block(simplified for explanation) and timing diagram.

and so is one additional comparator in the flash ADC. As described in the timing diagram, at the first cycle of clock CK (noted as S<1>), the flash ADC and the first channel SAR ADC (SAR1) sample the input simultaneously while the retired SAR5 stays in an offset calibration mode which was started from S<4> (gray colored), and the remaining channels are in the code decision mode with previously sampled inputs. During the following CK = 0 period (flash(1)), the flash ADC generates 3 b MSBs and transfers them to SAR1 (MSB set1). Since the SAR ADC has a 6-bit capacitor-DAC (CDAC) with a unary-structured MSB segment, the 7-digit thermometer code from the flash ADC is directly loaded to the high-speed SR-latch in the SAR ADC. While the flash ADC samples the next input with the SAR2 in S<2> cycle, SAR1 begins a typical

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Table I. Energy comparison of 6 b ADCs.

Architecture	6 b TI SAR	6 b FATI SAR
# of SAR channels	6	4
Required # of cycles/channel	6	4 ($1_{\text{for flash}} + 3_{\text{for SAR}}$)
Single channel energy(E)	1	1.09 ($0.3_{\text{for flash}} + 0.79_{\text{for SAR}}$)
Total energy(E x # of ch.)	6(E_{SAR} x 6ch)	4.36($E_{flash\text{-}SAR}$ x 4ch)
Energy saving@2GS/s	none	27% energy reduction

SAR operation to resolve the remaining 3 b LSBs in a 1 b/cycle manner. In this way, the completed 3 b LSBs from the SAR1 and the delayed 3 b MSBs from the flash ADC are added to generate the final 6 b output, Dout1, in S<5>, and with that, the entire ADC provides a 6 b conversion result at every cycle of CK. After completing one cycle of offset calibration (denoted as Cal-SAR5 in Fig. 1), SAR5 replaces SAR1, and SAR1 enters an offset calibration mode. In this way, the offset of all SAR ADCs are calibrated in a round robin way. The comparators in the flash ADC do a similar calibration by properly alternating their references as in [4].

The energy efficiency of the FATI SAR ADC architecture can be compared to a conventional TI SAR ADC. While conventional 6 b TI SAR ADC requires at least six cycles of a sample-rate clock per channel (in this work, the second half of the last conversion cycle is utilized for the next input sampling) and a total of six time-interleaved channels are required, the proposed architecture requires only four cycles for each SAR ADC and four channels of SAR ADCs are used with a single low-power 3 b flash ADC. The quantitative energy comparison at a same conversion-rate is shown in Table I. The energy models of the flash and SAR ADC basically follow the models used in [5] including some modifications with reflection of the real circuit implementation, such as the merged capacitor switching scheme [6] and the dynamic comparator without a preamplifier. The energy consumed in converting a sampled input into a 6 b output was estimated as follows: The two clock cycles reduced from the single channel SAR ADC save the energy by 33% and 38% from the comparator and DAC switching, respectively, resulting in 21% energy saving from the 6b SAR ADC. However, since an additional 3 b flash ADC is utilized that consumes 30% energy of the 6 b SAR ADC, the energy consumed in converting one sample into 6b digital is 1.09 times higher than that of a single-channel 6b SAR ADC. Nevertheless, because the proposed FATI SAR ADC has only four channels of SAR ADCs while the typical TI SAR ADC structure requires six, the total energy consumed by the FATI SAR ADC in A/D converting one sample to 6b digital is estimated to be 73% of the energy consumed by the conventional 6b TI SAR ADC. The design in this work has an additional channel of SAR ADC for the back ground calibration. However, the additional power consumed by the SAR ADC in the calibration mode is negligible owing to the comparator-only and slow operation (refer to Fig. 4).

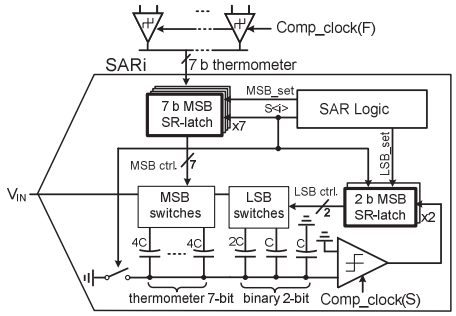


Fig. 2. 6 b SAR ADC block diagram.

III. Circuit Implementation

A. 3 b Flash ADC

The flash ADC shown in Fig. 1 has 8 comparators with bottom-plate sampling networks, a thermometer-to-binary encoder (TH2BI), and an MSB synchronizer (MSB syn.) which synchronizes the 3 b MSBs with the 3 b LSBs from the SAR ADC. The reference voltages for each comparator are defined by a resistor string. The offset calibration timing of the flash ADC with the retire-and-replace manner is shown in the lower half of Fig. 1(b). In order to replace the comparator that is in the calibration mode, each comparator has extra reference switches. When CMP1 is in the calibration mode, the other 7 comparators are connected to the one step upper references of their own so that CMP2 can operate as CMP1 and so on. In the same way, all comparators enter the calibration mode in order.

B. 6 b SAR ADC

A single-channel 6 b SAR ADC that is assisted by a flash ADC is designed for a 500MS/s conversion rate (Fig. 2). Each SAR ADC has a capacitor-DAC, a dynamic comparator, a 3 b shift-register for SAR control (SAR Logic), seven SR-latches for thermometer-coded MSB control (MSB SR-latch) and two SR-latches for LSB control (LSB SR-latch). The CDAC is composed of seven 4C MSB capacitors controlled by the 7 b thermometer code and three binary-weighted LSB capacitors.

The flash and SAR ADCs operate at a 2 GHz internal clock. In order to secure sufficient CDAC settling, the proposed SR-latch is utilized for controlling both the 7 b thermometer-coded CDAC and the 2 b binary-coded CDAC without any switch control logic. This switching-logic-free fast SAR design is similar to the technique used in [7], in principle, but different structures of CDAC and switch configurations were used (note that all switches for CDAC control were implemented with NMOS only in this design).

The proposed SR-latch is shown in Fig. 3. The SR-latch, which is based on a cross-coupled inverter pair, has two pairs of parallel NMOS switches (M_3 – M_6) for output reset and two series PMOS switches (M_1, M_2) to eliminate static current during the reset period. M_3 and M_6 are used to reset the SR-latch in the ADC input sample phase (S<i> = 1) in order to turn

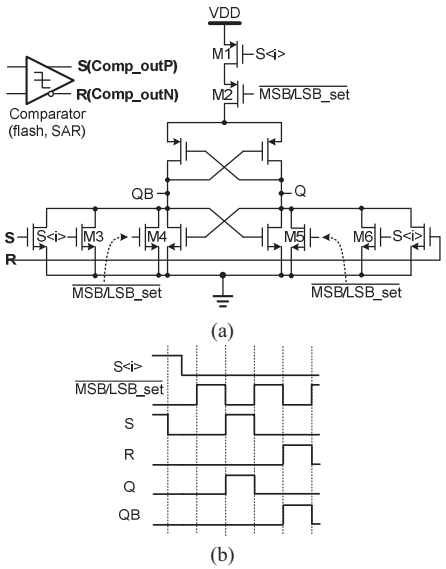


Fig. 3. The proposed SR-latch with dual reset capability (a) block and (b) timing diagram.

off the reference switches of CDAC, and M_1 cuts off the static current path. After the input sampling, SR-latches remain in reset state by M_4 and M_5 until its corresponding capacitor needs to be controlled, and in that phase, M_2 prevents the static current. When the SR-latch is enabled (S<i> = 0 and $\overline{\text{MSB/LSB\_set}}$ = 0), the SR-latch works as a typical one (Fig. 3(b)).

C. Solutions for Mismatches between Flash and SAR ADCs

The circuit for the comparator offset calibration is implemented as shown in Fig. 4, for both the flash and SAR ADCs. During the offset calibration mode, the original differential inputs connected to the CDAC are tied together for a zero input condition. For low-power consumption and fine offset calibration, a charge-pump-based offset tracking method was used. To reflect the feedback information from the charge-pump, the comparator has an additional input pair. The ratio of the hold capacitor (C_{CAL}) and the update capacitor in the charge-pump (C_{Update}) was chosen to be C_{CAL} : C_{Update} = 1000:1 for 0.1 LSB-level offset accuracy. The offset correction was conducted through three clock cycles of offset polarity sensing, C_{Update} charging/discharging, and C_{CAL} updating. Since the charging/discharging and updating can be conducted simultaneously with the typical comparator's decision operation, comparators in the flash ADC needs to be retired only during the offset polarity sensing period as denoted in Fig. 1(b).

The timing skew between the flash and SAR ADCs was minimized by using a single sampling clock (CLK) for every channel with channel enable signals (EN<1:5>), as Fig. 5 illustrates. In order to reduce the effect of the logic delay mismatch of the AND gates utilized for the channel enable operation, the sampling clock, CLK, was designed with a sharp transition slope. Owing to the excellent capacitor matching in the given process, the gain mismatch problem between the flash and SAR ADCs was resolved by the bottom-plate sampling networks in both ADCs.

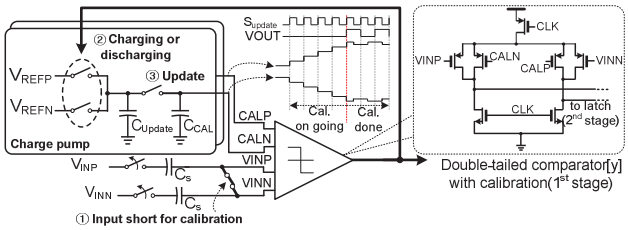


Fig. 4. Charge-pump-based background offset calibration [8].

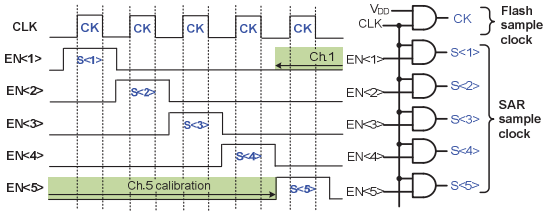


Fig. 5. Flash (CK) and SAR(S<1:5>) sample clock generation.

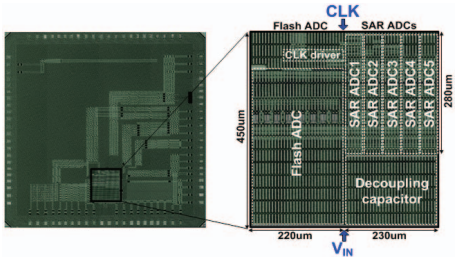


Fig. 6. Chip photograph.

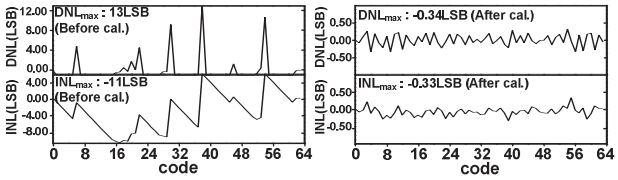


Fig. 7. Measured DNL/INL. (Before cal./after cal.)

IV. Measurement Results

The prototype ADC fabricated in a 45 nm CMOS occupies 0.16 mm^2 (Fig. 6). The core of the ADC including the calibration block occupies 450µm x 450µm. The size of the flash ADC is 450µm x 220µm, and the size occupied by the 5 channel SAR ADCs is 280µm x 230µm. To minimize the sample-time skew, the flash and SAR ADCs were symmetrically placed with respect to the input (V_{IN}) and the clock (CLK) signals.

Owing to the background offset calibration, both the DNL and INL were improved to ±0.34 LSB-levels from the 13 LSB (DNL) and -11 LSB (INL) as shown in Fig. 7. The improved DNL and INL measurement prove that the offset and gain mismatches between the flash and SAR ADCs were efficiently

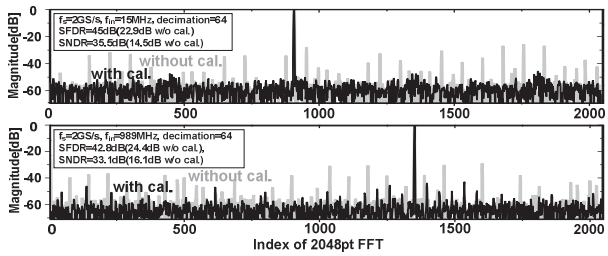
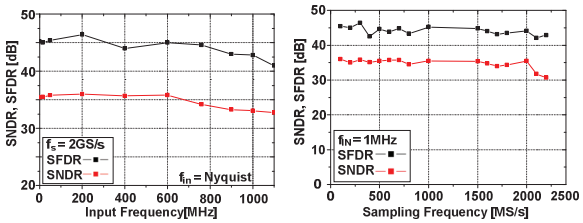


Fig. 8. Measured FFT waves at 2 GS/s. (fin = 15 MHz/989 MHz.)



(a) (b)

Fig. 9. Measured SFDR/SNDR (a) at 2 GS/s under 1.2 V from 1 MHz to 1.2 GHz input and (b) from 100MS/s to 2.2GS/s with the 1MHz input.

suppressed. The FFT result with a 15 MHz input at a 2 GS/s rate also proves this with low harmonic tones (Fig. 8). At a Nyquist-rate input, SFDR and SNDR were 42.8 dB and 33.1 dB (5.2 ENOB), respectively. The residual timing skew error, despite the scheme shown in Fig. 5, is observed by the tones. Nonetheless, Fig. 9(a) shows that the ENOB maintains higher than 5 up to 1.2 GHz input frequency, which indicates the residual timing skew is less than 3.5 ps (rms) based on the estimation in [9]. Fig. 9(b) plots the measured SNDR and SFDR as a function of the sampling frequency at a 1 MHz input. The SNDR stays above 30 dB up to the conversion speed of 2.2 GS/s. The power consumed by the dynamic comparators and the resistor string in the flash ADC is 5.1 mW, and the digital power consumption including the calibration logic and the clock driver is 9.3 mW. The total power consumption is 14.4 mW under a 1.2 V supply and at a 2 GS/s conversion rate (Table II). Table III compares this work with previous high-speed, low-to-medium resolution TI ADCs (with 6 – 8 b resolution) that have background calibration schemes. The prototype ADC shows a competitive FOM of 195 fJ/conversion-step owing to the power-efficient high-speed TI operation assisted by a simple flash ADC.

V. Conclusion

This paper presents a FATI SAR ADC architecture proposed for high speed A/D conversion. The low-resolution low-power flash ADC reduces the conversion cycles from the TI SAR ADCs, and time-interleaving could be realized with a reduced number of channels. This enables high speed A/D conversion with reduced hardware and power overheads. The offset mismatch between ADCs was removed with background calibration. The gain and timing skew mismatch between the flash ADC and SAR ADCs and that between the SAR ADCs were reduced by an adequate sampling network design without redundancy. The operation of the proposed architecture has been proved by the 6 bit 2 GS/s ADC.

Table II. Performance summary.

Process		45nm
Supply		1.2 V
Resolution		6 b
Sampling rate		2GS/s
Power	Analog	5.1mW
	Digital	9.3mW
	Total	14.4mW
DNL		- 0.34 ~ 0.33 LSB
INL		- 0.33 ~ 0.33 LSB
SFDR		42.8 dB @ f_{in}=989MHz
SNDR		33.1 dB @ f_{in}=989MHz
Core area		0.16mm^2
FOM		195fJ/Conv-step

Table III. Performance comparison with background calibrating TI ADCs.

TI ADC with BG-calibration	ISSCC 09, Alpman	ISSCC 09, Liu	JSSC 10, NaKajima	This work
Architecture	TI-SAR	TI-SAR	TI-folding	FATI-SAR
Technology[nm]	45	130	90	45
Resolution[bit]	7	8	6	6
Fs[MS/s]	2500	600	2700	2000
# of channles	16	10	2	4
Calibration type	offset, gain	offset, gain	offset	offset
Supply[V]	1.1	1.2	1	1.2
SNDR[dB]	35.5	47	36.5	35.5
SNDR[dB](ENOB) @Nyquist	34	43	33.6	33.1
Power(mW)	50	30	50	14.4
Area(mm^2)	1	1.1	0.36	0.16
FoM(J/Conv.step) @ Nyquist	480f	340f	470f	195f

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