Highly Reliable M1X MLC NAND Flash Memory Cell with Novel Active Air-gap and p+ Poly Process Integration Technologies

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Abstract

Our Middle-1X nm MLC NAND (M1X) flash cell is intensively characterized with respect to reliability and manufacturability. For the first time, the novel active air-gap technology is applied to alleviate the drop of channel boosting potential of program inhibition mode, BL-BL interference is reduced to our 2y nm node level by this novel integration technology. Furthermore, it also relaxes the effect of process variation like EFH (Effective Field oxide Height) on cell Vt distribution. Better endurance and retention characteristics can be obtained by p+ doped poly gate. By optimization of active air-gap profile and poly doping level, M1X nm MLC NAND flash memory has been successfully implemented with superior manufacturability and acceptable reliability.

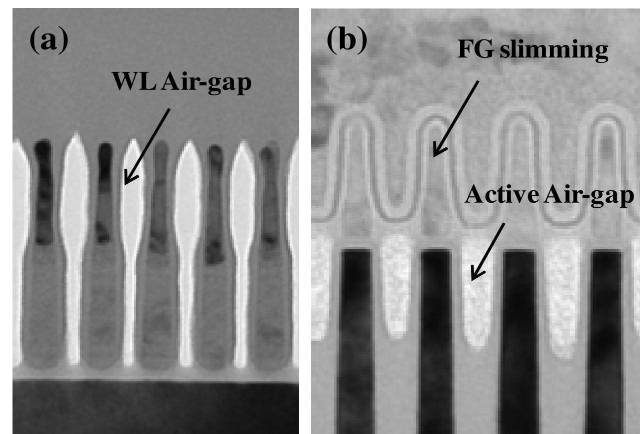

Fig. 1: The Cross-sectional TEM views of the cells along WL (a) & BL (b) direction. Uniform active air-gap is formed successfully.

Introduction

M1X nm floating gate technology had been proposed using ArF immersion QSPT (Quad Spacer Patterning Technology) and word-line (WL) direction air-gap [1]. However, chip size reduction has been demanded continuously, so that the additional bit-line (BL) pitch shrinkage has been required. Because of extremely closed distance between BLs, we have encountered severe problems, such as large BL interference, PGM disturbance caused by boosted potential drop. The active air-gap scheme between BLs is seriously considered [2]. The lack of program Vt with decrease of cell C/R (Coupling Ratio) and reliability degradation also give rise to adoption of p+ doped poly gate (FG & CG). However, the poly depletion issue by adjacent WL's read bias has been appeared differently from n-type poly gate, which causes cell Vt widening. In this paper, these issues are intensively investigated both with mass electrical data and with 3-D simulation work to clarify the mechanism.

Cell Characteristics

(1) Effect of active air-gap

The air-gap between silicon actives was successfully manufactured with WL air-gap as well in middle 1X nm generation as shown in Fig. 1. The similar PGM Vt can be obtained in our device compared with our 2y nm as shown in Fig. 2. BL interference at the same EFH is reduced under 2y nm level, and its dependency with EFH fluctuation is also alleviated by 50% as shown in Fig. 3.

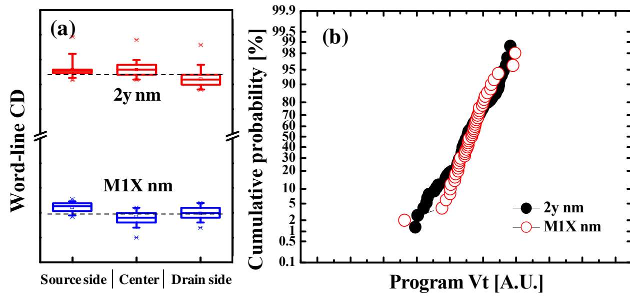

Fig. 2: M1X WL CD variation is precisely controlled with a comparable to 2y nm (a). Uniformity of programmed cell Vt is also almost same as 2y nm technology.

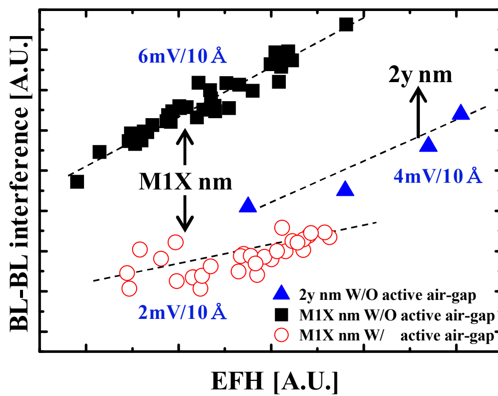

Fig. 3: The process dependency and BL interference are reduced to the half of 2 y nm node level.

In scaled device, the boosted channel potential drop due to interference of adjacent grounded BL makes a severe PGM disturbance problem in M1X nm as shown in Fig. 4. This phenomenon is called '0F' PGM disturbance mode, which is the worst case of various PGM disturbance modes. Fig. 5 shows a great improvement of 0F disturbance about 800mV compared with no active air-gap in same M1X nm. Even though a larger volume of active air-gap controlled by ABH (Air Bottom Height) induces a smaller disturbance Vt shift, it can give rise to retention degradation caused by the tunnel oxide damage. One can make sure that the boosting level is recovered as much as pinned level by active air-gap from the measurement in Fig. 6. The optimized volume of active air-gap is also investigated in Fig. 7. The ATH (Air Top Height) which means the air-gap region above silicon surface has an optimum point in terms of PGM Vt. Over this optimum point, the program e-field shielding effect is dominant and finally Vt is rolled off slightly due to C/R drop, while the BL interference still decreases as shown in Fig. 8.

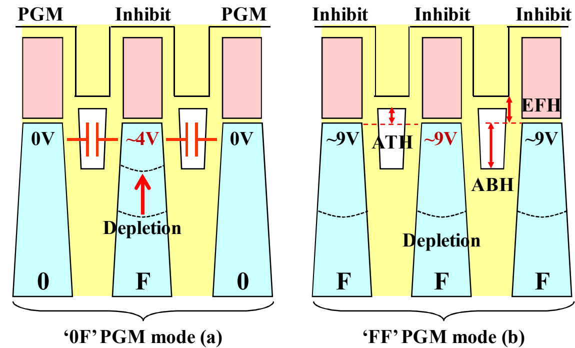

Fig. 4: The Schematic of '0F' and 'FF' disturbance mode. Boosted channel potential of inhibit BL is severely affected by grounded adjacent BL.

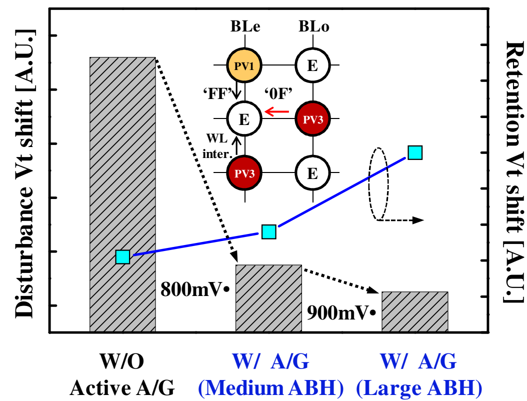

Fig. 5: 0F disturbance of inhibit cell is improved ~800mV with active air-gap technology.

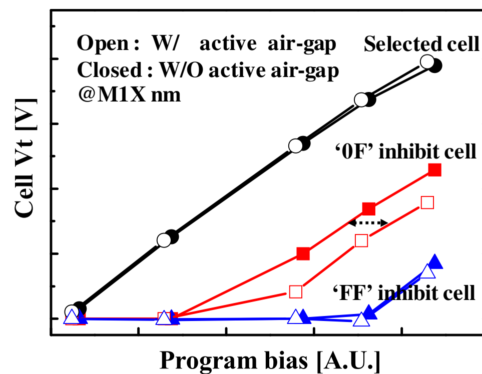

Fig. 6: The improvement of '0F' boosting level with active air-gap.

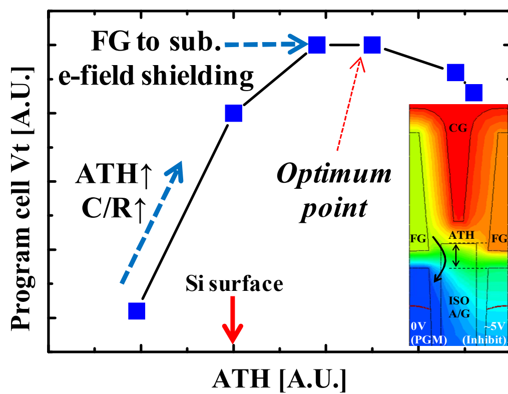

Fig. 7: The optimum volume of active air-gap. The increase of cell Vt is saturated due to e-field shielding.

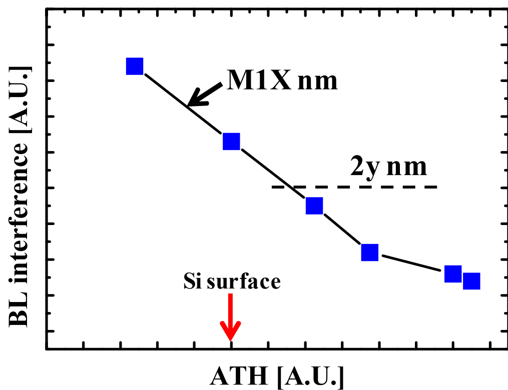

Fig. 8: The BL interference decreases continuously with increased active air-gap top height (ATH).

(2) Effect of p-type poly depletion

Even though WL air-gap diminishes coupling between WLs, the RBS (Read Bias Sensitivity) of M1X cell still bigger than 2y nm as shown in Fig. 9. The RBS means the cell Vt shift for N±1 read bias of 1V. That is, the lower RBS can be obtained at their own higher gate controllability. The p-type doped poly gate has a severe CG depletion problem due to high N±1 read bias and narrow CG valley between FGs as simulated in Fig 10. It makes an abnormal cell Vt drop and widening of cell distribution as shown in Fig. 12. In order to solve this problem and find the actual doping level of real size patterned cell, the RBS change as a function of victim cell status is utilized as an electrical indicator. The remarkable RBS tendency as doping level is found by simulation in the case of four relative FG & CG doping status in Fig. 11.

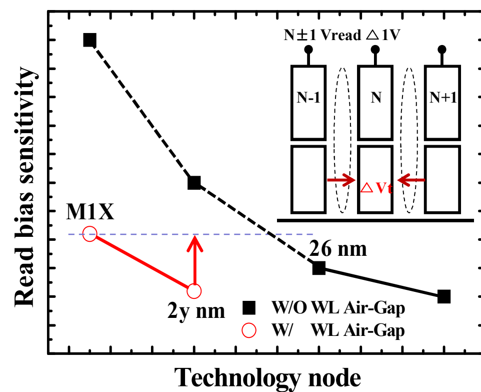

Fig. 9: The WL potential coupling (RBS) is increased with technology shrinkage.

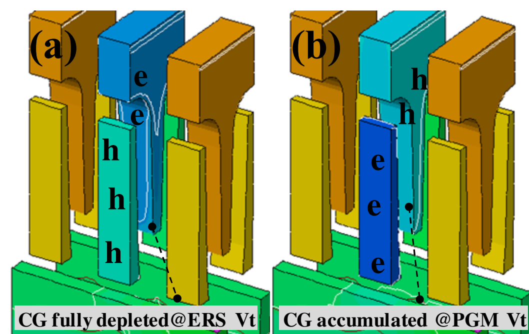

Fig. 10: The simulated depletion results of low CG doping level. The fully depleted CG makes a poor IPD capacitance.

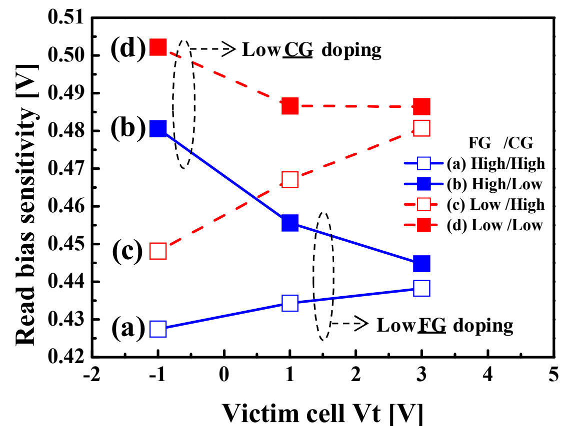

Fig. 11: The 4 cases of RBS change with the victim cell status. The highly balanced doping gate has a low RBS and a less dependency on cell Vt.

The fluctuation of the cell Vt slope with increasing program bias (step variation) is nearly stable to 1 V/V as shown in Fig. 13. It means that highly balanced FG & CG doping make the lowest RBS and curve flat by depletion free status.

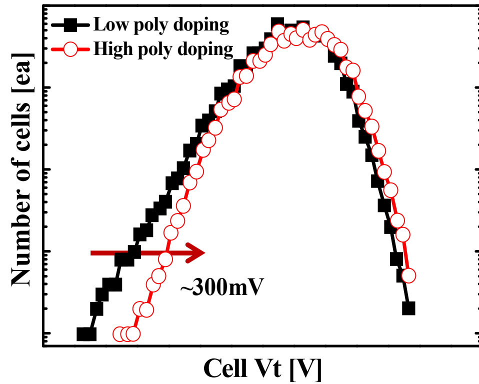

Fig. 12: The narrow cell Vt distribution is achieved at a high p+ poly doping with optimized process.

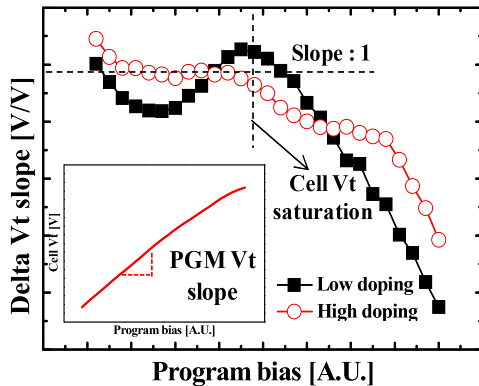

Fig. 13: The incremental step pulse PGM (ISPP) slope is well controlled at a high doping p+ poly gate.

The cycling endurance characteristics are improved by p+ poly gate as shown in Fig. 14. And it has known that the initial hole trap phenomenon makes a smaller cycling Vt shift [3]. The reduced BL interference and p+ doped poly gate scheme make similar initial and 3K cycled cell Vt distribution as shown in Fig. 15. Erase Vt disturbance after cycling is also well suppressed with optimized junction profiles. Therefore, BER (Bit Error Rate) is similar to 2y nm with 3K cycling stress as shown in Fig. 16.

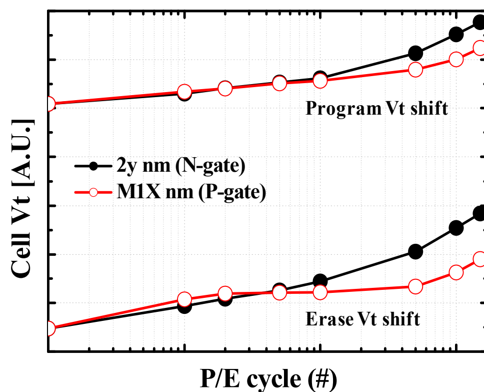

Fig. 14: The p+ poly gate show more improved cycling endurance compared with 2y nm.

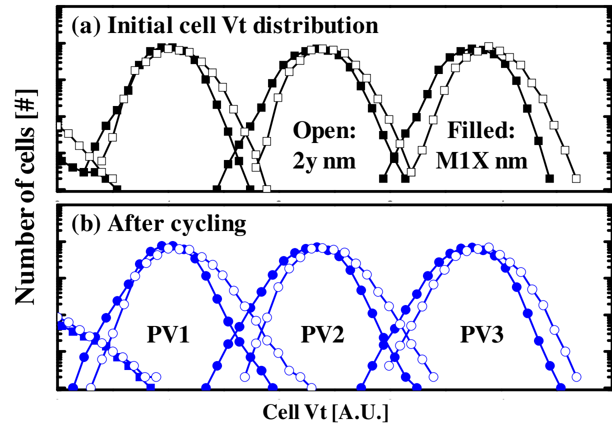

Fig. 15: The cell Vt distribution shows almost same as 2y nm (a). Furthermore, after P/E 3K cycling, the widening of cell Vt is well controlled (b). The erase cell disturbance is improved by optimized junction profile.

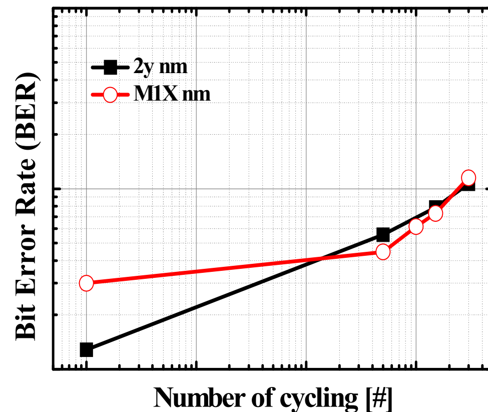

Fig. 16: MSB bit error rate (BER) shows nearly same level compared to 2y nm after P/E cycling.

Conclusion

Highly manufacturable and reliable M1X nm NAND flash memory has been developed by adopting the advanced process integration technologies, such as fine tuned active air-gap and highly activated p-type doped poly gate. By these novel schemes, the scaling limitation in M1X node could be overcome. Finally, we succeeded to implement the mass production of the middle-1x nm NAND flash memory with a similar cell performance and reliability with 2y nm.

References

[1] J. Hwang, et al., "A Middle-1X nm NAND flash memory cell (M1X-NAND) with highly manufacturable integration technologies", *IEEE IEDM Technical Digest*, pp. 199-202, 2011.

[2] S. Lee, "Scaling challenges in NAND flash device toward 10nm technology", *IEEE International Memory Workshop*, pp. 6-9, 2012.

[3] C. Lee, et al., "Physical modeling and analysis on improved endurance behavior of p-type floating gate NAND flash memory", *IEEE International Memory Workshop*, pp. 80-83, 2012.