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10 Gbps Transimpedance Amplifier-Receiver for Optical Interconnects

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A transimpedance amplifier (TIA)-optical receiver (Rx) using two intersecting active feedback system with regulated-cascode (RGC) input stage has been designed and implemented for optical interconnects. The optical TIA-Rx chip is designed in a 0.13 μm CMOS technology and works up to 10 Gbps data rate. The TIA-Rx chip core occupies an area of 0.051 mm^2 with power consumption of 16.9 mW at 1.3 V. The measured input-referred noise of optical TIA-Rx is 20 pA/√Hz with a 3-dB bandwidth of 6.9 GHz. The proposed TIA-Rx achieved a high gain-bandwidth product per DC power figure of merit of 408 GHzΩ /mW.

Keywords : Optical receiver, Transimpedance amplifier, Optical interconnect
OCIS codes : (040.5160) Photodetectors; (060.4510) Optical communications; (200.4650) Optical interconnects; (250.4480) Optical amplifiers

I. INTRODUCTION

In an optical Rx design, the TIA plays the role of a front-end amplifier for amplifying the weak current signals generated from the photodiode (PD) and converting to voltage signal which would be fed to a subsequent block (limiting amplifier or clock and data recovery circuit). The conventional Rx consists of a TIA preamplifier block, limiting amplifier, and the output buffer. There are several works that have reported on 10 Gbps front-end optical receiver designs [1-7]. Bandwidth enhancement techniques using inductive peaking has been proposed [1-5] for designing high data rate operation of an optical Rx. However, an excessive size of the inductor makes the chip big and expensive. An inductorless TIA has been designed in [6], where several shunt feedback TIAs connected in parallel were suggested for bandwidth improvement and chip size reduction. This design method has high power consumption due to the several TIAs deployed. The bandwidth enhancement technique for transimpedance amplifiers using capacitive peaking which has been realized using a single capacitor is a good candidate for small-area TIA design [7]. However, the negative capacitance is directly loading to the input of the TIA, therefore introducing high peaking at the transient response of TIA. We therefore propose an inductorless TIA that functions as an optical Rx, which does not require a limiting amplifier stage, thereby reducing total chip size. In our proposed design, the RGC input stage has been utilized with post amplifying active feedback amplifiers to lower the input capacitance of PD and for bandwidth improvement. A high gain-bandwidth product per DC power figure of merit of 408 GHzΩ/mW is achieved with the combination of passive (resistive) and active (NMOS transistor) feedback components. Thus, the absence of inductors in the proposed TIA-Rx results in a power efficient chip with small size. In this work, a 10 Gbps TIA-Rx chip that operates up to 10 Gbps have been designed and fabricated in a 0.13 μm CMOS technology.

II. THE TIA-Rx CIRCUIT DESIGN

The schematic of the TIA-Rx chip is shown in Fig. 1. The RGC input stage reduces the input impedance by the amount of its own voltage gain, which prevents the input pole from dominating the TIA-Rx bandwidth and reduces the capacitive effect of the PD [8]. Thus, the RGC circuit can be used effectively for CMOS integration as a front-end amplifier.

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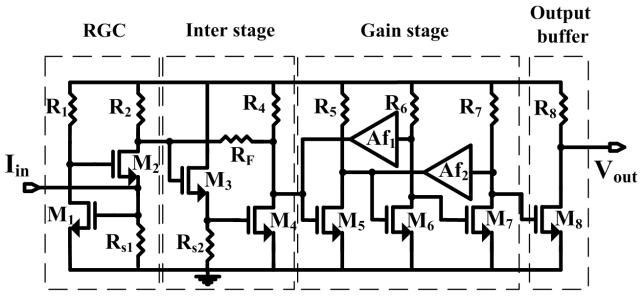


FIG. 1. Schematic of TIA-Rx circuit.

The input impedance of the RGC stage is given as [4]:

$$Z_{IN-RGC} = \frac{1}{gm_2(1+gm_1R_1)} \tag{1}$$

where $1+gm_1R_1$ is the gain of the local feedback and with the product of the common gate stage, it behaves as a large transconductor $Gm = gm_2(1+gm_1R_1)$. Thus, the size of local feedback decides the amount of reduction of input parasitic capacitance effect for bandwidth determination. The RGC peaking frequency in frequency response is given as:

$$f_{peak} = \frac{1}{2\pi R_1(C_{gs2}+C_{gd1})}. \tag{2}$$

At low frequency, the open-loop transimpedance gain of the TIA-Rx is given as:

$$Z_{IN-GAIN} = -(R_2 \| R_F)\frac{gm_3R_{s2}}{(1+gm_3R_{s2})}\left(gm_4 \| gmf_1\right) \cdot R_4\left(gm_5 \| gmf_2\right)R_5gm_6R_6gm_7R_7gm_8R_8 \tag{3}$$

The TIA-Rx is made up of four stages, namely, an input stage (which consists of the RGC); an inter-stage; a gain stage with intercepting active feedbacks; and an output stage (which acts as the buffer). The RGC block is important in the TIA-Rx circuit as it affects the input noise and the stability of the whole TIA-Rx circuit while delivering the input photo current to the output with increased gain. Thus, the design parameters have to be carefully chosen not to interfere with the input impedance for high frequency operation. The transfer function of the RGC input stage is given as:

$$\frac{I_{out}}{I_{in}}(s) = \frac{1+\frac{sC_1}{gm_1}}{\left[1+\frac{s(C_{gs1}+C_{sb1})}{(1+gm_1R_1)gm_2}\right]\left[1+sR_1\left(C_1+C_{gs2}+C_{gd2}\right)\right]} \tag{4}$$

M_3 and M_4 make up the transconductance inter-stage stage of the TIA-Rx, where high frequency operation should be maintained for delivering the converted input current to output voltage for the gain stage. The impedance at the drain of M_2 and M_4 are reduced by factor of $1+A$ by RF shunt feedback and correspondingly, the poles are sped up by the factor, $1+A$. A common-drain (CD) is placed at the drain of M_2 because the capacitive effect on bandwidth is small [8]. The inter-stage isolates the RGC input stage from the gain stage and also adjusts the input dc level from the RGC stage. The transfer function of the inter-stage is given as:

$$\frac{V_{out\_1}}{I_{out}}(s) = \frac{gm_3gm_4R_{s2}R_4R_F'}{1+gm_3R_{s2}}\left(1+\frac{sC_{gs3}}{gm_3}\right)\frac{1}{\left[1+\frac{s(R_F'C_{gs3}+gm_3R_{s2}R_F'C_1^*)}{1+gm_3R_{s2}}\right]}\frac{1}{\left[1+\frac{s\left(C_{gs3}+C_{gs4}\right)}{gm_3}\right]} \tag{5}$$

where R'_F is represented by

$$R_F' = \left(R_1 \| R_F\right)\frac{1}{1+\left(\frac{gm_3R_{s2}}{1+gm_3R_{s2}}\right)gm_4R_4} \tag{6}$$

To increase the overall transconductance of the TIA-Rx to higher output voltage levels, several stages of common-source (CS) amplifying stages have been utilized. However, placing a gain stage consisting of several CS amplifying stages may reduce the bandwidth. Hence, adding the active feedback stages, Af_1 and Af_2, compensate by peaking at high frequencies [9]. The negative active feedback utilized in the gain stage is different from the conventional resistive feedback which avoids the direct resistive load to the preceding transimpedance stage. Moreover, active devices suffer less process variation than passive devices during fabrication. The high-frequency peaking occurs at Af_1 and Af_2 active feedback. The peaking of the first and second active feedbacks is given as:

$$f_{peak,f1} = \frac{1}{2\pi R_4(C_{gd6}+C_{gdf1})} \tag{7}$$

$$f_{peak,f2} = \frac{1}{2\pi R_5(C_{gd7}+C_{gdf2})} \tag{8}$$

The negative active feedback increases the 3-dB bandwidth and thus, the active feedback effects of Af_1 and Af_2 has been included in the transfer function of the gain stage and the equation is given as:

$$\frac{V_{out}}{V_{out\_1}} = \frac{G_5(s)G_6(s)G_7(s)}{1+G_5(s)G_6(s)Gf_1(s)+G_6(s)G_7(s)Gf_2(s)} = \frac{G^3(s)}{1+2G^2(s)Gf(s)} \tag{9}$$

where $G_5(s)=G_6(s)=G_7(s)=GmR/(1+sRC)$, and $Gf_1(s)=Gf_2(s)=Gf(s)=GmfR/(1+sRC)$. By combining equations (4), (5), (6), and (9),we can write the transfer function of the TIA-Rx as:

$$\frac{V_{out}}{I_{in}}=\frac{1+\frac{sC_1}{gm_1}}{\left[1+\frac{s(C_{gs1}+C_{sb1})}{(1+gm_1R_1)gm_2}\right]\left[1+sR_1\left(C_1+C_{gs2}+C_{gd2}\right)\right]}\frac{gm_3gm_4R_{s2}R_4R_F^{'}}{1+gm_3R_{s2}}\left(1+\frac{sCgs3}{gm3}\right)\frac{1}{\left[1+\frac{s(R_F^{'}C_{gs3}+gm_3R_{s2}R_F^{'}C_1^{*}}{1+gm_3R_{s2}}\right]}\frac{1}{\left[1+\frac{s\left(C_{gs3}+C_{gs4}\right)}{gm_3}\right]}\frac{G^3(s)}{1+2G^2(s)Gf(s)} \tag{10}$$

The transimpedance gain of the TIA-Rx can be obtained from equation (10) and is written as follows:

$$Z_T(0)=\frac{gm_3gm_4R_{s2}R_4}{1+gm_3R_{s2}}*\left[R_1\,\|\,\frac{R_F}{1+\left(\frac{gm_3R_{s2}}{1+gm_3R_{s2}}\right)gm_4R_4}\right] \tag{11}$$

The 3-dB bandwidth of the TIA-Rx is affected by dominant poles at amplifying stages of gm_3, gm_5 and gm_6. Thus, the dominant poles can be described by the frequency response of gain stages with transconductance of the dominant poles given by equations (12) to (16):

$$\tau_{eq}=\tau_3+\tau_5+\tau_6 \tag{12}$$

$$\tau_3=\left(R_F\,\|\,\frac{1}{gm_3}\right)\underbrace{\left[C_{s3}+C_{gs4}+\left(1+gm_4R_4\right)C_{gd4}\right]}_{\alpha_1}=\left(R_F\,\|\,\frac{1}{gm_3}\right)\alpha_1 \tag{13}$$

$$\tau_5=\left(\left(R_4+\frac{1}{gm_4}\right)\|\,\frac{1}{gmf_1}\right)\underbrace{\left[C_{s5}+C_{gs6}+(1+gm_6R_6)C_{gd6}\right]}_{\alpha_2}=\left(\left(R_4+\frac{1}{gm_4}\right)\|\,\frac{1}{gmf_1}\right)\alpha_2 \tag{14}$$

$$\tau_6=\left(\left(R_5+\frac{1}{gm_5}\right)\|\,\frac{1}{gmf_2}\right)\underbrace{\left[C_{s6}+C_{gs7}+(1+gm_7R_7)C_{gd7}\right]}_{\alpha_3}=\left(\left(R_5+\frac{1}{gm_5}\right)\|\,\frac{1}{gmf_2}\right)\alpha_3 \tag{15}$$

$$\tau_{eq}=\left(R_F\,\|\,\frac{1}{gm_3}\right)\left(\left(R_4+\frac{1}{gm_4}\right)\|\,\frac{1}{gmf_1}\right)\left(\left(R_5+\frac{1}{gm_5}\right)\|\,\frac{1}{gmf_2}\right)\alpha_1\alpha_2\alpha_3 \tag{16}$$

The 3-dB response of the TIA-Rx can be obtained with τ_{eq} from $f_{3dB}=1/(2\pi\tau_{eq})$. Writing in terms of three dominant poles of TIA-Rx, the three major poles would be $P_1=\tau_1$; $P_2=\tau_5$; $P_3=\tau_6$.

Figure 2 shows the transimpedance gain of the TIA and the bandwidth extension effect of the active feedbacks Af_1 and Af_2. The dotted line is the simulation result of TIA-Rx without active feedback which has a gain of 68 dBΩ at a 3-dB bandwidth of 2.71 Ghz; the dashed line is the result of TIA-Rx with active feedback, Af_1, with 3-dB bandwidth of 5.01 GHz; and the solid line is the result of TIA-Rx gain with two feedbacks Af_1 and Af_2, where the transimpedance gain reduced to 60 dBΩ with a 3-dB bandwidth of 7.36 GHz. The 3-dB bandwidth has been improved from a value of 2.71 GHz to 7.36 GHz after adding two active feedbacks.

The input-referred noise of TIA-Rx can be described as follows:

$$I_{n,eq}\cong 4kT\left(\frac{1}{R_{s1}}+\frac{1}{R_F}+\frac{1}{R_2}\right)+\frac{4kT\omega^2\left(C_{db2}+C_{gs3}+Cf_{gd1}\right)^2}{gm_4^2}\left(\Gamma+\frac{1}{R_4}\right)+\frac{4kT\omega^2\left(C_{gs2}+C_{gd1}\right)^2}{gm_2^2}\left(\Gamma+\frac{1}{R_F}+\frac{1}{R_2}\right)+\frac{4kTR_1^2\left[1+\omega^2\left(C_{in}+C_{gs1}+C_{sb2}\right)^2\right]}{\left(1+gm_1R_1\right)^2R_{s1}^2}\left(\Gamma+\frac{1}{R_1}\right) \tag{17}$$

where k Boltzmann's constant; T is the absolute temperature; Γ is the channel-noise factor of MOSFET; C_{in} is the input parasitic capacitance which includes the photodiode capacitance; bond-pad parasitic capacitance, and electrostatic discharge capacitances ($C_{in}=C_{pd}+C_{ESD}+C_{pad}$). From eq. (17), it can be observed that low frequency noise is dominated by resistor thermal noises and high frequency dominant noise occurs due to input parasitic capacitances. The dominant high-frequency noise is divided by $(1+gm_1R_1)$ gain of the local feedback, and hence, the size of local feedback has been increased to reduce total equivalent noises. To reduce the overall noise current of TIA-Rx the resistors, R_{s1}, R_F, R_2, and gm_1 with gm_4 transistors sizes should be increased

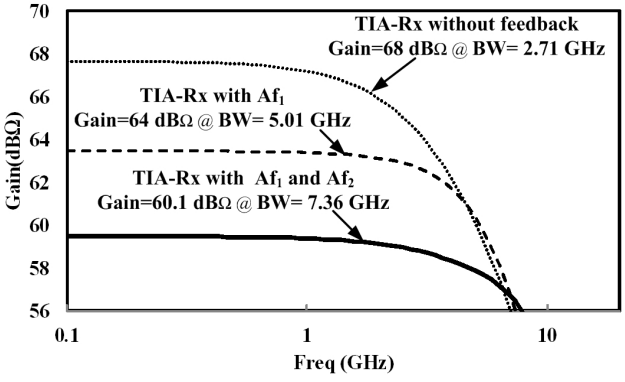


FIG. 2. The simulated result of TIA-Rx with and without active feedback.

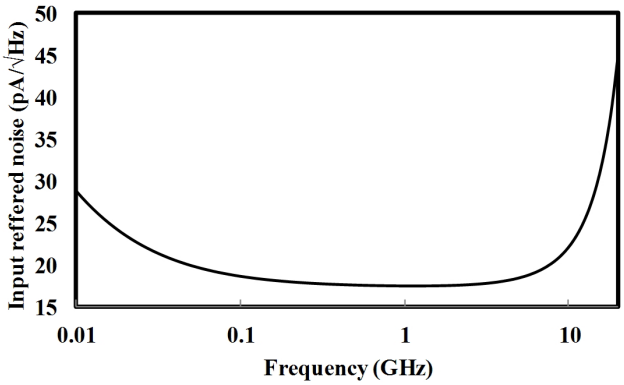


FIG. 3. The simulated input-referred noise of TIA-Rx.

to be as large as possible, and to reduce the parasitic capacitance the transistors, M_1, M_2 and M_3 sizes should be reduced. However, increasing R_F will result in bandwidth degradation from eq. (16) and increasing the gm_1 and gm_4 will result in W/L ratio and bias current of transistor M_1 and M_4. Hence, in our proposed TIA-Rx design we have optimized the values of R_{s1} and M_1 to reduce the bias current by increasing the resistor value for the increase of W/L ratio of a transistor and achieved compensated input-referred noise. The values of R_F, M_3 and M_4 have been carefully chosen to improve the frequency operation of the TIA-Rx while keeping the noise current minimum. Fig. 3 shows the simulated input-referred noise of TIA-Rx. The simulated input-referred noise of TIA-Rx is equal to 18 pA/√Hz at 3-dB bandwidth.

III. EXPERIMENTAL RESULTS

The proposed TIA-Rx circuit has been designed and fabricated in a 0.13 μm CMOS technology. The fabricated TIA-Rx chip core occupies an area of 0.051 mm^2. The TIA-Rx chip is mounted on wire-bounded chip-on-board (COB) for frequency response, eye-diagram and integrated output noise measurements. The photograph of TIA-Rx chip is shown in Fig. 4.

Figure 5 shows the integrated output noise measured from the output of the TIA-Rx chip with no input connected. The standard deviation of 0.52 mV is measured and by subtracting the oscilloscope noise of 0.1 mV, the corrected integrated noise is 0.42 mV.

The frequency response is measured using an Agilent 8703B lightwave component analyzer. The measured 3-dB bandwidth of the TIA-Rx chip is 6.9 GHz and a transimpedance gain of 60 dBΩ, as shown in Fig. 6, which were obtained with 1 kΩ shunt passive feedback, R_F, and 0.24 pF photodiode capacitance, C_{pd}. Fig. 7 shows the input-referred noise, where 3-dB bandwidth input-referred noise equals to 20 pA/√Hz. From Fig. 6 and Fig. 7, the measured results are in agreement with the simulated results. However, the slight

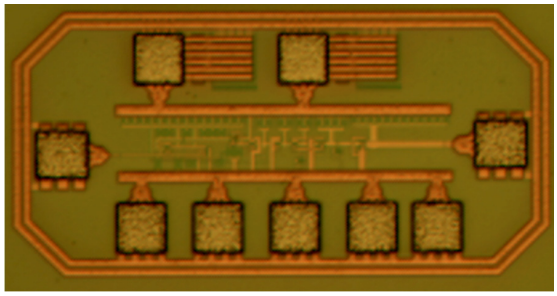


FIG. 4. Die photograph of the fabricated TIA-Rx chip.

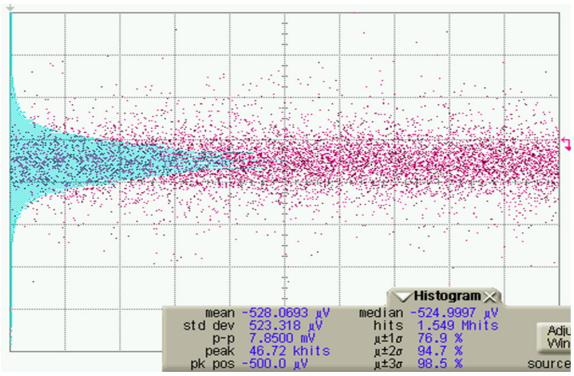


FIG. 5. Measured integrated output noise of the proposed TIA-Rx.

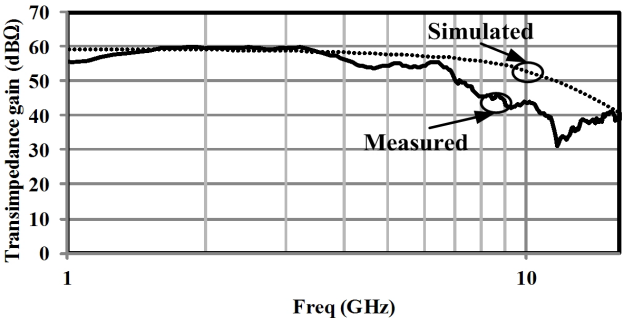


FIG. 6. Transimpedance gain (Z_T) of the proposed TIA-Rx chip: the solid and dotted lines show the measured and simulated results, respectively.

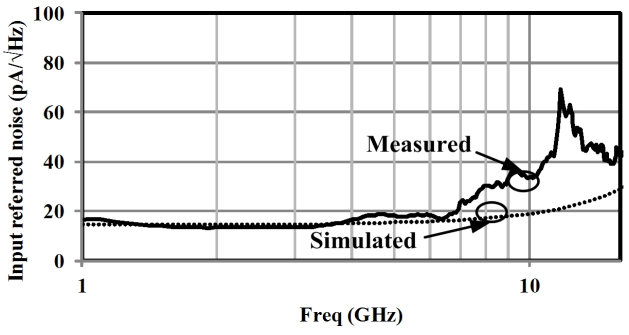
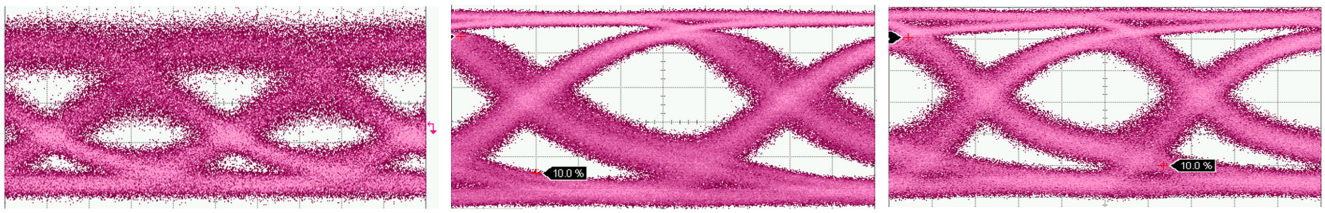


FIG. 7. The input-referred noise of the proposed TIA-Rx chip: the solid and dotted lines show the measured and simulated results, respectively.

TABLE 1. The comparison of the proposed TIA-Rx chip performance with other works

Ref.	This work	[2]	[3]	[4]	[5]	[6]	[7]
Inductor	No	Yes	Yes	Yes	Yes	No	No
GBP/PDC (GHz/mW)	408	578	441.1	810	114	78	233.9
Chip core size (mm^2)	0.051	0.0714	0.93	1.84	0.14	0.06	-
CMOS technology (μm)	0.13	0.13	0.18	0.18	0.18	0.13	0.18
DC power (mW)	16.9	4.1	91.8	210	70.2	98	13.97
Gain (dBΩ)	60	50	75	87	61	62	51.7
Data rate (Gbps)	10	10	10	10	10	10	10
3-dB BW (GHz)	6.9	7.5	7.2	7.6	7.2	6	8.5
PD capacitance (pF)	0.24	0.3	0.45	0.15	0.25	0.25	0.25
Sensitivity (μA)	120	20	-16.4 dBm	-12 dBm	10	22.4	-
BER	10^{-12}	10^{-12}	10^{-12}	10^{-12}	-	10^{-12}	-

Gain bandwidth product per DC power (GBP/PDC), bandwidth (BW).



(a) (b) (c)

FIG. 8. The measured eye-diagrams of the TIA-Rx chip with PRBS of 2^{31}-1 at 10 Gbps data rate: (a) I_{in}=20 μA and $V_{out,pp}$=20 mV, 20 ps/div, (b) I_{in}=120 μA and $V_{out,pp}$=120 mV, 16.3 ps/div and (c) I_{in}=850 μA and $V_{out,pp}$=750 mV, 23.4 ps/div.

discrepancy between the measured and simulated results may have been attributed by process variation during the fabrication process.

Table 1 shows a comparison of the TIA-Rx performance with other works. From Table 1, it can be seen that the size of the proposed TIA-Rx is smaller than the other TIA circuits, where passive inductor peaking have been utilized for bandwidth extension. In our proposed TIA-Rx, using active feedback system achieves comparatively high gain-bandwidth product per DC power (GBP/PDC) figure of merit of 408 GHzΩ/mW with reduced chip area.

To evaluate optical TIA-Rx dynamic response, 2^{31}-1 pseudorandom binary sequence (PRBS) input signal, generated from Anritsu MP1736 pulse-pattern generator was applied, while the output was measured with an Agilent 8610A oscilloscope. The eye-diagrams of TIA-Rx are shown in Fig. 8. The applied input current 20 μA, 120 μA and 850 μA results in 20 mV, 120 mV and 750mV TIA-Rx output, respectively. The eye-diagrams of TIA-Rx show rise/fall times with root-mean square (RMS) jitter of 86.7/90ps with 13 ps for I_{in} = 20μA, 75.1/129ps with 6.91ps for I_{in} = 120μA and 71.4/118.2ps with 6.76 ps for I_{in} = 750μA at 10 Gbps. The measured bit error rate (BER) as a function of the input current is presented in Fig. 9. This BER measurement is done at 10 Gbps data rate using 2^{31}-1 PRBS input signal, and a BER of less than 10^{-12} is achieved with input current of about ~120 μA. The power dissipation of the TIA-Rx is 16.9 mW at 1.3 V.

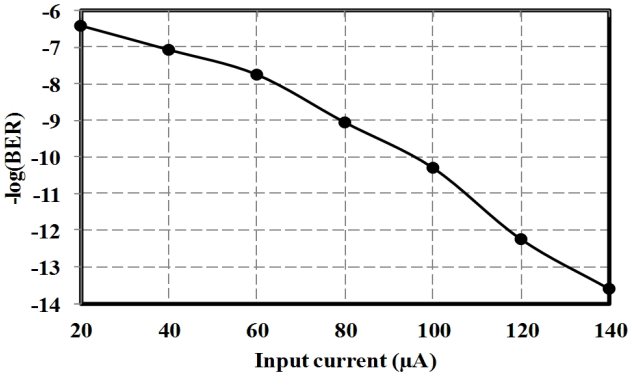


FIG. 9. The measured BER using 2^{31}-1 PRBS input signal as a function of input current at 10 Gbps data rate.

Besides reducing input impedance of TIA-Rx, the RGC block with local (resistive) feedback increases the input-

referred noise as well. The addition of post amplifying transconductance stages adds extra noise. The increase in input-referred noise leads to degradation of input sensitivity. As a result, the dynamic characteristics (eye diagram) of the TIA-Rx chip shows better performance with slightly higher input current than the TIA-Rx with lower input current. From the eye-diagrams and BER measurement results are shown in Figs. 8 and Fig. 9, with increase of an input current, the output voltage of the TIA-Rx increases. Thus, our proposed TIA-Rx design requires higher input current of about ~120μA and above to be able to provide sufficient output signal to the next stages such as De-serializer, PLL, and clock data recovery (CDR) circuitry. Hence, our proposed TIA-Rx can be applied as a front-end optical Rx to convert the input photo current to the output voltage signal in order to feed to the De-serializer, PLL and CDR circuits.

IV. CONCLUSION

A TIA-Rx has been designed and implemented in 0.13 μm CMOS technology for optical interconnect applications operating up to 10 Gbps. The TIA-Rx shows a good eye performance up to 10 Gbps with BER of less than 10^{-12}. The TIA-Rx chip core is 0.051 mm^2 with power consumption of 16.9 mW at 1.3 V. The measured input-referred noise of the TIA-Rx is 20pA/$\sqrt{}$Hz with a 3-dB BW of 6.9 GHz. The TIA-Rx chip utilizes two intersecting active feedback systems with RGC input stage and occupies a small chip area with an efficient GBP/PDC figure of merit of 408 GHzΩ/mW. Our proposed TIA-Rx can be applied as a front-end optical Rx to convert the input photo current to output voltage signal, high enough to feed to the next stages such as the De-serializer, PLL, and/or CDR circuits, and it is applicable for chip-to-chip optical interconnects.

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REFERENCES

1. B. Analui and A. Hajimiri, "Bandwidth enhancement for transimpedance amplifier," IEEE Journal of Solid-Stage Circuits **39**, 1263-1270 (2004).
2. T. H. Ngo, T. W. Lee, and H. H. Park, "4.1 mW 50 dBΩ 10 Gbps transimpedance amplifier for optical receivers in 0.13 μm CMOS," Microwave and Optical Technology Lett. **53**, 448-451 (2011).
3. J. D. Jin and Sh. S. H. Hsu, "A 75-dBΩ 10-Gb/s transimpedance amplifier in 0.18-μm CMOS technology," IEEE Photon. Technol. Lett. **20**, 2177-2179 (2008).
4. W.-Z. Chen, Y.-L. Cheng, and D.-Sh. Lin, "A 1.8-V 10-Gb/s fully integrated CMOS optical receiver analog front-end," IEEE Journal of Solid-State Circuits **40**, 1388-1396 (2005).
5. Ch.-H. Wu, Ch.-H. Lee, W.-Sh. Chen, and Sh.-I. Liu, "CMOS wideband amplifiers using multiple inductive-series peaking technique," IEEE Journal of Solid-State Circuits **40**, 548-552 (2005).
6. O. Momeni, H. Hashemi, and E. Afshari, "A 10-Gb/s inductorless transimpedance amplifier," IEEE Trans. on Circuits and Systems **57**, 926-930 (2010).
7. L. Zhenghao, Ch. Dandan, and Y. K. Seng, "An inductor-less broadband design technique for transimpedance amplifiers," in *Proc. of ISIC* (Suntec, Singapore, Dec. 2009), pp. 232-235.
8. S. M. Park and H. J. Yoo, "1.25-Gb/s regulated cascode CMOS transimpedance amplifier for gigabit Ethernet applications," IEEE Journal of Solid-State Circuits **39**, 112-121 (2004).
9. Ch. T. Chan and O. T. Chen, "Inductor-less 10Gb/s CMOS transimpedance amplifier using source-follower regulated cascode and double three-order active feedback," in *Proc. of IEEE Int. Symp. on Circuits and Systems* (Island of Kos, Greece, May 2006), pp. 5487-5490.