Modeling of Eye-Diagram Distortion and Data-Dependent Jitter in Meander Delay Lines on High-Speed Printed Circuit Boards (PCBs) Based on a Time-Domain Even-Mode and Odd-Mode Analysis

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Abstract—Crosstalk induced in a meander delay line produces a significant amount of waveform distortion and data-dependent jitter at the output port. This paper introduces an interpretation of the eye-diagram distortion and the jitter generation mechanism based on a time-domain even- and odd-mode analysis of a coupled transmission line structure. From the proposed analysis, this paper proposes jitter-estimation equations for both the short and long unit line delay cases. The eye-diagram distortion and timing jitter are predicted and estimated, respectively. In order to verify the jitter-estimation equations, a series of microstrip-type printed circuit board test vehicles with the meander delay line are fabricated and tested. The measured jitter shows good agreement with the proposed jitter-estimation equations.

Index Terms—Crosstalk, data-dependent jitter (DDJ), eye diagram, meander delay line.

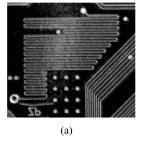
I. INTRODUCTION

R ECENTLY, as clock frequencies and data transmission rates in semiconductor systems steadily increase over gigahertz frequency ranges, timing control of high-speed clock and digital data signal traces on printed circuit boards (PCBs) becomes a critical part of the PCB design task. A timing error of even a tiny fraction of the clock cycle time can cause serious timing problems between the clock trace and the signal traces or between the signal traces on the multilayer PCB. This ultimately limits are achievable clock frequency and data transmission rate of the system [1]. As a result, design methods for timing error minimization have attracted significant attention not only at chip and package design levels, but also at the PCB design level. As

Manuscript received November 15, 2007; revised March 9, 2008. First published July 25, 2008; last published August 8, 2008 (projected). This work was supported by the Ministry of Knowledge Economy/Institute for Information Technology Advancement (MIC/IITA) under the Information Technology Research and Development Program (2005-S-118-02, Development of High-Performance and Smallest SiP Technology).

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Digital Object Identifier 10.1109/TMTT.2008.927543



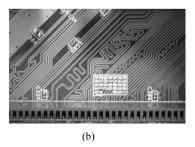


Fig. 1. Meander delay lines on PCB designs. (a) Meander delay line design on a mother board of a laptop computer. (b) Meander delay line designs on a mother board of a desktop computer.

a method for reducing the timing error in the PCB design, delay lines have been adopted in critical nets to provide predetermined timing delay of the clock traces or the signal traces. A space and cost effective delay line structure should have a regular and delay-predictable shape with a compact design [2].

The most popular delay line scheme in PCB design is the meander-type structure, which consists of a group of unit delay lines with equal lengths, as shown in Fig. 1. The objective of the meander delay line is to achieve a precisely controlled timing delay of a clock or a signal trace with considerably enhanced surface area efficiency on the PCB [3].

However, since each unit delay line in the meander line structure is facing its neighbor unit delay line so closely in a compact surface area, electromagnetic (EM) coupling crosstalk occurs between the adjacent lines. In particular, since the amount of the crosstalk at the delay line is heavily dependent on the data pattern and transmission rate, it can produce a considerable amount of the timing jitter at the high-speed digital data traces. This timing jitter is referred to as data-dependent jitter (DDJ) [4], [5]. As a consequence, predicting the eye-diagram distortion and estimating the timing-jitter increase caused by the EM coupling crosstalk in the meander delay line are considered as essential components of PCB design.

There have been several attempts to analyze the EM coupling crosstalk effect at the meander delay line. Previous studies in [2], [3], [6]–[9] have pointed out that the crosstalk noise between the unit delay lines at the meander delay line structure is accumulated synchronously at the receiving end due to inherent periodicity of the structure. In these studies, the crosstalk noise

levels at the output waveform of the receiving end have been calculated using quantitative analysis [3], laddering crosstalk analysis [6], and method of moments (MoM) simulation [7]. Reference [8] has proposed an alternative delay line structure, called a flat spiral delay line to alleviate the crosstalk problem. Furthermore, [9] has reported the eye diagrams of the proposed delay line structure in [8] and provided a comparison with the conventional meander delay line structure. It analyzed the eye diagrams using conventional crosstalk equations by mutual capacitance and mutual inductance model, obtained the eye diagram using HSPICE simulation, and compared them with measurements. However, no research has yet been reported to estimate the DDJ caused by the crosstalk noise at the meander delay line, which is now a crucial subject of the PCB design, due to its frequent use in high-speed digital signal traces. Furthermore, the conventional crosstalk equations does not consider the signal rise time in the coupled transmission line section.

In this paper, the new crosstalk modeling based on time domain even- and odd-mode analysis will first be represented, which is one factor of the DDJ mechanism. Second, an analytical method to estimate the eye-diagram distortion and the DDJ at the meander delay line will be introduced based on a time-domain even- and odd-mode analysis. Jitter-estimation equations will then be derived from the suggested analysis. In order to verify the proposed eye-diagram analysis and the jitter-estimation equations in the meander delay line, a series of meander delay lines on test PCBs with a microstrip-type coupled transmission line structure are fabricated and measured. The design of the test vehicles has different numbers of unit line sections and unit line lengths. Finally, the measured timing jitters will be compared with the jitter predictions from the jitter-estimation equations. The measured eye diagrams match very well with the proposed analysis. The proposed jitter estimations have aslo shown good agreement with the measurements for both short unit line delay case and long unit line delay case.

II. MODELING AND ANALYSIS OF NEAR-END CROSSTALK (NEXT) AND INCREASED SIGNAL RISE TIME IN MEANDER DELAY LINES

Fig. 2 shows the structure and dimensions of a meander delay line structure. It consists of equal-length unit lines (l_u) of N unit lines and can be regarded as a combination of numerous coupled transmission line sections. This section focuses on the derivation of NEXT waveforms and NEXT equation, which affects the DDJ in a meander delay line, as well as the effect of an increased signal rise time in the coupling mechanism at the output waveform of the coupled transmission structure.

A. NEXT Waveform and Equation in a Coupled Transmission Line

In this paper, a time-domain even- and odd-mode analysis is used to derive the NEXT waveform and equations in the coupled line sections in the meander delay line [10]–[12].

As illustrated in Fig. 3, an input step pulse with an amplitude of V_s and a rise time of T_r , which is applied using a 50- Ω source impedance $Z_{0_SE}(Z_{0_SE}=50~\Omega)$ [port (A) in Fig. 3(a)] at the

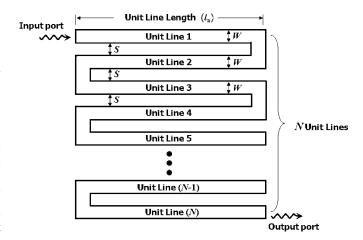


Fig. 2. Structure and dimensions of the meander delay line.

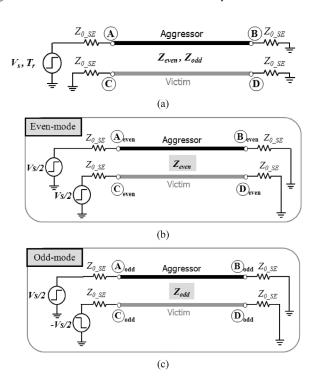


Fig. 3. (a) Even- and odd-mode time-domain analysis setup of a coupled transmission line with an excitation at input port (a) with a voltage level of V_s and a rise time of Tr through $Z_{0_SE}=50~\Omega$ source-end impedance. (b) Even-mode excitation. (c) Odd-mode excitation.

aggressor line can be separated into even- and odd-mode excitations. Each mode has different propagation velocity and characteristic impedance (even-mode impedance $Z_{\rm even}$ and odd-mode impedance $Z_{\rm odd}$), resulting in different arrival times at the receiver ports and different excitation voltage magnitude [12].

To simplify the analysis, the even- and odd-mode waveforms can be considered separately, as shown in Fig. 3. $TD_{\rm odd}$ and $TD_{\rm even}$ represent the time delay (TD) of the odd- and the even-mode waves, respectively. The excited even-mode voltage at A when t=0 is expressed by (1) using the voltage division rule. Next, the even-mode voltage at B when $t=TD_{\rm even}$ can be described by (2), while the incident even-mode wave is reflected by the mismatched termination at A with Z_{0_SE} . The reflected wave is then superimposed with the incident wave. The even-

mode waveform at A is also induced when $t = 2\text{TD}_{\text{even}}$ using the same procedure as shown in (3)

$$V_{A_\text{even}}(0) = \frac{Z_{\text{even}}}{Z_{0_SE} + Z_{\text{even}}} \times \frac{V_S}{2}$$

$$= k_{\text{even}_1} \times V_S$$

$$= V_{C_\text{even}}(0) \qquad (1)$$

$$V_{B_\text{even}}(\text{TD}_{\text{even}}) = (1 + \Gamma_{\text{even}}) \times V_{A_\text{even}}(0)$$

$$= \frac{2Z_{0_SE}}{Z_{0_SE} + Z_{\text{even}}} \times \frac{Z_{\text{even}}}{Z_{0_SE} + Z_{\text{even}}} \times \frac{V_S}{2}$$

$$= k_{\text{even}_2} \times V_S \qquad (2)$$

$$V_{A_\text{even}}(2\text{TD}_{\text{even}}) = V_{A_\text{even}}(0) + \Gamma_{\text{even}} \times V_{A_\text{even}}(0)$$

$$= (1 + \Gamma_{\text{even}}) \times V_{A_\text{even}}(0)$$

$$= V_{C_\text{even}}(2\text{TD}_{\text{even}}) \qquad (3)$$

$$\Gamma_{\text{even}} = \frac{Z_{0_SE} - Z_{\text{even}}}{Z_{0_SE} + Z_{\text{even}}} \qquad (4)$$

where Γ_{even} is the reflection coefficient at port \mathbb{B}_{even} .

In a similar way, the following equations are for the odd-mode excitation and reflection:

$$V_{A_\text{odd}}(0) = \frac{Z_{\text{odd}}}{Z_{0_SE} + Z_{\text{odd}}} \times \frac{V_S}{2}$$

$$= k_{\text{odd_1}} \times V_S$$

$$= -V_{C_\text{odd}}(0) \qquad (5)$$

$$V_{B_\text{odd}}(\text{TD}_{\text{odd}}) = (1 + \Gamma_{\text{odd}}) \times V_{A_\text{odd}}(0)$$

$$= \frac{2Z_{0_SE}}{Z_{0_SE} + Z_{\text{odd}}} \times \frac{Z_{\text{odd}}}{Z_{0_SE} + Z_{\text{odd}}} \times \frac{V_S}{2}$$

$$= k_{\text{odd_2}} \times V_S \qquad (6)$$

$$V_{A_\text{odd}}(2\text{TD}_{\text{odd}}) = V_{A_\text{odd}}(0) + \Gamma_{\text{odd}} \times V_{A_\text{odd}}(0)$$

$$= (1 + \Gamma_{\text{odd}}) \times V_{A_\text{odd}}(0)$$

$$= -V_{C\text{-odd}}(2\text{TD}_{\text{odd}})$$

$$\Gamma_{\text{odd}} = \frac{Z_{0\text{-}SE} - Z_{\text{odd}}}{Z_{0\text{-}SE} + Z_{\text{odd}}}$$
(8)

where Γ_{odd} is the reflection coefficient at port \textcircled{B}_{odd} .

To obtain the final waveform at each port, the even- and the odd-mode waveforms can be added together through the principle of superposition.

In order to analyze the crosstalk effect at the meander delay line for the eye-diagram distortion and the jitter generation in Sections III and IV, this study is focused on the NEXT waveform, which is measured at port \bigcirc in Fig. 3(a), as shown in Fig. 4. In Fig. 4(c), the NEXT voltage level from $t=T_r$ to $t=2\mathrm{TD}_{\mathrm{odd}}$ is denoted as V_{NEXT_1} , and the NEXT voltage level from $t=2\mathrm{TD}_{\mathrm{odd}}+T_r$ to $t=2\mathrm{TD}_{\mathrm{even}}$ is referred to as V_{NEXT_2} . V_{NEXT_1} can be calculated from the summation of (1) and (5). V_{NEXT_2} can be calculated from the summation of (1) and (7). The propagation velocity difference between the two-mode waves produces a stair-type NEXT waveform from $t=2\mathrm{TD}_{\mathrm{odd}}$ to $t=2\mathrm{TD}_{\mathrm{even}}$, V_{NEXT_2} , which cannot be explained by the conventional crosstalk mechanism. The final NEXT equation is represented as follows:

$$V_{\text{NEXT}} = \begin{cases} V_{\text{NEXT_1}} = k_{\text{NEXT_1}} \times V_S, \\ \text{if } T_r \le t \le 2\text{TD}_{\text{odd}} \\ V_{\text{NEXT_2}} = k_{\text{NEXT_2}} \times V_S, \\ \text{if } 2\text{TD}_{\text{odd}} + T_r \le t \le 2\text{TD}_{\text{even}} \end{cases}$$
(9)

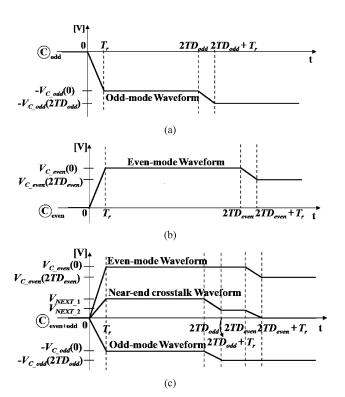


Fig. 4. NEXT waveform caused by the separated even- and odd-mode propagation in the coupled transmission lines. (a) Odd-mode waveform at port \bigodot $_{\rm odd}$ in Fig. 3(c). (b) Even-mode waveform at port \bigodot $_{\rm even}$ in Fig. 3(b). (c) Final NEXT waveform at port \bigodot in Fig. 3(a) by the superposition of the two-mode waveforms.

where

$$V_{\text{NEXT-1}} = \left(\frac{Z_{\text{even}}}{Z_{0_SE} + Z_{\text{even}}} - \frac{Z_{\text{odd}}}{Z_{0_SE} + Z_{\text{odd}}}\right) \times \frac{V_S}{2}$$

$$V_{\text{NEXT-2}} = \left(\frac{Z_{\text{even}}}{Z_{0_SE} + Z_{\text{even}}} - \frac{2Z_{0_SE} \times Z_{\text{odd}}}{(Z_{0_SE} + Z_{\text{odd}})^2}\right) \times \frac{V_S}{2}$$

$$k_{\text{NEXT-1}} = \frac{1}{2} \times \left(\frac{Z_{\text{even}}}{Z_{0_SE} + Z_{\text{even}}} - \frac{Z_{\text{odd}}}{Z_{0_SE} + Z_{\text{odd}}}\right)$$

$$= (k_{\text{even-1}} + k_{\text{odd-1}}) \qquad (10)$$

$$k_{\text{NEXT-2}} = \frac{1}{2} \times \left(\frac{Z_{\text{even}}}{Z_{0_SE} + Z_{\text{even}}} - \frac{2Z_{0_SE} \times Z_{\text{odd}}}{(Z_{0_SE} + Z_{\text{odd}})^2}\right)$$

$$= (k_{\text{even-1}} + k_{\text{odd-2}}). \qquad (11)$$

The main NEXT coefficient $k_{\rm NEXT_1}$ will be used to analyze the eye-diagram distortion and jitter generation in the following sections.

B. Increased Signal Rise Time by Separated Even-Mode and Odd-Mode Propagations

The signal rise time can be degraded at the output port of the meander delay line due to high-frequency conductor and dielectric losses at the transmission line [10]. However, the increase in the signal rise time at the port of the meander delay line is

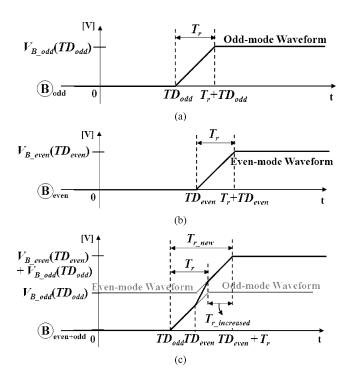


Fig. 5. Increased signal rise time caused by the separated even- and odd-mode propagation in the coupled transmission lines. (a) Odd-mode output waveform at port $\textcircled{}_{\text{odd}}$ in Fig. 3(c). (b) Even-mode output waveform at port $\textcircled{}_{\text{even}}$ in Fig. 3(b). (c) Final output waveform at port $\textcircled{}_{\text{odd}}$ in Fig. 3(a) by the superposition of the two-mode waveforms resulting in the increased signal rise time.

mainly caused by the propagation velocity difference between the even- and odd-mode waves, especially in the coupled microstrip-type transmission line structure. Detailed waveforms and analysis of the rise-time degradation are presented in Fig. 5. The voltage amplitudes of $V_{B_{\rm even}}({\rm TD_{\rm even}})$ and $V_{B_{\rm odd}}({\rm TD_{\rm odd}})$ are expressed in (2) and (6), respectively.

Assuming that the coupled transmission lines consist of a lossless medium, the resulting signal rise time $(T_{r_{-new}})$ after propagation through a single section of the coupled transmission line of Fig. 3(a) is expressed in (12), as illustrated in Fig. 5(c). The increased signal rise time $(T_{r_{-increased}})$ can then be represented as follows in (13):

$$T_{r\text{-new}} = T_r + T_{r\text{-increased} = T_r + \text{TD}_{\text{even}} - \text{TD}_{\text{odd}}}$$
 (12)

$$T_{r_increased} = TD_{even} - TD_{odd}$$
 (13)

where $TD_{\rm even}$ and $TD_{\rm odd}$ are propagation delays of the evenand odd-mode waveforms through a single section of the coupled transmission line, respectively.

Equation (13) makes it possible to calculate total signal rise time degradation through the full meander delay line with N unit lines, as shown in Fig. 2. As shown in Fig. 6(a) and (b), both outside unit lines (k = 1 and k = N) of the meander delay line are experiencing one coupling structure with the adjacent unit line (k = 2 or k = N - 1), while the inside unit lines (from k = 2 to k = N - 2) are experiencing two coupling structures with both adjacent unit lines (for k = i, i - 1 and i + 1 lines).

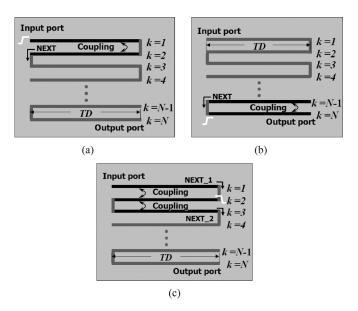


Fig. 6. NEXT in a meander delay line structure. (a) Coupling at the first coupled transmission line section and a resulted NEXT propagation. (b) Coupling at the last coupled transmission line section and resulted NEXT propagation. (c) Coupling in the inner coupled transmission line sections and resulted NEXT propagations.

Therefore, the number of coupled transmission line structures $(N_{\rm ctl_propagation})$ in the meander delay line with N unit lines, through which an input pulse can experience, can be determined as follows:

$$N_{\text{ctl-propgation}} = 2 + 2 \times (N - 2) = 2(N - 1).$$
 (14)

Consequently, the signal rise time at the output port of the meander delay line with N unit lines can be calculated as follows using (15):

$$T_{r_{-N}\text{-meander}} = T_r + N_{\text{ctl_propagation}} \times T_{r_{\text{-increased}}}$$

= $T_r + 2(N-1) \times (\text{TD}_{\text{even}} - \text{TD}_{\text{odd}})$. (15)

Equation (15) will be used for the analysis and prediction of the timing jitter in the following sections. This term also was not considered in the conventional crosstalk mechanism.

III. OUTPUT WAVEFORM MODELING IN CASE OF SINGLE-STEP INPUT SIGNAL IN MEANDER DELAY LINES

In order to analyze the timing jitter in the meander delay line structure, it is necessary to obtain the output waveform equation of the single step input signal. In the meander delay line with N unit lines and a single step input signal, the output waveform at the end of the meander delay line can be acquired using a superposition of all of the NEXT generated in the crosstalk occurrences of $N_{\rm ctl}$ -propagation. The accumulation mechanism for the crosstalk noise of the meander delay lines has been addressed by [15]. A general output waveform equation has been proposed to predict the output waveform in the meander delay lines considering the crosstalk effect described

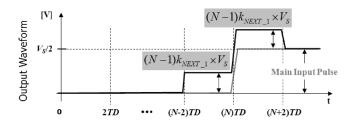


Fig. 7. Output waveform analysis of a meander line with N unit lines in case of single step input signal, where TD means the propagation delay time of one unit line. The source step pulse with a voltage amplitude of V_s and a rise time of T_r is injected at the input port through a $50-\Omega$ source impedance at t=0.

in (16), shown at the bottom of this page, where u(t) is the unit step function.

To clarify the general output waveform equation in the meander delay line with N unit lines, as expressed in (16), the output waveform is plotted in Fig. 7. Nevertheless, the lossless assumption can cause small TD between each NEXT. It can induce a decrease of the piled NEXT voltage level after the original source input signal. This effect will be discussed later in this paper.

IV. EYE DIAGRAM AND TIMING-JITTER ESTIMATION IN MEANDER DELAY LINES

This section will analyze the eye diagram and jitter generation mechanism in the meander delay line based on the NEXT analysis introduced in the previous sections, and will propose jitter-estimation equations using a relationship between the propagation TD of one unit line and the unit interval (UI) of the pseudorandom bit sequence (PRBS). In Section IV-A, the predicted eye diagram and proposed jitter-estimation equations will be verified by comparisons with eye diagram and jitter measurements of the test vehicles.

Total jitter (TJ) is composed of random jitter (RJ) and deterministic jitter (DJ), and DDJ is one part of DJ [4], [5]. In the meander delay line case, DDJ is from inter-symbol interference (ISI) caused by the following two factors:

- ISI caused by the NEXT;
- ISI caused by channel loss,

Here, the DDJ due to the NEXT will also be analyzed assuming a lossless meander delay line because DDJ due to loss is very small and negligible. (Both simulation results of lossless and lossy medium show same DDJ.)

Fig. 8(a) shows a meander delay line of a PCB with N unit lines with a PRBS input data. At first, the short unit line delay case is when the unit line delay (TD) is much shorter than UI, as described in (17). In order to simplify the analysis, a data pattern of "101101" is fed into the input port of the meander delay line

$$2TD < UI$$
 (short unit line delay case) (17)

$$2TD \ge UI$$
 (long unit line delay case) (18)

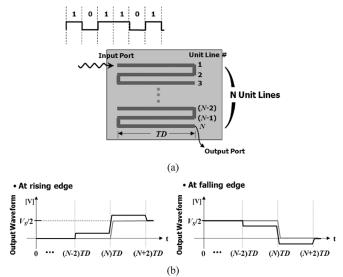


Fig. 8. (a) Meander delay line with N unit lines with the PRBS input data. (b) Induced NEXT caused by the rising/falling edges of the input step pulse. The PRBS data with voltage amplitude of V_s and a rise time of T_r is injected at the input port through a 50- Ω source impedance.

where TD = l_u/v is the propagation TD of one unit line, $v = c/\sqrt{\varepsilon_{r_{-}\text{eff}}}$ is the velocity of the waveform for a microstrip line, and l_u is the length of one unit line.

Fig. 8(b) presents the NEXT waveforms by rising and falling edges, as previously explained in Fig. 7. A rising edge of the input step pulse generates the NEXT with a positive voltage in the output waveform. Similarly, a falling edge also induces the NEXT with a negative voltage.

A. Case of the Long Unit Line Delay

When 2TD is equal to or greater than UI, the output waveform is affected by the NEXT at the rising and falling edges over the entire UI, as shown in Fig. 9. The NEXT occurs before and after the transitions when $t=N\times \mathrm{TD}$, as shown in Fig. 7. Therefore, the expected output waveform and the eye diagram can be described as shown in Fig. 9(a) and (b), respectively. It should be noted that the eye diagram has three discrete high levels around $V=V_S/2$, and three discrete low levels around V=0, regardless of the number of unit lines (N). The three high-voltage levels consist of the positive NEXT by the rising edge, the original high input voltage level, and the negative NEXT by the falling edge. In a similar manner, the three low-voltage levels are the positive NEXT by the rising edge, the original low input voltage level, and the negative NEXT by the falling edge.

An expanded eye diagram is shown in Fig. 10 for the case of the long unit line delay. Since there are three high-voltage levels and three low-voltage levels, respectively, there are also three crossing points at rising and falling edges of the eye diagram. In this way, it is found that DDJ is produced in the case of the long

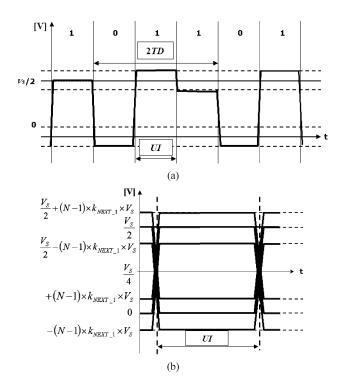


Fig. 9. Case of a long unit line delay in the meander delay line with N unit lines. The PRBS data with voltage amplitude of V_s and a rise time of T_r is injected at the input port through a 50- Ω source impedance. (a) Output waveform. (b) Expected eye diagram.

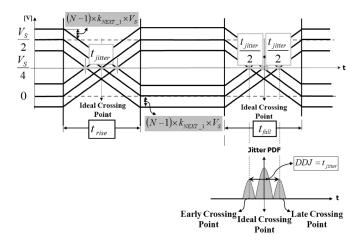


Fig. 10. Expanded eye diagram for the case of the long unit line delay in the meander delay line with N unit lines.

unit line delay, whereas DDJ is not generated in the case of the short unit line delay, which will be shown in Section V. Since the DDJ can be characterized by the width across these crossing points, the jitter equation can be extracted in order to estimate DDJ amount [4].

To extract a jitter-estimation equation for the case of the long unit delay line, the eye diagram at the rising edge is depicted in Fig. 11(a). If the meander delay line has N unit lines, the accumulated NEXT, which decides the three levels in the expanded eye diagram, is $(N-1) \times k_{\text{NEXT-1}} \times V_S$, while this value is shown in (16) and Fig. 7. The jitter-estimation equation can then be extracted using a triangle principle, as demonstrated

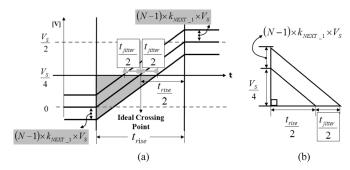


Fig. 11. Extraction of the timing jitter (t_{jitter}) for the case of the long unit delay line in the meander delay line with N unit lines. (a) At the rising edge. (b) Triangle principle to calculate the timing jitter (t_{jitter}) .

in Fig. 11(b). From Fig. 11(b), the following relations can be induced:

$$\left\{ \frac{V_S}{4} + (N-1) \times k_{\text{NEXT}_1} \times V_S \right\} : \frac{V_S}{4} \\
= \left(\frac{t_{\text{jitter}}}{2} + \frac{t_{\text{rise}}}{2} \right) : \frac{t_{\text{rise}}}{2}.$$
(19)

Therefore, the proposed jitter-estimation equation for the case of the long unit line delay in the meander line with N unit lines can be represented as

$$t_{\text{jitter}} = 4 \times t_{\text{rise}} \times (N-1) \times k_{\text{NEXT_1}}$$
,
if $2\text{TD} \geq \text{UI}$ (long unit line delay case). (20)

The timing jitter is seen to be heavily dependent on the number of unit lines (N), the main NEXT coefficient (k_{NEXT_1}) , and the increased signal rise time $(t_{\text{rise}} = T_{r_N_\text{meander}})$. The increased signal rise time $T_{r_N_\text{meander}}$ at the output port will also increase proportionally to the number of unit lines (N-1). As a result, t_{jitter} increases proportionately to the square of the number of unit lines $((N-1)^2)$. This means that the NEXT at the meander delay line can cause a significant amount of timing jitter, especially when there are many unit lines. Using this proposed jitter-estimation equation (20), the timing jitter can be estimated for the case of the long line delay in meander delay lines with N unit lines.

B. Case of the Short Unit Line Delay

As shown in Fig. 12, since 2TD is much smaller than UI, the induced NEXT by the rising and falling edges occupies only a small portion of the duration of the UI. As a consequence, the eye diagram can be depicted as shown in Fig. 12(b).

An expanded eye diagram of Fig. 12(b) is redrawn in Fig. 13. It illustrates the crossing points of the output waveform at the rising and the falling edges with respect to the ideal crossing points. It is found that real crossing points are shifted by the amount of $-\Delta t_{\rm delay}$ at both edges in the eye diagram due to the NEXT. However, the time interval between the two crossing points stays the same as the UI. Therefore, DDJ is not generated in the case of the short unit line delay due to the NEXT. However, the total propagation TD along the meander delay line

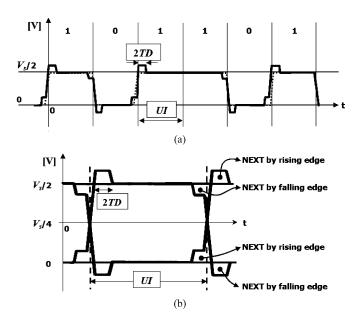


Fig. 12. Case of the short unit line delay in the meander delay line with N unit lines. The input waveform with voltage amplitude of V_s and a rise time of T_r is injected at the input port through a 50- Ω source impedance. (a) Expected output waveform. (b) Expected eye diagram.

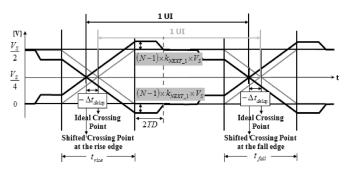


Fig. 13. Expanded eye diagram for the case of the short unit line delay. It can be seen that the crossing points are shifted with a negative timing delay both at the rising and falling edges. It should be noted that DDJ is not produced, even though a negative delay is generated.

is reduced by the amount of $-\Delta t_{\rm delay}$. Hence, a jitter-estimation equation can be suggested for the short delay line case, presented in (21) as follows:

$$t_{\rm jitter} \approx 0$$
 if 2TD < UI (short unit line delay case). (21)

To extract the reduced TD term $-\Delta t_{\rm delay}$, an eye diagram at the rising edge is depicted again in Fig. 14(a). If the meander delay line has N unit lines, then the accumulated NEXT is $(N-1) \times k_{\rm NEXT_1} \times V_S$, as explained in Section IV-A. $-\Delta t_{\rm delay}$ can then be extracted using the triangle principle, as shown in Fig. 14(b). Therefore, the following relations can be obtained:

$$\frac{V_S}{4} : \left\{ \frac{V_S}{4} - (N - 1) \times k_{\text{NEXT-1}} \times V_S \right\}$$

$$= \frac{t_{\text{rise}}}{2} : \left(\frac{t_{\text{rise}}}{2} - \Delta t_{\text{delay}} \right) \tag{22}$$

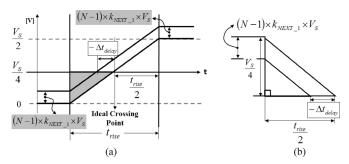


Fig. 14. Extraction of the reduced term of TD $(-\Delta t_{\rm delay})$ for the case of a short unit delay line in the meander delay line with N unit lines. (a) At the rising edge. (b) Triangle calculation principle of the TD $(-\Delta t_{\rm delay})$.

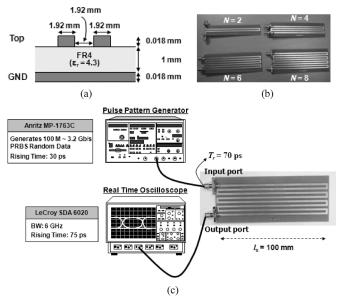


Fig. 15. (a) Cross section of the microstrip type meander delay line. (b) PCB test vehicles. (c) Measurement setup for the verification of the jitter-estimation equations in the meander delay line.

$$-\Delta t_{\text{delay}}$$

$$= -2 \times t_{\text{rise}} \times (N-1) \times k_{\text{NEXT-1}}$$

$$= -2 \times T_{r-N_\text{meander}} \times (N-1) \times k_{\text{NEXT-1}}$$

$$= -2 \times (N-1) \times k_{\text{NEXT-1}}$$

$$\times \{T_r + 2(N-1) \times (\text{TD}_{\text{even}} - \text{TD}_{\text{odd}})\},$$
if 2TD < UI (short unit line delay case). (23)

The designer of the meander delay line with the short unit line delay case should consider this reduced TD $(-\Delta t_{\rm delay})$.

V. EYE-DIAGRAM MEASUREMENTS AND VERIFICATION OF THE JITTER-ESTIMATION EQUATION

To verify the proposed jitter-estimation equation of (20), as suggested in Section IV, timing jitter was measured and compared to the suggested estimations, as shown in Fig. 15. A real-time oscilloscope (LeCroy SDA 6020) was used, which can measure eye diagrams and jitter histograms, along with a pulse pattern generator (PPG: Anritz MP-1763C), which can produce PRBS with a signal rise time of 30 ps. The actual signal rise

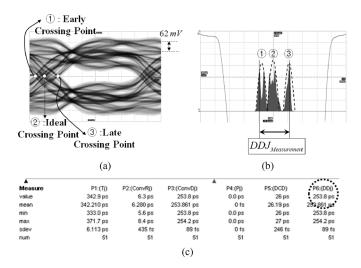


Fig. 16. Eye diagram and jitter measurements for the case of the long unit line delay in the meander delay line with eight unit lines (N=8), where the length of one unit line (l_u) is 100 mm. The data rate of the input data is 1 Gb/s. TD is 0.62 ns and UI is 1 ns. Therefore, this is a long unit line delay case $(2\mathrm{TD} \geq \mathrm{UI})$, as shown in (18). (a) Measured eye diagram. (b) Measured jitter histogram. (c) Measured DDJ value.

time fed into the input port of the meander delay line is 70 ps because of the cable loss. The real-time oscilloscope can extract RJ, DJ, and TJ from the timing-jitter measurements. It also can separate DDJ and PJ from the extracted DJ [5].

In order to verify the proposed jitter-estimation equations, a series of microstrip type test vehicles with the meander delay line were fabricated and tested. In the test vehicles, l_u is fixed to 100 mm. In addition, N is varied from two to eight, as shown in Fig. 15(b), to investigate the suggested jitter-estimation equations that are dependent on N. The eye diagram and the timing jitter for the two cases of the long unit line delay and the short unit line delay were obtained. Since the length of one unit line was fixed l_u , two UIs of the PRBS input data were selected for separation between the long and short unit delay line cases.

A. Eye Diagram and Jitter Measurements for the Case of the Long Unit Line Delay

The timing jitter was first analyzed for the case of a long unit line with eight unit lines (N=8). When N is eight and l_u is 100 mm, the increased rise time due to the even/odd-mode propagation mismatch can be calculated using (15). Furthermore, the NEXT coefficient is evaluated by (10)

$$T_{r_N_{meander}} = 70 \text{ ps} + 2 \times 7 \times (621 - 583) \text{ ps} = 602 \text{ ps}$$

 $k_{\text{NEXT_1}} = 0.016.$

The amount of the timing jitter by the NEXT can then be estimated using the proposed jitter-estimation equation (20). This estimated timing jitter is the DDJ caused by the NEXT in the meander delay line

$$t_{\text{iitter}} = 4 \times 602 \text{ ps} \times 7 \times 0.016 = 270 \text{ ps}.$$
 (24)

Fig. 16 shows the measured eye diagram and the jitter histogram of the meander delay line with N=4 and $l_u=100\,$ mm. As shown in Fig. 16(a), the measured eye-diagram distinctively exhibits three crossing points (\square , \bigcirc , and \bigcirc). The measured timing jitter is then 253.8 ps, as shown in Fig. 16(b) and (c). It can be noted that the measured timing

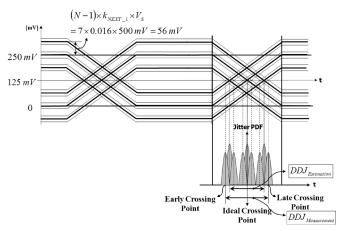


Fig. 17. Blurred eye diagram and the blurred jitter histogram for the case of the long unit line delay to interpret the sub-peaks in the measured jitter histogram caused by the channel loss in Fig. 16.

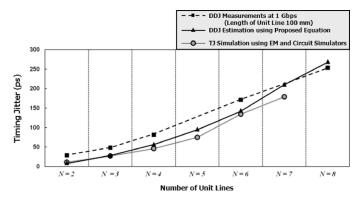


Fig. 18. Comparisons between estimated by the proposed equation simulated by EM/circuit simulator and measured DDJ for the case of the long unit line delay, where $l_u=100\,$ mm. The data rate of the input PRBS is 1 Gb/s. TD is 0.62 ns and UI is 1 ns. Therefore, this is a long unit line delay case (2 TD \geq UI), as shown in (18).

jitter of 253.8 ps is fairly close to the estimated timing jitter in (24) confirming the validity of the proposed analysis and equations. This unique eye diagram with each three high and low levels agrees very well with the analysis of the timing-jitter mechanism by the NEXT through the lossless assumption.

However, as shown in Fig. 16(b), the jitter histogram has sub-peaks inside the main three peaks. These sub-peaks can be produced by blurred NEXT levels and blurred rising edge caused by the channel loss, as described in Fig. 17. Since each NEXT level will blur the same amount, the shape of the sub-peaks will then be like Fig. 17. As discussed in Fig. 10, the jitter histogram is supposed to have three discrete peaks originating from the three crossing points in the eye diagram.

Fig. 18 shows the tendency of the timing jitter highly depending on N. It shows the measured, simulated, and the estimated DDJ for the cases of a long unit line delay with $l_u=100~\rm mm$ and varied N. It should be stated that the NEXT produces a significant amount of the DDJ, as can be seen from the measurements, simulations, and estimations. For the timing-jitter simulation, S-parameters of each pattern were extracted by Ansoft's Design System EM solver, and then they were imported in Agilent's Advanced Design System (ADS). For accurate simulation results, the simulated frequency was from dc to 20 GHz and the accumulated time was 1 μ s (1-ps step). In the

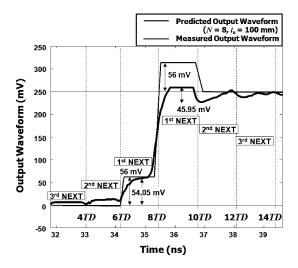


Fig. 19. Predicted and measured output waveform in the meander delay line with N=8 and $l_u=100$ mm.

simulations, the channel was assumed as a lossless line. The simulated timing jitter is the TJ value because DDJ cannot be separated from TJ in ADS. Due to hardware limitation, the case with eight unit lines also cannot be simulated. However, the tendency of simulated timing jitter is also the same for measurement and estimation.

The most obvious fact derived from Fig. 18 is that the DDJ is proportionally increasing with the higher N for the case of the long unit line delay $(2\mathrm{TD} \geq \mathrm{UI})$. The measurements, simulations, and estimations exhibit the same tendency. It is mainly due to the fact that the NEXT is accumulated as the N increases, as expressed in (20). It is also confirmed that the major mechanism to produce the DDJ is the NEXT at the meander delay line for the case of the long unit delay line. The measurements are well matched to the expectations. As a consequence, it can be said that the proposed jitter analysis and estimation equations are adequately reasonable.

From Fig. 18, it can also be seen that the measured DDJ has slightly higher values than the estimated DDJ values. These slightly higher jitter values in the measurement results can be interpreted by analyzing the assumptions employed in the jitterestimation equations. In the proposed analysis, there were some assumptions that the second NEXT and third NEXT are negligible compared to the first NEXT in order to simplify the analysis. However, the second NEXT and the third NEXT can also have some minor effect on the output waveform and the eye diagram. This is the major reason for the slight difference in Fig. 18. To reveal the second NEXT and third NEXT effects, Fig. 19 illustrates the output waveform in the case of single step input signal at the meander delay line with N=8. The predicted waveform and the first NEXT can be obtained using (16) and Fig. 7. As mentioned in Section III, the predicted output waveform does not include the channel loss effect and the corner line section effect. These effects can induce small TD (12.4 ps per one corner line section) and some voltage loss between each NEXT. As a result, it can be the cause that two first NEXTs show a different amplitude of the voltage level.

On the other hand, these effects can be producing island peaks, as can be seen in Fig. 17. If the second NEXT and the third NEXT effects will be considered, the predicted eye

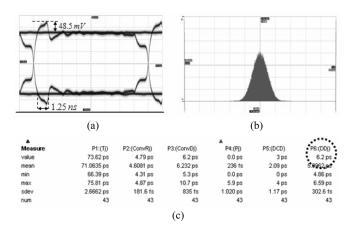


Fig. 20. Eye diagram and jitter measurement for the case of the short unit line delay with N=8 and $l_u=100$ mm. The data rate of the input data is 100 Mb/s. TD is 0.62 ns, while UI is 10 ns, Therefore, this is a short unit line delay case $(2\,\mathrm{TD} < \mathrm{UI})$, as shown in (17). (a) Measured eye diagram. (b) Measured jitter histogram. (c) Measured DDJ value.

diagram and the estimated jitter in Fig. 10 can be much close to the measurements, even though the analysis and equations can become much more complicated. It could be a future research subject.

Considerations on the corner line section effect and the channel loss can also further improve the accuracy of the analysis and estimation. In the current analysis, there is one major assumption that the corner line section (S+2W) in Fig. 2 is much shorter than l_u . Of course, the test vehicles are satisfied with this assumption, $(l_u=100\,\mathrm{mm}\gg(S+2W)=5.76\,\mathrm{mm})$. However, in the real measurement, these effects can lead to additional timing jitter at the measurements compared to the predictions, as seen in Fig. 18.

B. Eye Diagram and Jitter Measurements for the Case of the Short Unit Line Delay

If UI is much smaller than TD, the NEXT does not produce additional DDJ, as discussed in the preceding analysis of the previous sections. To confirm this, the eye diagram and the DDJ were measured for a 100-Mb/s PRBS input with a 100-mm unit line length and N=8. The measured results are shown in Fig. 20. The eye diagram in Fig. 20(a) shows the same waveform shape, as expected in Fig. 13. The measured DDJ in Fig. 20(c) is 6.2 ps, which is very close to the source timing-jitter value (average 6 ps) when the source signal from the PPG is directly measured with the oscilloscope without the meander delay line. This measured DDJ value of 6.2 ps is much smaller than the DDJ (253.8 ps) for the case of the long unit line delay of Fig. 16. This noticeable difference is caused by the fact that the NEXT does not affect the timing jitter for the case of the short delay line, as discussed in Fig. 13. It is also confirmed that the jitter histogram in Fig. 20(b) has a Gaussian distribution and does not exhibit a discrete peak due to the DJ. The expected eye diagram in Fig. 13 shows good agreement with the measured eye diagram in Fig. 20 for the short unit line delay case. Consequently, it is well confirmed that the DDJ is not added by the NEXT in the meander delay line with the short unit line delay.

Furthermore, as shown in Fig. 21, it is confirmed that the DDJ stays almost unchanged even though N increases from 2 to 8.

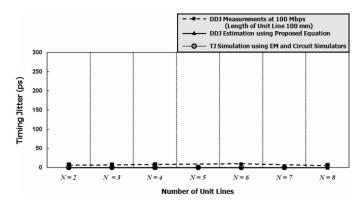


Fig. 21. Comparisons between estimated by the proposed equation, simulated by EM/circuit co-simulation, and measured DDJ for the short unit line delay case with respect to N (from N=2 to N=8) and $l_u=100$ mm. The data rate of the input data is 100 Mb/s.

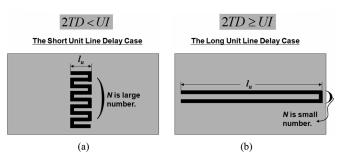


Fig. 22. Two designs of a meander delay line with a fixed total line length and a fixed data rate. (a) Short unit line delay case with small timing jitter. (b) Long unit line delay case with small NEXT.

On the other hand, the DDJ increases with N for the case of the long unit line delay.

If the data rate of the input PRBS is 1 Gb/s and the unit line length of the meander delay line is reduced to 10 mm ($l_u=100$ mm), then TD is 62 ps and UI = 1 ns. Therefore, this is another condition to meet the short unit line delay case (2TD < UI), and the same result of small jitter will be presented as shown in Fig. 21.

Consequently, it can be said that when designing a meander delay line on a PCB, the meander delay line, which meets the condition of the short unit line delay case, as described in (17), is the better choice with respect to minimizing the timing jitter. The rule of thumb in designing a meander delay line with the minimal timing jitter caused by the NEXT is that l_u should be kept as small as possible. On the other hand, increasing N can cause excessive overshoot in the eye diagram of Fig. 13, which is $(N-1)\times k_{\text{NEXT-1}}\times V_S$. Additionally, the meander delay line with the short unit line delay condition will produce the reduced TD term $(-\Delta t_{\text{delay}})$, as discussed in Fig. 14. It should be considered when starting the design process by adding an extra delay line.

There is a tradeoff between the timing-jitter generation by the NEXT and the piled NEXT voltage in the eye diagram, when a meander delay line is designed with a fixed total line-length $(l_{\text{total}} = N \times l_u)$. The short unit line delay case of Fig. 22(a) produces less timing jitter, but it has a large NEXT voltage level. If the number of unit lines is very large and the unit line length is not much larger than the corner line section, the assumption, which is the corner line section is much shorter than the length of the unit line, is not satisfied and the timing jitter is not exactly

estimated. This means that when it comes to the timing-jitter issue, the meander delay line should be designed as the short unit line delay case. However, if the voltage margin is the main concern, the long unit line delay case of Fig. 22(b) is a better design approach.

VI. CONCLUSION

This paper proposed an eye-diagram analysis method and jitter-estimation equations in the densely spaced meander delay line structure used in PCB designs based on the time-domain even- and odd-mode analysis of a coupled transmission line. Eye-diagram distortion and an increased DDJ are caused by EM crosstalk noise between the closely spaced adjacent lines in the meander delay line. In order to verify the proposed eye-diagram analysis and the jitter-estimation equations, a series of microstrip-type test vehicles were fabricated and tested. To further improve the analysis and estimation accuracy further, additional timing-jitter sources at the meander delay line caused by high-frequency dielectric and conductor loss should be accounted. The proposed method can be also applied to analyze eye-diagram distortion and jitter generation in a stripline-type meander delay line structure. The proposed analysis will be used to investigate the eye-diagram distortion and the jitter generation in the case of a 3-D meander delay line structure in a multilayer PCB with vertical vias in order to save the surface area of the meander delay line further. The proposed analysis provides an analytic interpretation approach, which is more efficient than EM/circuit co-simulation.

REFERENCES

- H. Bakoglu, Circuits, Interconnections, and Packaging for VLSI. New York: Addison-Wesley, 1990, ch. 8.
- [2] B. J. Rubin, "Study of meander line delay in circuit boards," *IEEE Trans. Microw. Theory Tech.*, vol. 48, no. 9, pp. 1452–2000, Sep. 2000.
- [3] O. M. Ramahi, "Analysis of conventional and novel delay lines: A numerical study," *J. Appl. Comput. Electromagn. Soc.*, vol. 18, no. 3, pp. 181–190, Nov. 2003.
- [4] Jitter Fundamentals Wavecrest Corporation, Eden Prairie, MN, 2006. [Online]. Available: http://www.wavecrest.com/technical/pdf/ Jitter_Fundamentals.pdf
- [5] "Serial Data Analyzers Manual" LeCory Corporation, Chestnut Ridge, NY, 2006. [Online]. Available: http://www.lecroy.com/tm/ products/Analyzers/SDA/SDA_Brochure.pdf
- [6] R. Wu and F. Chao, "Laddering wave in serpentine delay line," *IEEE Trans. Compon.*, *Packag.*, *Manuf. Technol.*, vol. 18, no. 4, pp. 644–650, Nov. 1995.
- [7] H. Lee et al., "Unit cell approach to full-wave analysis of meander delay line using FDTD periodic structure modeling method," *IEEE Trans. Adv. Packag.*, vol. 25, no. 2, pp. 215–222, May 2002.
- [8] R. Wu and F. Chao, "Flat spiral delay line design with minimum crosstalk penalty," *IEEE Trans. Compon., Packag., Manuf. Technol.*, vol. 19, no. 2, pp. 397–402, May 1996.
- vol. 19, no. 2, pp. 397–402, May 1996.

 [9] W. Guo et al., "Comparisons between serpentine and flat spiral delay lines on transient reflection/transmission waveforms and eye diagrams," *IEEE Trans. Microw. Theory Tech.*, vol. 54, no. 4, pt. 1, pp. 1379–1387, Apr. 2006.
- [10] S. H. Hall et al., High-Speed Digital System Design, A Handbook of Interconnect Theory and Design Practices. New York: Wiley, 2000, pp. 42–73.
- [11] M. Sung et al., "An efficient crosstalk parameter extraction method for high-speed interconnection lines," *IEEE Trans. Adv. Packag.*, vol. 23, pp. 148–155, May 2000.
- [12] K. C. Gupta et al., Microstrip Lines and Slotlines, 2nd ed. Boston, MA: Artech House, 2000, ch. 3.
 [13] W. J. Dally and J. W. Poulton, Digital Systems Engineering. New
- [13] W. J. Dally and J. W. Poulton, *Digital Systems Engineering*. New York: Cambridge Univ. Press, 1998, ch. 6.
- [14] R. Garg and I. J. Bahl, "Characteristics of coupled microstriplines," IEEE Trans. Microw. Theory Tech., vol. MTT-27, no. 7, pp. 700–705, Jul. 1979.

- [15] G. Kim et al., "TDR/TDT analysis by crosstalk in single and differential meander delay lines for high speed PCB applications," in *IEEE Int. Electromagn. Compat. Symp.*, Aug. 2006, vol. 3, pp. 657–662.
- [16] E. Song et al., "Estimation of data-dependent jitter using single pulse analysis method in high-speed differential signaling," in *IEEE Int. Electromagn. Compat. Symp.*, Sep. 2006, vol. 2, pp. 741–746.



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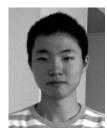
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