Characterization of On-chip Interconnections and Capacitive Coupling Effect on CMOS Operational Amplifier

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***Abstract*— The operational amplifier is one of the most important circuits to compose ADCs, DACs and active filters. Now, there are many papers which deal with noise characters of op amps. Most of them are focused on the input signal noises which flow into circuits without account about noise source. Capacitive coupling is one of the most frequent sources of signal noise. The capacitive coupling is inevitable because of high integration. This paper investigates mechanism of input noises flowing into the op amp and effects of capacitive coupling on the op amp as on-chip interconnection modeling and analytical model of the DC output offset voltage of the OPamp are proposed. Furthermore, the models are verified by experimental measurement.**

I. INTRODUCTION

Recently, CMOS technology is continuously scaled down and more and more devices are highly integrated in a chip [1]. And as operational frequency increases, various noises are generated and couples to circuits. On chip, coupling is one of the most common reasons making a signal worsen. And as integration of circuit increases, coupling among interconnections is not avoidable. The on-chip coupling among interconnections affects circuit performance and deteriorates signal integrity. The dominant coupling is capacitive on the chip [2]. The capacitive coupling effects on delay time and jitter performance of digital circuits. Furthermore, it adds noises on the signal lines and then, deteriorates output of the analog circuits.

The closely located signal can be easily coupled to noise sensitive circuits in the analog chips such as OpAmps, PLL, LNA, ADC, and DAC, resulting in severe degradation of performance and reliability in the wireless communication system. Especially, the OpAmp is the most commonly used circuit among analog blocks such as ADCs, DACs, and active filters, which are essential analog building blocks for implementing the mixed-mode signal systems [3][4]. There are many publications about noise effect on op amp operations [4]-[9], which successfully present and model the noise effect. However, these previous works model and verify without account of the RFI source. In the OpAmp, one of the most crucial properties for determining the performance of the OpAmp is the DC output voltage offset that can lead to fatal system errors or a failure. The most probable mechanism generating this DC output voltage offset in the OpAmp is radio frequency interference (RFI) coupled to a signal input path to the OpAmp circuit. Consequently, it is essential to investigate capacitive coupling effects on the DC output voltage offset of the OpAmp in order to ensure reliable operation and the associated analog blocks.

In this paper, we study the capacitive effect on the OpAmp. In order to model the effect, characterization of on-chip interconnection and coupling mechanism between lines are deemed. Therefore, we propose the scalable models to characterize on-chip interconnections. By combining the scalable models of on-chip interconnections and the analytical model of the OpAmp, we can realize the capacitive effect on the OpAmp. And then, the DC output offset voltage is derived when the digital signal is assigned to the close signal line.

In order to validate the proposed hybrid model, we have designed and fabricated a CMOS negative feedback OpAmp chip, and have mounted it on a package substrate with wire-bonding interconnections. The OpAmp chip was fabricated using a TSMC 0.25 um CMOS process, and the OpAmp chip and package were assembled using a COB technology. We then measured the capacitive coupling effect onto the DC output voltage offset of the CMOS OpAmp and compared the measurement results with the estimations obtained using the suggested modeling approach. For the validation of the proposed models, we have measured the DC output offset voltage by sweeping the aggressor's frequency from 10MHz up to 3GHz. We successfully demonstrated that the experimental results coincide well with the expectations induced from the proposed model. These results demonstrate the necessity of co-modeling and analysis of the interconnection and the circuit.

II. CHARACTERIZATION OF ON-CHIP INTERCONNECTIONS

In this paper, the on-chip interconnection is modeled in R, L, G, C networks with balanced structure. Each R, L, G, C models is obtained analytically. If the length of interconnection is not short and the frequency is high, inductance is not negligible as shown in Fig.. 1. There are two return current paths. The one is the nearest ground or power metal line. The other one is the silicon substrate highly dopped. The dominant path is determined by the frequency and distance between signal and ground.

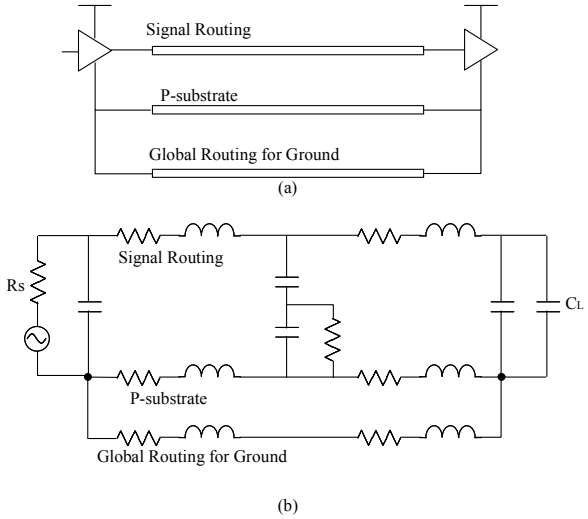

Fig.. 1 (a) Conceptual diagram of the single-ended on-chip interconnection. (b) The models of the on-chip interconnection. R_s is the source resistance of the signal source and C_L is the load capacitance (input capacitance of the driver).

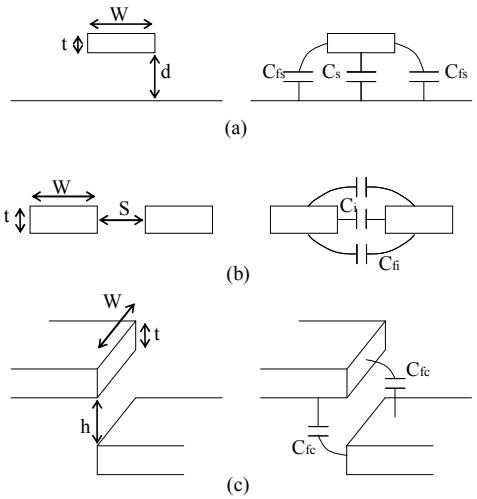

Fig. 2 Capacitance model. (a) Capacitance between a signal metal line and wide metal. C_s is the face to face capacitance and C_{fs} is the fringing capacitance. (b) Capacitance between a signal line and a signal line. Ci is the face to face capacitance and C_{fi} is the fringing capacitance. (c) C_{fc} is the fringing capacitance between edge an edge.

$$C_s = \varepsilon \frac{WL}{d}, \; C_i = \varepsilon \frac{tL}{s} \qquad (1)\ (2)$$

$$C_{fs} = \varepsilon \frac{L}{\pi} \ln\left(\frac{d + t + \sqrt{t^2 + dt}}{s} \right) \qquad (3)$$

$$C_{fi} = \varepsilon \frac{L}{\pi} \ln\left(\frac{s + 2W}{s} \right) \qquad (4)$$

$$C_{fc} = \varepsilon \frac{W}{\pi} \ln\left(\frac{h + t + \sqrt{t^2 + ht}}{h} \right) \qquad (5)$$

The fringing effect should be considered because the width of the on-chip interconnection is relatively small compared with PCB interconnections. C_{fs} and C_{fc} can be derived from [10].

Inductance can be derived as bellows.

$$L_l = \frac{\mu}{\pi} \left(\frac{1}{4} + \ln \frac{d}{W + t} \right) \qquad (6)$$

$$L_p = \mu \frac{hL}{W} \qquad (7)$$

The signal lines are nearly placed and they have an effect on each other. The coupling capacitance can be obtained using eq (2) and (4). The capacitive coupling effect is dominant on the chip [2]. From impedance profile, we can make a decision of the dominant factor. In this case, the capacitance is dominant up to 10GHz. The model is verified with 3D filed solver as shown in Fig. 3.

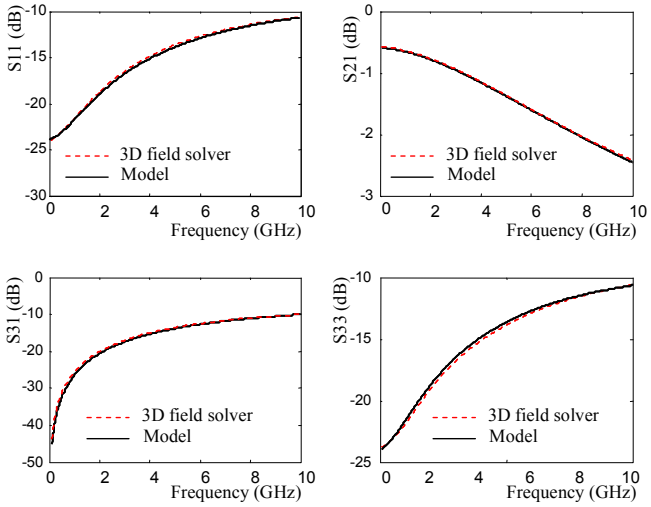

Fig. 3 Comparison of the 3D field solver and the model. The solid lines shows the results of the model and the dash lines indicate 3D field solver.

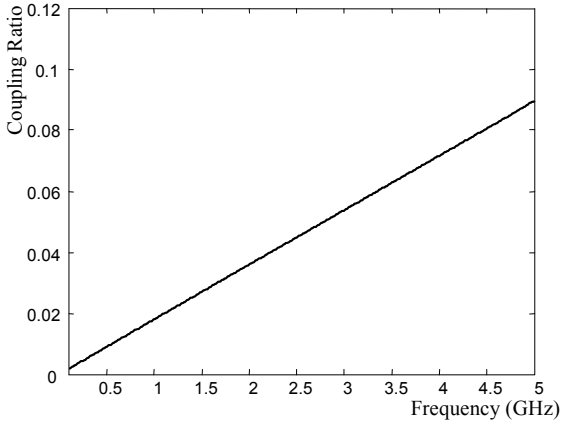

Fig. 4 Capacitive coupling coefficient depending on frequency. The coupling coefficient is the ratio of transfer impedance and self impedance of the aggressor.

The capacitive coupling ratio versus frequency is shown in Fig. 4. If the resistance is small, the capacitive coupling coefficient is constant for every frequency [11]. But the load resistance is large, the coupling effect is dependent on frequency. The coupling ratio is the ratio of transfer

impedance and self impedance. Port 1 is the signal source of the aggressor and port 4 which is the input of the OPamp is the victim.

$$k_c(f) = \frac{Z_{41}(f)}{Z_{11}(f)},\ V_c = k_c(f)V_{in}(f) \tag{8}$$

III. DC Output Offset Voltage bt Input Noise

In this section, we will use analytical equations to show that the noise coupled to the OpAmp input can create the $\Delta V_{DCoffset}$. First, the Drain current I_1 and I_2 of M_1 and M_2 will be derived. The current of the Drain node at the CMOS transistor is expressed using Eq.(9) [12].

$$i_D = \frac{1}{2}k\frac{W}{L}(v_{GS}(t) - V_{th})^2(1 + \lambda v_{DS}(t)) \tag{9}$$

Since the crosstalk noise can be expressed as an AC noise signal, the Gate-Source voltage can be represented as the sum of a DC bias signal, V_{GS}, and an AC coupled noise signal, v_{gs} .

$$v_{GS}(t) = V_{GS} + v_{gs}(t) \quad ,\ V_T = V_{GS} - V_{th} \tag{10)(11}$$

$$v_{gs}(t) = |V_{gs}(\omega)|\cos\omega t \tag{12}$$

We use Eq. (10) to simplify the equations, while V_T is the DC voltage difference between the DC bias voltage of the Gate-Source and the threshold voltage of the MOS transistor. The AC coupled noise of the Gate-Source voltage is a sinusoidal wave as shown in Eq. (11). $\mathbf{V_{gs}(\omega)}$ is the Fourier transform of the v_{gs}. ω is the angular frequency of the coupled noise signal. Thus, the drain current can be expressed as bellows:

$$i_D = \frac{1}{2}k\frac{W}{L}\left[\begin{array}{l} V_T{}^2 + \frac{1}{2}|V_{gs}(\omega)|^2 + (2|V_{gs}(\omega)|V_T\cos\omega t \\ + \frac{1}{2}|V_{gs}(\omega)|^2\cos 2\omega t) \end{array}\right] \tag{13}$$

The Drain current can be divided into three current components as shown in Eq. (13). Three current components are the DC bias current (I_D) component, the DC current (I_d) component produced by the coupling and non-linearity of the CMOS transistor, and AC currents (i_d) component. Then, the DC currents I_1 and I_2 have two DC components as Eq.(14).

$$i_D = I_D + I_d + i_d \tag{14}$$

$$I = I_D + I_d = \frac{1}{2}k\frac{W}{L}V_T{}^2 + \frac{1}{4}k\frac{W}{L}|V_{gs}(\omega)|^2 \tag{15}$$

Imbalance of the DC current between I_1 and I_2 generates the DC output offset voltage.

$$\begin{aligned}\Delta I = &\frac{1}{2}k\frac{W}{L}V_{T1}{}^2 + \frac{1}{4}k\frac{W}{L}|V_{gs1}(\omega)|^2 \\ &-\frac{1}{2}k\frac{W}{L}V_{T2}{}^2 + \frac{1}{4}k\frac{W}{L}|V_{gs2}(\omega)|^2\end{aligned} \tag{16}$$

Therefore, if the capacitive coupling effect to the transistor M_1 and M_2 in the OpAmp circuit is not same, in other words, if $|V_{gs1}(\omega)|$ is not equal to $|V_{gs2}(\omega)|$, we find that it can create the DC voltages offsets at the input and output nodes of the OpAmp as shown in Eq. (17). In other words, the imbalance of the gate-source voltage in M_1 and M_2 can produce $\Delta V_{DCoffset}$. It is obvious that the DC voltage offset, $\Delta V_{DCoffset}$, can be described as a function of v_{gs1} and v_{gs2}.

$$\Delta V_{DCoffset} = \Delta I \cdot (R_1 + R_2) \tag{17}$$

Fig. 5 indicates the equivalent circuit model to analyze the DC output offset voltage.

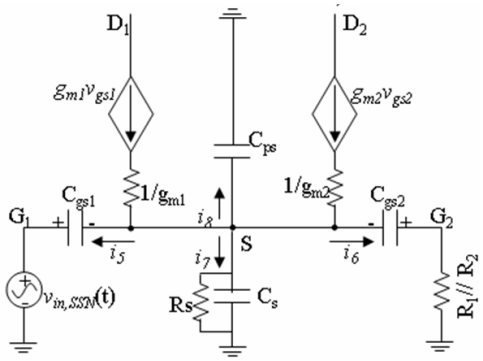

Fig. 5 Equivalent circuit model to analyze the DC output offset voltage

First, we obtain the Gate-Source voltage, $v_{gs1}(t)$ and $v_{gs2}(t)$. The source voltage of M_1 and M_2 is assumed to be $v_s(t)$. Then, by applying the Kirchoff's current law in the equivalent circuit model, we can obtain following equations of Eq. (18)-(24) in the frequency domain.

$$g_{m1}V_{gs1}(s) + g_{m2}V_{gs2}(s) = i_5(s) + i_6(s) + i_7(s) + i_8(s) \tag{18}$$

$$V_{gs1}(s) = V_{in}(s) - V_s(s),\ V_{gs2}(s) = -\frac{V_s(s)}{sC_{gs}R + 1} \tag{19)(20}$$

$$i_5(s) = -V_{gs1}(s)\cdot sC_{gs1} = sC_{gs1}\cdot(V_s(s) - V_{in}(s)) \tag{21}$$

$$i_6(s) = -V_{gs2}(s)\cdot sC_{gs2} = \frac{sC_{gs2}}{sC_{gs2}R + 1}\cdot V_s(s) \tag{22}$$

$$i_7(s) = sC_S\cdot V_s(s),\ i_8(s) = sC_{ps}\cdot V_s(s) \tag{23)(24}$$

Since C_{gs1} equals C_{gs2} and g_{m1} is same as g_{m2}, we can represent C_{gs1} and C_{gs2} as C_{gs}. g_{m1} and g_{m2} are defined as g_m. Therefore, we obtain the Gate-Source voltages of M_1 and M_2, as represented as the following equations Eq. (25) and Eq. (26).

$$V_{gs1}(s) = \frac{-(g_m + sC_{gs})\cdot V_{in}(s)}{(sC_{gs} + g_m)\cdot(1 + 1/sC_{gs}R + g_m) + s(C_S + C_{ps}) + g_m} \tag{25}$$

$$V_{gs2}(s) = \frac{-1}{sC_{gs}R + 1}\cdot\frac{(g_m + sC_{gs})}{s(2C_{gs} + C_S + C_{ps}) + 2g_m}\cdot V_{in}(s) \tag{26}$$

Then, by applying these equations of Eq. (25) and Eq. (26) to Eq. (19), we can derive the graph of the DC output offset voltage caused by the input noise, $v_{in}(t)$. Fig. 6 shows the DC output offset voltage sweeping frequency of the aggressor.

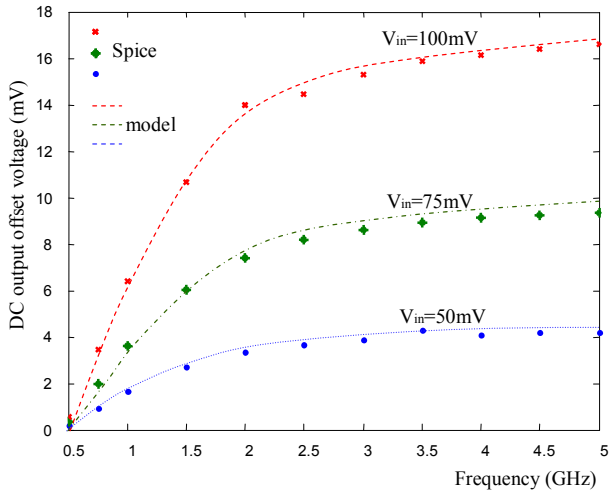

Fig. 6 The DC output offset voltage with the input noise.

IV. Expectation and Experimental Verification

The coupled noise is able to be represented a ratio of transfer impedance and self impedance. Therefore, we can get the DC output offset voltage as the function of transfer impedance and self impedance.

$$V_{in} = V_s k_c(f) = \frac{Z_{41}(f)}{Z_{11}(f)} V_s \tag{27}$$

$$\Delta V_{DCoffset} = f(v_{gs1}, v_{gs2}) = h(V_s, Z_{11}, Z_{31}) \tag{28}$$

After getting coupled noise voltages depending on frequencies by injection of 1V, if the results substitute for output offset formula, it is possible to get the output offset depending on frequencies as Eq (28).

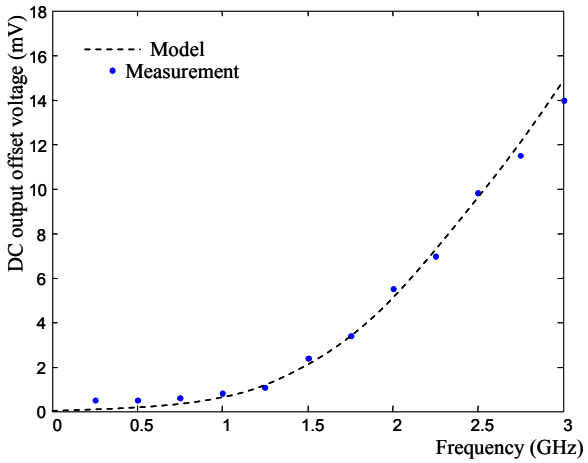

Fig. 7 Comparison of measurement results and proposed models. Circuit points represent measurement results. The dashed show results of the proposed model.

Fig. 7 shows the measurement results and results of the proposed analytical model. Circle points are measurement results and the dashed line shows the DC output offset voltage obtained by the proposed model. It is demonstrated that the DC output voltage offsets from the proposed hybrid model are well matched to the measurements. We also found that both the model and measurement in Fig. 7 exhibit a distinctive behavior compared to the curves in Fig.6. The coupled noise by the aggressor depends on the frequency. As sweeping the frequency of aggressor with the same amplitude for each frequency, the coupled noise increases depending on frequency. Consequently, the DC output offset voltage by capacitive effect is different from the circuit property for the input noise. Furthermore, the effect is not negligible and the DC output offset voltage by the capacitive coupling dramatically increases depending on frequency. As shown in Fig.4, the coupling ratio increases as the frequency rises. Therefore, the DC output offset voltage increases like a square function as shown in Fig. 7. Accordingly, the on-chip interconnection model should be considered and the capacitive coupling effect degrades circuit performance.

V. Conclusion

In this paper, capacitive effect on the operational amplifier is analyzed. In order to, the on-chip interconnection is characterized and the analytical scalable models are proposed. The scalable models of the interconnections are verified with 3D field solver. And the equivalent circuit model and analytical model are proposed to analyze the DC output offset voltage by input noise. We can expect the output offset voltage using these models. And then, the proposed models are verified by experimental measurement.

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