A Ku-band MOSFET Phase Shifter MMIC

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***Abstract* — A Ku-band four-bit MOSFET monolithic-microwave integrated-circuit (MMIC) phase shifter using MOSFET switching elements and transmission line is presented. Electromagnetic simulation and compact circuit were employed to yield an MMIC with a 2.2mm × 1.5mm (3.08mm^2) die size. The measured results exhibit the maximum RMS phase error of about 8 degree and the maximum RMS amplitude error less than 0.5 dB across the frequency band from 11.7 GHz to 12.7 GHz. Typical insertion loss is about 11.1 dB, and input/output return loss is larger than 11 dB.**

***Index Terms* — phase shifter, MOSFET switch, switch model, monolithic microwave integrated circuit(MMIC) .**

I. INTRODUCTION

The microwave control component employed to realize phase shift functions in an electronically scanned array antenna is the phase shifter. Most of the integrated phase shifters reported to date were utilized in gallium arsenide (GaAs) MESFET or pHEMT technology due to excellent switching devices capable of broadband performance and low insertion loss. However, silicon MOSFET continues to scale down device geometries and thereby scale up operating frequencies. Thus, advanced silicon MOSFET devices can now operate at frequencies which in the past relegated to GaAs devices.

A broadband phase shifter can be realized by switching between a low-pass filter and a high-pass filter[1]. For silicon MOSFET phase shifter implementations, MOSFETs are the most readily available switching elements. The source and drain are used as RF terminals, and the gate is used as the bias(switch control) terminal. The MOSFET can be adequately modeled as a resistance in the on state, and as a parallel connected capacitor and resistor in the off state[2].

In this paper, an integrated Ku-band four-bit phase shifter MMIC utilizing 0.18μm n-type MOSFET technology is described. This digital phase shifter is firstly implemented by using CMOS technology over 10 GHz. The four-bit MOSFET phase shifter consists of four different phase shifters with the phase shift of 45°, 90°, 180°, and 22.5° cascaded in a linear arrangement.

II. CIRCUIT DESIGN

A conventional broadband phase shifter is made by switching between separate high-pass and low-pass filters[1]. The switching elements are located external to the filters. In MMIC implementations, passive FETs can be typically used as switching elements. In such a design the off-state capacitance of the FETs tends to degrade the performance and limit the bandwidth of the phase shifter.

The embedded-type phase shifter behaves as either a high-pass or a low-pass filter depending on the states of the various switching elements. By selection of appropriate circuit topologies, it is possible to incorporate switching FET off-state capacitances as filter elements[3]. Since these capacitances are no longer undesired parasitics, high performance and broadband response can be more easily achieved in consideration of them. In our design, an accurate MOSFET switch model is not provided in the frequency range over 10 GHz. Therefore, the development of the MOSFET switch model is essential, to design four-bit phase shifter. And then, four-bit embedded-type phase shifter using developed MOSFET switch model can be implemented.

A. MOSFET Switch Design

Both the insertion loss and isolation level are very important characteristics to determine the switch transfer performances. GaAs switch is often used in practical wireless communications because the insertion loss of GaAs switch is much lower that of MOSFET switch[4]. The large insertion loss of the MOSFET switch is mainly due to the low-resistivity substrate and large on-state resistance in comparison with a GaAs switch[5]. However, it is possible for MOSFET devices to be used as a switching component because of increasing high frequency performance as the continuous and aggressive down-scaling of them.

In the MOSFET switch design, enlarging gate width of MOSFET reduces the on-state resistance, thus improving the insertion loss but increases the substrate parasitics, leading to the degradation of not only the isolation but also insertion loss. Therefore, it is essential to determine

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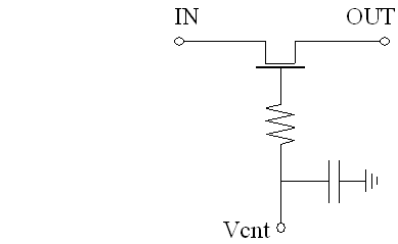
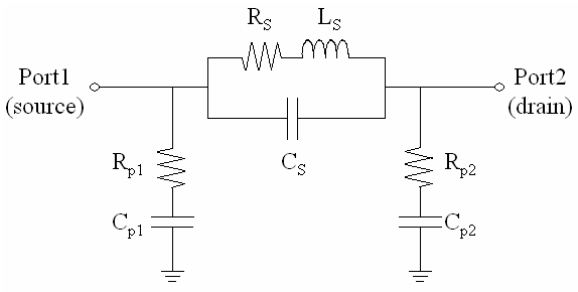
the optimum gate width which provides the minimum insertion loss and sufficient isolation level about each phase bit. We decided the unit gate width of 5μm, minimum gate length of 0.18μm for high yield, and the available number of fingers of 8~64 to obtain the appropriate insertion loss and isolation level at the operating frequency range of 11.7~12.7 GHz.



(a) circuit schematic

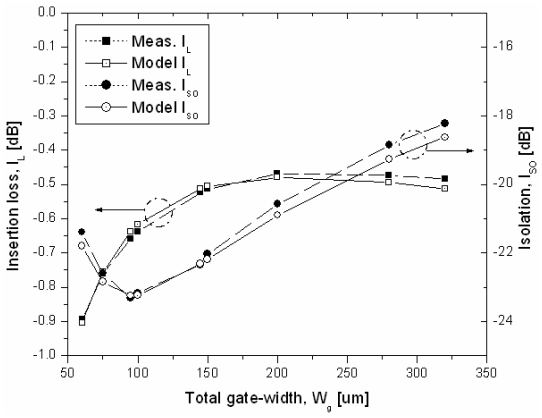


(b) equivalent circuit

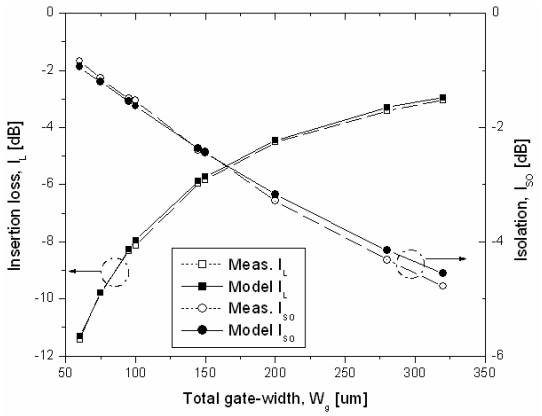
Fig. 1. MOSFET switch schematic and equivalent circuit

The circuit schematic and equivalent circuit are illustrated in Fig. 1. The switching is performed through 2.5 Kohm resistors which provide enough RF isolation between the gates of MOSFET switch and control source. This equivalent circuit is used at on-state condition as well as at off-state condition. In this figure, the resistances R_{P1} and R_{P2} and capacitances C_{P1} and C_{P2} represent parasitic resistances and capacitances resulting from a low-resistivity substrate. The resistance R_S and capacitance L_S are mostly the on-state resistance and parasitic inductance. The capacitance C_S generally denotes the off-state capacitance. Table I lists an example of the equivalent circuit parameters derived from the measured S parameters for a MOSFET switch of the 150μm gate-width.

The measured and modeled transfer characteristics for the MOSFET switch are shown in Fig. 2. The modeled results show good agreement with the measured one. The insertion loss at on-state is minimized at total gate width, W_g=200μm. To design various phase bits such as 22.5°, 45°, and 90°, the scalable switch model was completed as function of the number of fingers. The available number of fingers is from 8 to 64.



(a) on-state condition



(b) off-state condition

Fig. 2. Measured and modeled transfer characteristics

TABLE I
EQUIVALENT CIRCUIT PARAMETERS FOR MOSFET SWITCH OF THE 150UM GATE-WIDTH

	On-state	**Off-state**
R_S [ohm]	4.04	604.1
L_S [pH]	20.6	1.2
C_S [fF]	12.5	97.6
R_{P1} [ohm]	31.9	105.7
C_{P1} [fF]	61.4	30.4
R_{P2} [ohm]	53.1	130.7
C_{P2} [fF]	73.4	20.2

B. Four-Bit Phase Shifter Design

The Ku-band phase shifter described in this paper is comprised of four bits – 22.5°, 45°, 90°, and 180°. The

schematic for the z22.5°, 45°, and 90° phase bit is illustrated in Fig. 3. This circuit uses three MOSFETs and requires two complementary control signals. When gate control voltages V_1 and V_2 are biased at 2 volts and 0 volts, respectively, a high-pass filter with shunt high impedance is realized. When the biases are reversed, a three element T-type low-pass filter is realized. Most of the off-state MOSFET capacitances are incorporated as filter elements. By properly selecting the effective capacitance and inductance values in the filters, various phase shifts may be realized. Transmission lines may be used as inductors. The circuit shown in Fig. 3 does not provide optimal performance as a 180° phase shifter; element values are difficult to realize, and phase variation over the frequency band is excessive.

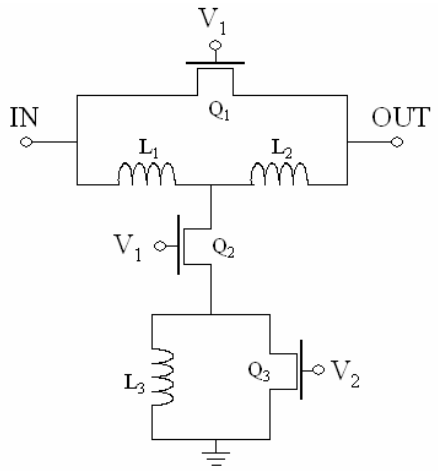


Fig. 3. Schematic for the 22.5°, 45°, and 90° phase bits

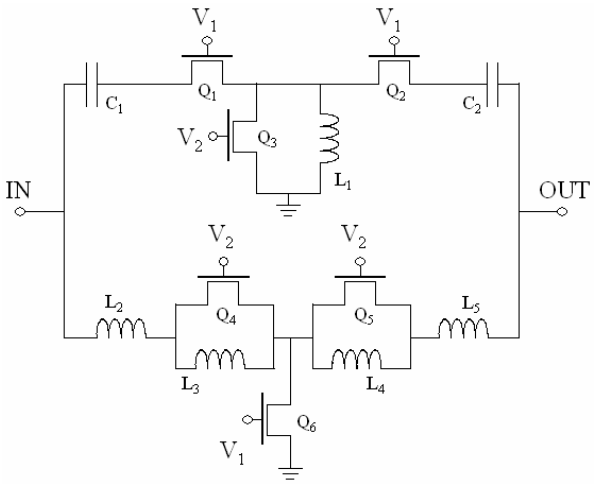


Fig. 4. Schematic diagram for the 180° phase bit

The 180° bit uses the embedded-type topology shown in Fig. 4[3]. When gate biases V_1 and V_2 are at 2 volts and 0 volts, a five element π -type high-pass filter is realized. When the biases are reversed, a five element π -type low-pass filter is realized. The extensive electromagnetic (EM) simulation is utilized to yield the results similar to measured one. All transmission lines are EM simulated. The individual bits were designed and simulated on Agilent ADS and layout was performed on Cadence.

III. Measured Results

The complete four-bit Ku-band phase shifter MMIC chip is shown in Fig. 5. Input/output terminals of each bit were matched to 50 ohms. Then, four-bit phase shifter was easily matched to 50 ohms by cascading each phase bit. The 45° bit was arranged on the left side, the 22.5° bit on the right side, and the 90° and 180° bits on the center. High impedance transmission lines were used as inductors. The chip measures 2.2 × 1.5 mm^2.

The four-bit phase shifter was measured with a computer controlled HP 8510C vector network analyzer connected to a Cascade Microtech Summit probe station. DC probes were used to provide the necessary MOSFET gate biasing and the substrate voltages. The measured S-parameters for all phase states over the 10 ~ 14 GHz band is summarized in Fig. 6 through Fig. 9.

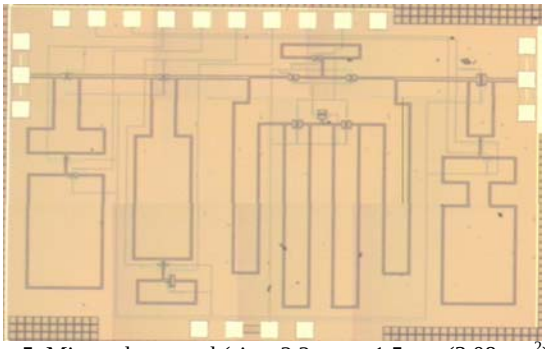


Fig. 5. Micro-photograph(size: 2.2mm × 1.5mm (3.08mm^2))

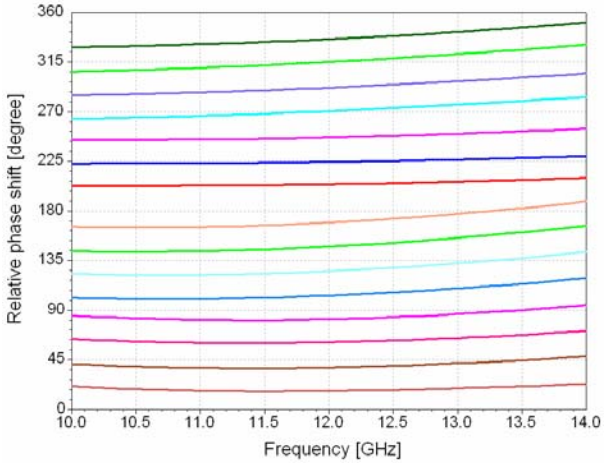


Fig. 6. Measured phase performance

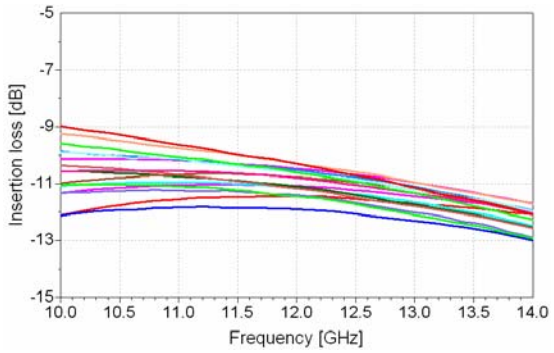


Fig. 7. Measured insertion loss

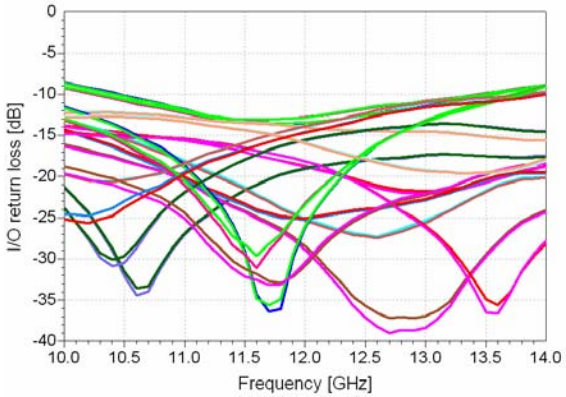


Fig. 8. Measured input/output return loss

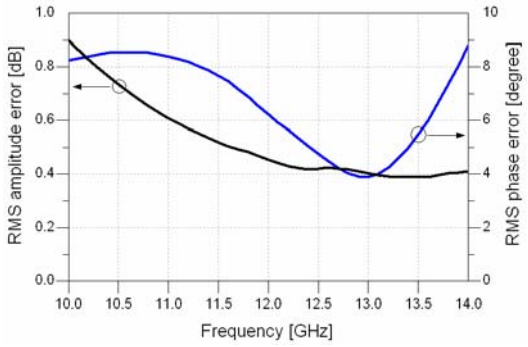


Fig. 9. RMS amplitude error and phase error

For the reference state, all phase bits were switched to the high-pass state. The measured response of phase shift is shown in Fig. 6. We can find an exceptional phase spacing around 180° phase. The 180° phase bit has some phase errors due to the insufficient accuracy of MIM capacitor model provided by foundry's company. Measured insertion loss plotted in Fig. 7 is between 10.2dB and 12.1dB with an overall mean of 11.1dB at the operating frequency range of 11.7~12.7 GHz. The minimum return loss shown in Fig. 8 is 11.3 dB. RMS phase error is less than 8 degrees and RMS amplitude error has a maximum of 0.5dB at 11.7 GHz in Fig. 9.

IV. Conclusion

A four-bit MOSFET phase shifter MMIC by using the developed MOSFET switch model was successfully demonstrated. MOSFET switch model was well validated Extensive EM simulation was employed to yield an MMIC with a 2.2mm × 1.5mm (3.08mm^2). The maximum RMS phase error (8 degree) and amplitude error (0.5 dB) have are measured over the 11.7-12.7 GHz band. Average insertion loss is 11.1 dB, and input/output return loss are larger than 10dB.

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