Novel Current-Mode Background Suppression for 2-D LWIR Applications

Doo Hyung Woo, Sang Gu Kang, and Hee Chul Lee

***Abstract*—A new readout circuit involving two-step current-mode background suppression is studied for two-dimensional long-wavelength infrared focal plane arrays (2-D LWIR FPAs). Buffered direct injection (BDI) and a feedback amplifier are used for the input circuit and background suppression circuit, respectively. The readout circuit has been fabricated using a 0.6-μm 2-poly 3-metal CMOS process for a 64 $\times$ 64 LWIR HgCdTe IR array with a pixel size of 50 μm$\times$ 50 μm. The simple pixel circuit has a very small skimming error of less than 0.3% and low noise characteristics for an adequate calibration range and integration time.**

***Index Terms*—Current copier cell, current-mode background suppression, infrared focal plane array (FPA), readout circuit.**

I. Introduction

INFRARED (IR) focal plane arrays (FPAs) that detect infrared and generate electrical signals are invaluable products that have military, industrial, and medical applications. The design of a high-performance readout circuit that reads electrical signals from the infrared detector is critical for the fabrication of a high quality IR FPA.

In the readout circuit design for an IR FPA, noise performance is a very important concern. The noise of the infrared focal plane array can be classified as photon noise, detector noise, and readout circuit noise. Especially in the HgCdTe detector for long-wavelength regions (from 8 to 12 μm), the noise of the FPA should be dominated by photon noise. In this case, the signal-to-noise ratio (SNR) is proportional to the square root of the integration time [1]

$$i_{ph} = \sqrt{2qI_d\Delta F} \approx \sqrt{2qI_d\frac{1}{2T_{\rm INT}}} = \sqrt{\frac{qI_d}{T_{\rm INT}}} \quad (1)$$

$$\frac{S}{N} = \frac{I_d}{i_{ph}} = \sqrt{\frac{I_d \cdot T_{\rm INT}}{q}} \quad (2)$$

where $i_{\rm ph}$, I_d, ΔF, and $T_{\rm INT}$ are the photon noise current, detector photo current, noise bandwidth, and integration time, respectively.Therefore, it is necessary to use a large integration capacitor for long integration time, but, in a two-dimensional (2-D) application, it is hard to locate a large integration capacitor in the pixel because of area limitation. In addition, a long-wavelength IR (LWIR) HgCdTe detector has a large background current compared to its signal current. To effectively overcome these problems, a current-mode background suppression technique can be used [2]–[4].

In this paper, we suggest a new readout technique involving current-mode background suppression per pixel, which is highly effective for 2-D LWIR applications. Simplicity, reduced skimming error, and low skimming noise are key considerations in our design.

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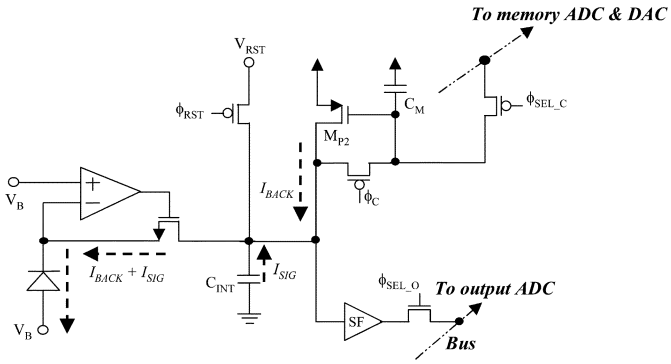

Fig. 1. Pixel readout circuit involving the conventional background suppression method (operation mode; ϕ_c is off).

II. Circuit Implementation

A. Conventional Background Suppression Method

Fig. 1 shows a pixel readout circuit using the conventional background suppression method and a simple current copier cell composed of M_{P2}, C_M, and ϕ_C [2]. The diode-type LWIR detector is connected to the readout circuit using hybrid bonding, and it generates photocurrent for incident photon flux. The input part uses a buffered direct injection (BDI) structure composed of an nMOS transistor and a feedback amplifier because it offers high injection efficiency and a very stable bias for LWIR applications [5]. The feedback amplifier of the BDI can decrease the input impedance by a factor of its open loop gain. Thus, the injection efficiency is increased to near unity. The photocurrent flows through BDI, and it is integrated at integration capacitor $C_{\rm INT}$. $V_{\rm RST}$ and $\phi_{\rm RST}$ are the reset voltage and the reset switch, respectively. The $C_{\rm INT}$ should be reset at every frame before integrating a photocurrent.

In the calibration mode for background suppression, the detector generates background current $(I_{\rm BACK})$ only, and ϕ_c is turned on. Then, the current copier cell copies the background current through controlling the gate voltage of M_{P2}. In the operation mode for signal integration, the detector generates the background current and the signal current used for imaging $(I_{\rm BACK} + I_{\rm SIG})$, and ϕ_c is turned off. Then, the memory

transistor M_{P2} suppresses the background current by means of the voltage of C_M, which was defined in the calibration mode. Therefore, integration capacitor $C_{\rm INT}$ should integrate signal current $I_{\rm SIG}$ only, and the integration time can be increased. In a 2-D FPA, the calibration process needs a mechanical shutter that prevents the IR detector from generating $I_{\rm SIG}$. Therefore, instead of calibrating the $I_{\rm BACK}$ at every frame, it is more efficient to calibrate once before the operation mode. Because the silicon MOS transistor has an inherent leakage current, $V(C_M)$ should be stored in another memory through analog-to-digital (A/D) conversion during calibration and should then be refreshed periodically through digital-to-analog (D/A) conversion during operation. In Fig. 1, SF and $\phi_{\rm SEL\_C}(\phi_{\rm SEL\_O})$ are a source follower for transferring analog data and a control switch for multiplexing, respectively.

Now, we should consider skimming error, which refers to copying error for the background current. The skimming error is a residue of the background current and itself a fixed pattern noise, and it makes correcting offset nonuniformity difficult. Moreover, skimming error decreases integration time, especially when the $I_{\rm SIG}$ level is very low. In this case, the theoretical limit of the minimum detectable signal current $(I_{\rm MIN})$ can be represented by noise level

$$I_{\rm MIN} \approx \sqrt{\frac{qI_{\rm BACK}}{T_{\rm INT\cdot MAX}}} = \sqrt{\frac{qI_{\rm BACK}I_E}{(V_{\rm SWING}C_{\rm INT})}} \qquad (3)$$

where $T_{\rm INT\cdot MAX}$, I_E and $V_{\rm SWING}$ are the maximum integration time, skimming error current, and maximum output voltage swing, respectively. Therefore, it is necessary to reduce the skimming error as much as possible. Skimming error is mainly due to the clock feedthrough from $\phi_{\rm SEL\_C}$ in Fig. 1, and this error can be reduced using a large C_M value, a small W/L ratio of M_{P2}, and/or other complex circuitry. However, the area size of the pixel readout circuit is generally limited for 2-D applications. Another important source of skimming error is the channel length modulation effect of M_{P2}, because the drain voltage of M_{P2} in the operation mode is different from that in the calibration mode.

Next, we should consider the noise of $V(C_M)$ caused by D/A conversion during refreshing. Unlike skimming error, this refreshing noise of $V(C_M)$ causes random noise for signal integration. It is very hard to reduce this random noise in the conventional method because a very small W/L ratio of M_{P2}, and an ultralow-noise D/A converter (DAC) must be used.

B. Two-Step Background Suppression Method

Fig. 2 shows a novel pixel readout circuit using two-step background suppression method that is more effective for 2-D LWIR applications than the conventional method. BDI is used for the input part, and the background suppression part uses a feedback amplifier structure that can minimize skimming error due to the channel length modulation of M_{P2} in Fig. 2 [6]. To relieve the pixel area limitation, time-shared BDI is used for both input and background suppression.

The circuit operation of the two-step method is similar to the conventional method. In the calibration mode, ϕ_c is turned on, then the background current is roughly copied by a global current mirror $\rm CM_1$ (first step), and the remainder in each pixel is copied exactly by controlling $V(C_M)$ through the feedback loop

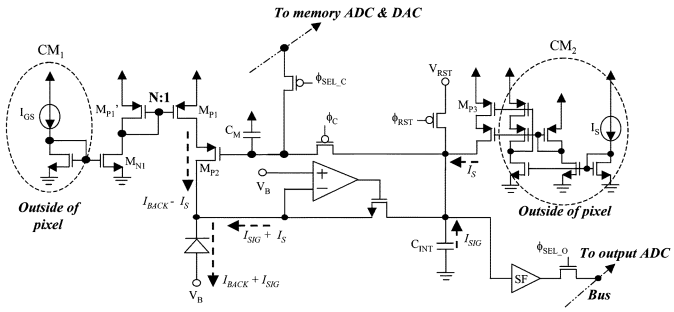

Fig. 2. Pixel readout circuit involving two-step background suppression method (operation mode; ϕ_c is off).

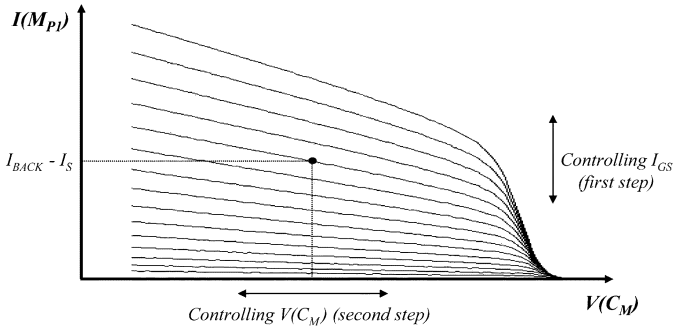

Fig. 3. Characteristic curve of current copier cell for two-step background suppression method.

(second step). Fig. 3 shows the characteristic curve of current copier cell. $I_{\rm GS}$ is controlled to flow as the approximate average value of the background current in the whole array. Next, in the operation mode, the ϕ_c is turned off, then the memory transistor M_{P2} suppresses the background current by means of $V(C_M)$ which was defined in the calibration mode. The global current mirror CM_2 generates a small current I_S, which prevents the feedback loop from turning off in the calibration mode. Moreover, without I_S in the operation mode, BDI input will be turned off when $I_{\rm SIG}$ is a negative value, and it will have low injection efficiency when $I_{\rm SIG}$ is a small value. This global current should always flow as fixed value, so it is designed as a stacked current mirror that is free from channel length modulation and does not affect signal integration in the operation mode. Therefore, the integration capacitor $C_{\rm INT}$ should integrate signal current $I_{\rm SIG}$ only in the operation mode.

Compared with the conventional method, the memory transistor M_{P2} has a very small voltage-to-current conversion gain $(I\text{–}V)$ in the two-step method because it has a large resistor (output resistor of M_{P1}) at its source node. This $I\text{–}V$ value is approximately the same as the reciprocal of the output resistance of M_{P1}. The skimming error that is due to clock feedthrough and the refreshing noise that is due to the D/A conversion affect $V(C_M)$. Therefore, these nonideal effects can be reduced extensively by the two-step method. The circuitry is simple and takes up only a small area, which makes it suitable for 2-D applications.

Fig. 4(a) represents a block diagram of the entire readout circuit. We designed the readout circuit for a 64×64 test array. To minimize pixel area limitation and to maximize the efficiency of the two-step background suppression method, four neighboring pixels are united. They share one input readout circuit, and each

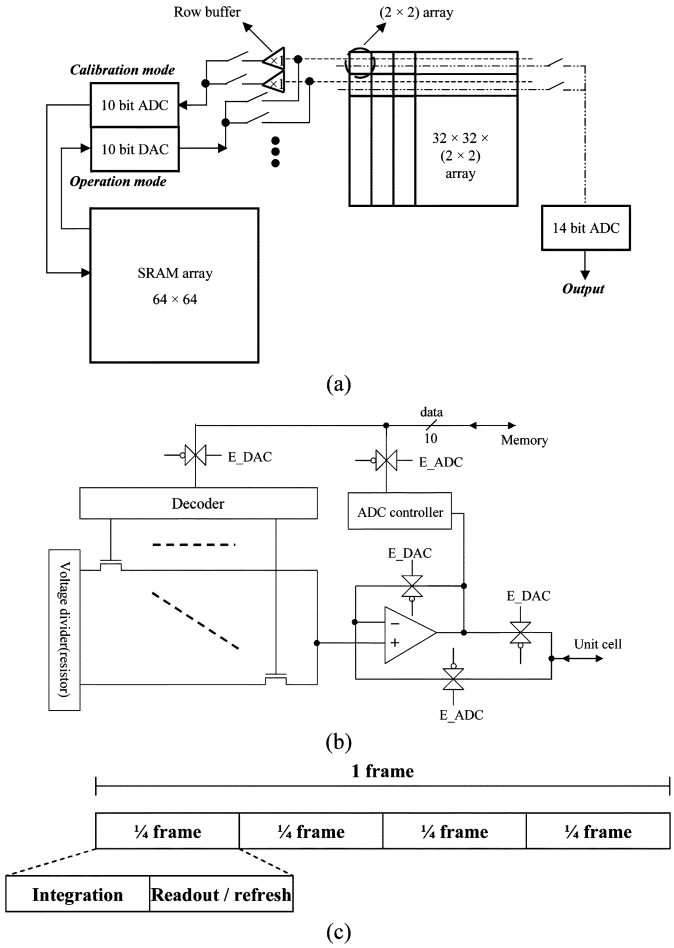

Fig. 4. Entire readout circuit for background suppression. (a) Entire readout circuit. (b) 10-b ADC and DAC. (c) Simplified timing diagram for operation mode.

detector of 2×2 array has a multiplexing switch. Therefore, we can have a large integration capacitor of about 7 pF and an integration time of over 2 ms. In the calibration mode, the $V(C_M)$ in each pixel is stored in an SRAM array through a 10-b A/D converter (ADC). In the operation mode, the $V(C_M)$ in each pixel is refreshed periodically in a regular sequence through a 10-b DAC. The readout circuit has another advantage for the A/D conversion in that the range of $V(C_M)$ is larger than that of previous designs. To reduce total calibration time, we use a row buffers and process the calibration column-by-column. The image data is digitized by a 14-b pipelined ADC.

Fig. 4(b) represents a schematic diagram of the 10-b ADC (DAC). This ADC structure is a successive approximation type, and the DAC is a decoder-based resistor string type. In Fig. 4(b), E_ADC and E_DAC switches enable ADC and DAC operation, respectively. The ADC has the same transfer curve as the DAC in this structure because the ADC and DAC share the decoder, resistors, and amplifier. Therefore, it is possible to store and refresh special voltage irrespective of integral nonlinearity error (INL). The differential nonlinearity error (DNL) and the least significant bit (LSB) are more important in this case. The 10-b ADC (DAC) generates the quantization error, which is another source of the skimming error, and it should be much smaller than the total skimming error.

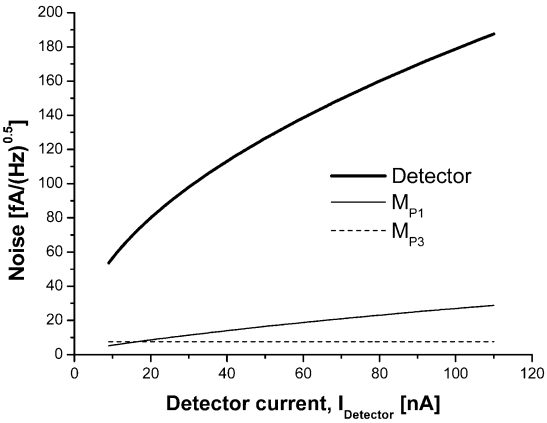

Fig. 5. Noise current characteristics versus the detector current.

Fig. 4(c) shows a simplified timing diagram for operation mode. One frame is composed of four quarter frames because four neighboring pixels (2×2 array) share one input readout circuit. A quarter frame is divide into two parts. One is an integration period, and another is for transferring image data and refreshing calibration data of background current.

C. Other Design Considerations

The global current $I_{\rm GS}$ is mirrored in each pixel, but its value varies slightly among pixels because of a threshold voltage $(V_{\rm th})$ mismatch of the current mirror. If the gate length of M_{P1} in Fig. 2 is not short enough, the current copier cell cannot cover the variations of the global current and the background current in each pixel. However, if we used only M_{P1} in each pixel for current mirroring, the current mismatch would be worse for the difference of $V_{\rm th}$ as the gate length of M_{P1} decreases. To make matters worse, because M_{P1} operates in the subthreshold or weak inversion region in our application, current mismatch is a very serious problem. To overcome these problems, we use two current mirrors as shown in Fig. 2. M'_{P1} and M_{P1} can be well matched because they are in a same pixel, and the matching ratio is $N(N \approx 10)$. Now, M_{N1} operates over the subthreshold region, and the W/L ratio of M_{N1} could be small enough to reduce the current mismatch. The expected current mismatch of the current mirroring is below 20% for a $V_{\rm th}$ mismatch of 50 mV.

The noise current characteristics at $M_{P1}(M_{P2})$ and M_{P3} are very important because the goal of background suppression is enhancement of the SNR. Fig. 5 shows the simulation result of noise current at the detector, $M_{P1}(M_{P2})$, and M_{P3}. Using (1), the noise current of the detector can be calculated. The noise current at $M_{P1}(M_{P2})$ and M_{P3} is much smaller than the detector photon noise, as shown in Fig. 5.

III. Measurement Results

The readout circuit has been fabricated using a 0.6-μm 2-poly 3-metal CMOS process for a 64×64 LWIR HgCdTe detector array with a pixel size of 50 μm$\times$ 50 μm. The microphotograph of the fabricated FPA is shown in Fig. 6. The total die size is 4.7 mm $\times$ 4.5 mm with the exception of test patterns and I/O pads. The total power consumption is approximately 11 mW in the operation mode except for the 14-b ADC, which consumes

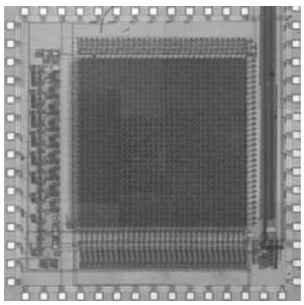

Fig. 6. Microphotograph of the fabricated 64 × 64 FPA.

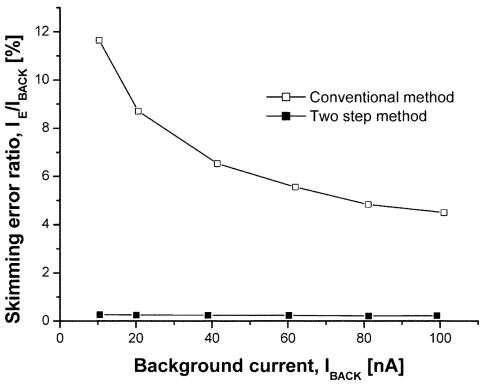

Fig. 7. Ratio of skimming error to background current for conventional and two-step background suppression methods.

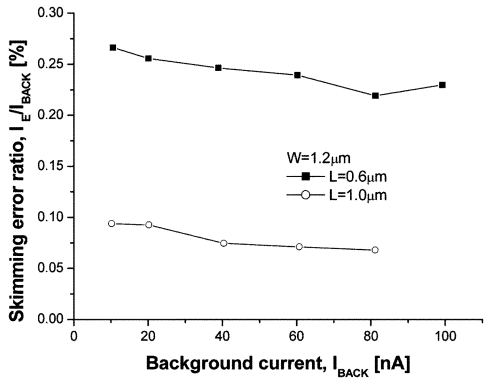

Fig. 8. Skimming error ratio of the two-step background suppression method for two different cases.

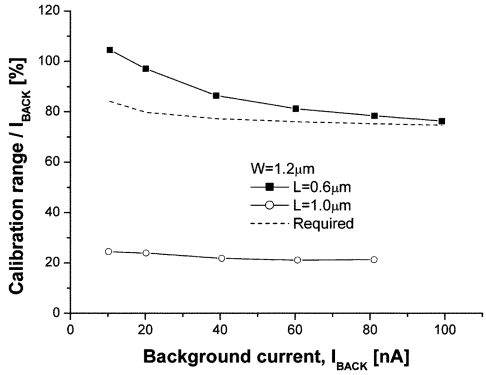

Fig. 9. Normalized calibration range of the two-step background suppression method for two different cases, as in Fig. 7.

approximately 40 mW of power. The operating temperature of LWIR HgCdTe FPA is 77 K.

Instead of using the background suppression method, we can lay the integration capacitor outside of the pixel array and share it for one column. However, the integration time would be limited by the overall frame rate in this case; the integration time can be estimated to be 130 μs for a frame rate of 60 Hz. By means of using the background suppression method, we can improve the integration time by more than 2 ms.

A. Skimming Error and Calibration Range

Fig. 7 shows the ratio of skimming error (I_E) to background current (I_{BACK}) versus the background current. As shown in this figure, the skimming error of the conventional method is very large because the I–V value of M_{P2} in Fig. 1 is not small enough, especially in 2-D applications and in cryogenic temperatures. Therefore, the conventional method is not effective enough for our application. However, the I–V characteristics of M_{P2} in Fig. 2 can be controlled with the gate length of M_{P1}. Therefore, the two-step method can reduce skimming error remarkably, as shown in Fig. 7.

Fig. 8 shows the skimming error ratio of the two-step method for the two different gate lengths of M_{P1}. The I–V value of M_{P2} decreases as the gate length increases because the output resistance of the M_{P1} increases; therefore, the skimming error decreases as the gate length increases. We should now consider the calibration range of the current copier cell, which refers to the available range for covering the variations of background current. The current copier circuit in each pixel should cover an adequate range of the background currents because the background current in each pixel is not uniformly distributed throughout the whole array. In the two-step method, the requirement of the calibration range can be expected from detector nonuniformity, I_{GS} mirroring mismatch, and current copier cell nonuniformity. We calculated this requirement for the worst case, which is represented in Fig. 9. This figure shows the normalized calibration range versus the mean value of the background current. It is found that increasing the gate length of M_{P1} decreases the calibration range as well as the skimming error. Therefore, we should optimize the gate length of M_{P1}. According to Figs. 8 and 9, we can expect a very small skimming error of below 0.3% for an adequate calibration range if we use the two-step background suppression method.

B. Noise From Storing and Refreshing

As previously mentioned, the $V(C_M)$ value in each pixel should be stored and then refreshed. Fig. 10 shows the transfer characteristics of a 10-b ADC for storing $V(C_M)$ in each pixel. LSB, DNL, and INL characteristics of the ADC were calculated from Fig. 10, and conversion noise was estimated from 10 000 samples for some fixed input values. As mentioned before, INL characteristics are unimportant, but LSB, DNL, and noise characteristics are important in our application. The quantization noise of the ADC is shown in Fig. 11, and it can be calculated from LSB, DNL, and noise characteristics. The quantization noise affects the total skimming error, so it is associated with fixed pattern noise. Therefore, we designed the ADC so the quantization noise is much smaller than the skimming error that is due to other effects. The skimming error data in Fig. 11 are

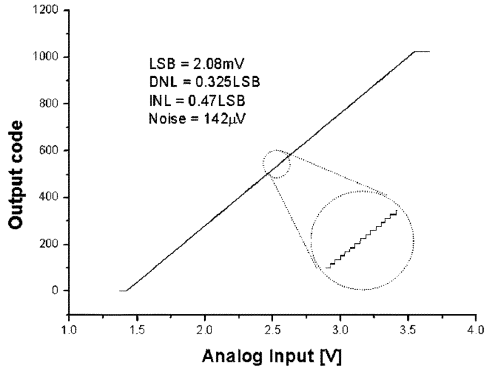

Fig. 10. Transfer characteristics of a 10-b ADC.

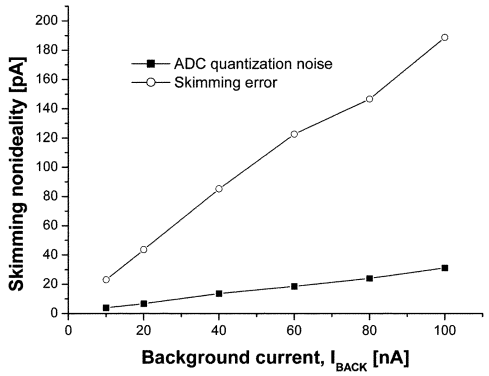

Fig. 11. Quantization noise of ADC and the skimming error due to other effects.

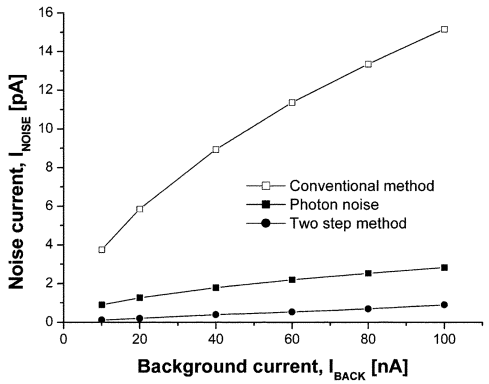

Fig. 12. Refreshing noise due to DAC.

for the two-step method when the gate length of M_{P1} is 0.6 μm. The square ratio of quantization noise to total skimming error is below 2%, as shown in Fig. 11.

Fig. 12 shows the noise characteristics due to DAC for refreshing $V(C_M)$ in each pixel. The random noise of DAC affects the skimming current, the signal integration, and final output signal. Therefore, the DAC output noise effect is very important because our goal is enhancing the SNR of the final output signal. In the two-step method, the current noise caused by DAC is much less than the detector photon noise, as shown in Fig. 12. It satisfies the 95% background limited performance condition. However, the current noise is much larger than the photon noise in the conventional method. In other words, current-mode background suppression can increase total noise rather than decrease it in the conventional method.

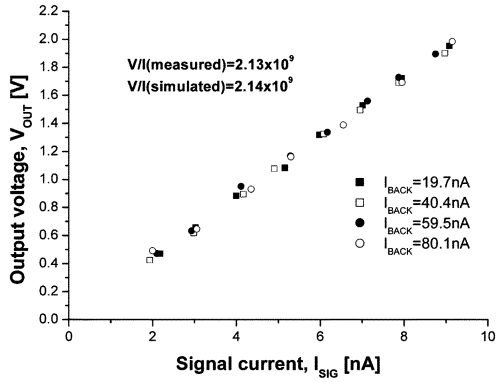

Fig. 13. Transfer characteristics of signal current for different background currents.

C. Transfer Characteristics of the Signal Current

Fig. 13 shows transfer characteristics of the signal current for different background currents in the readout circuit involving the two-step background suppression method. The measured transfer gain $(I_{\mathrm{SIG}}/V_{\mathrm{OUT}})$ is 2.13×10^9 and the expected one is 2.14×10^9 for the integration time of 1.5 ms.

IV. Conclusion

In this paper, a readout technique was studied for a 2-D LWIR HgCdTe detector. To increase the integration time and to reduce the skimming error for a limited pixel area, we proposed a novel readout circuit involving a two-step current-mode background suppression method. This method can effectively increase the SNR of image data because of its low noise characteristics. The readout circuit is expected to offer a very small skimming error $(<0.3\%)$ and long integration time $(>2\ \mathrm{ms})$ for an adequate calibration range.

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