A 2.4-GHz Sub-mW CMOS Current-Reused Receiver Front-End for Wireless Sensor Network

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***Abstract* — In this paper we report a 2.4 GHz low-power receiver front-end using current-reused folded-cascode scheme. Two fully integrated receiver front-ends are presented as a proof of concept. A conventional merged LNA and single-balanced (SB) mixer shows a conversion gain of 20.4 dB and a noise figure of 19 dB at 10 MHz intermediate frequency (IF), taking 500 μA bias current from 1.0 V power supply. The proposed front-end achieves a conversion gain of 30.5 dB and a noise figure of 10.2 dB at 10MHz IF with the same power consumption of 500 μW. The front-ends performances are compared with the previously reported low-power front-ends operating at similar frequency.**

***Index Terms* — LNA, Mixer, Front-end, Current-reusing, Folded-cascode, Flicker noise**

I. INTRODUCTION

The modern disposable wireless sensor network (WSN) markets have put great demands on low-power RF transceiver operating in ISM (Industrial, Scientific, and Medical) bands. These transceivers require a high level of energy efficiency to operate continuously over durations greater than one year while using only a single battery. Especially, low-power implementation of RF receiver front-end circuit is a key issue, because the receiver front-end has to be constantly turned on for waiting for a wake-up signal. However, it is challenging to achieve a required system performance in such a low-power front-end of WSN, where the maximum power consumption should be lower than mW. This issue is caused by the trade-off between power consumption and system performance.

Fig. 1 shows two configurations of conventional front-end architectures: (a) a cascaded LNA and SB mixer scheme and (b) a merged LNA and SB mixer scheme. In the aspects of performance of a noise figure (NF), a cascaded LNA and SB mixer is a better performer because the noise contribution of the mixer can be screened by the high voltage gain of the LNA; however, its high power consumption has been a significant obstacle to its use in low-power applications. On the other hand, the merged LNA and SB mixer has been widely used in sub-mW receivers because it can reduce power consumption effectively by removing the DC current path flowing into the LNA [1-2]. However, a problem occurs when a RF signal is directly applied to the mixer input without signal amplification like a merged LNA and mixer. This results in a low gain and a high NF which significantly hampers the entire receiver performance.

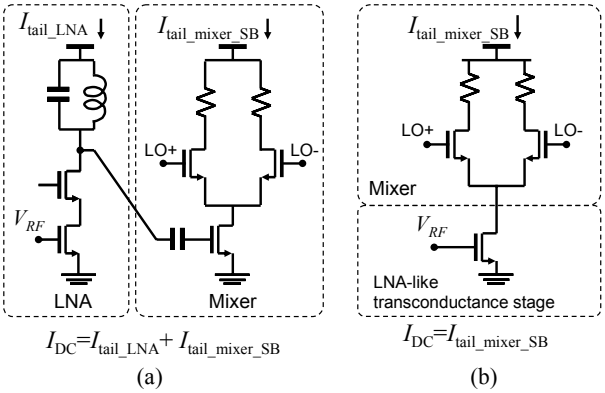

Fig. 1. Conventional front-end configurations (a) a cascade of LNA and SB mixer (b) merged LNA and SB mixer

In this paper, we propose a 2.4 GHz current-reused folded-cascode scheme for sub-mW receiver front-end in WSN applications to achieve both high gain and low noise figures while maintaining a low power operation.

In the next section, we will briefly describe the specifications of receiver in WSN. In section III, the proposed current-reused front-end architecture is presented. In section IV, measurement results from two front-end architectures are compared to prove the proposed concept. Finally, summary and conclusion will follow in section V.

II. SYSTEM CHARACTERISTICS

A. Architecture and Modulation Scheme

Direct conversion architecture is better suited for system integrity and channel selectivity compared with heterodyne or super-regenerative receiver, although it has its own drawback of a high sensitivity to flicker noise [3]. This effect can be suppressed by using a frequency shift keying (FSK) modulation with large modulation index. Moreover, FSK is the most power-efficient modulation scheme because FSK modulated signals can be amplified by non-linear power amplifiers (class E and F) with no spectral regrowth in a transmitter.

B. Receiver Specifications

This work targets on design of receiver front-end for indoor applications, which have the maximum distance between two sensor nodes of 20 m. And a 2.4 GHz ISM band is selected as a carrier frequency to use in all part of Europe and USA, and to minimize antenna size. Then, the maximum path losses between two sensor nodes is given by

$$L_{path}(R) = 10\log\frac{(4\pi)^2 \cdot R^n}{\lambda^2} + L_{atten.} \qquad (1)$$

where R is the maximum distance of 20 m, λ is the wave-length of 2.4 GHz, n and $L_{atten.}$ are the scattering exponent and the attenuation parameter, respectively. Assuming that n is 4 and $L_{atten.}$ is 10 dB in indoor application, the maximum path losses is about 100 dB. Considering power efficiency of transmitter and receiver performance, we have determined the receiver sensitivity of -90 dBm and the transmission power of 10 dBm.

Relatively low data rate of 100 kbps and high BER of 10^{-3} are appropriate for WSN because sensor nodes detect and transmit data of slowly varying physical quantities. Therefore, system noise figure (NF) of 20 dB is an enough value with margin, corresponding to a minimum signal-to-noise ration (SNR) at the non-coherent FSK demodulator of 11 dB. Table I shows that the summary of the specifications of the WSN of this work.

TABLE I
SPECIFICATIONS OF WSN

Item	Spec.	Item	Spec.
Frequency	2.4 GHz	Sensitivity	-90 dBm
Data rate	100 kbps	BER	10^{-3}
Bandwidth	100kHz	SNR	11 dB
Transmit power	10 dBm	NF	20 dB

III. THE PROPOSED CURRENT-REUSED FRONT-END

A. Circuit Implementation

Fig. 2 shows the configuration of the proposed current-reused folded-cascode receiver front-end. To prevent RF performance degradation caused by the absence of LNA, both a LNA and a mixer are implemented in the proposed front-end. In addition, in order to achieve low power consumption, we removed the DC current path from the power supply to the LNA. Instead, we have stacked a mixer above the LNA and inserted a large bypass

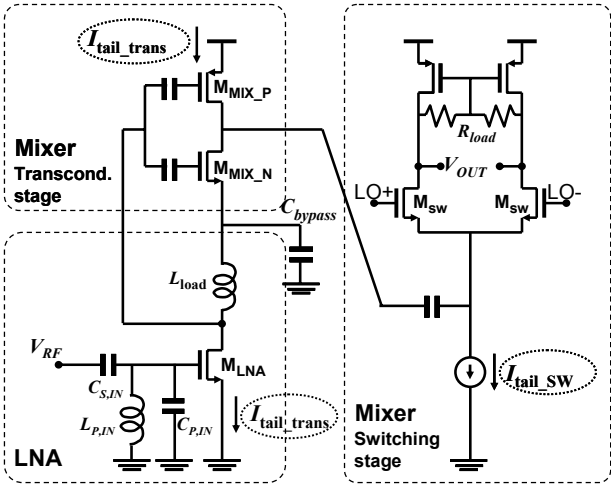

Fig. 2. The proposed current-reused folded-cascode front-end

capacitor (C_{bypass}) between the LNA and the mixer, as this will provide a reliable AC ground. In this scheme, the LNA operates by only reusing the DC bias current of the mixer without any additional power consumption. However, if a LNA and a SB mixer are vertically stacked, there may not be much voltage headroom because many transistors would be stacked between V_{DD} to ground. In order to address this problem, we have employed a folded-cascode mixer instead of a SB mixer, as shown in Fig. 2. The LO switching stage current of I_{tail_SW} doesn't flow into the LNA, and the LNA only reuses the transconductance stage current of the mixer (I_{tail_trans}). Fortunately, the LO switching stage of the folded-cascode mixer can operate only with much lower DC current, as compared to the transconductance stage. This means that most of the DC bias current flows into the LNA so as to reuse the bias current. In addition, we have utilized an inverter-type transconductance stage instead of a conventional single nMOS transistor to enhance the gain of the mixer [4]. Therefore we can achieve better RF performance compared to those of a cascaded LNA and SB mixer with this implementation of the LNA and mixer with the inverter-type transconductance stage. This uses no more than the amount of power used in the merged LNA and SB mixer, as it reuses the DC bias current.

B. Noise Immunity Characteristics

Noise figure improvement of the proposed front-end can be explained from two points of view. First, the large voltage gain of LNA sufficiently suppresses white and flicker noises modulated by the mixer. Second, a folded-cascode mixer is intrinsically less influenced by flicker noise, which is the dominant noise source in direct-conversion receivers. In a fully symmetric differential mixer, the output signal is only affected by flicker noise generated in the switching stage [5]. In a commutating mixer, the flicker noise generated from the switching pair (M_{SW}) slowly modulates zero-crossing points in each switching pair as shown in Fig. 3. Flicker noise makes the time of the zero-crossing of LO signals advanced by [5]

$$\Delta t = \frac{V_n(t)}{S} \tag{2}$$

where $V_n(t)$ is flicker noise voltage and S is the slope of the LO voltage at the switching time. Thus, the frequency spectrum of flicker noise at the mixer output is given by

$$i_{o,n}(f) = \frac{4I_{tail\_SW}}{T}\Delta t = I_{tail\_SW} \cdot \frac{4V_n(f)}{S \times T} \propto I_{tail\_SW} \tag{3}$$

where I_{tail_SW} is the DC tail current in the switching stage, and T is the period of the LO signal. This equation demonstrates that one way of lowering the mixer flicker noise is to reduce the DC current of the switching stage. Unfortunately, in a SB mixer, the bias current should be large enough to obtain a sufficient voltage gain. This is because the switching current eventually is supplied to the transconductance gain stage. However, in the proposed folded-cascode mixer, the switching current can be drastically reduced without any loss of voltage gain because the transconductance stage and the switching stage are separated in DC biasing. Therefore, the noise voltage at the mixer output caused by flicker noise is decreased by the ratio of $I_{tail\_SW\_Folded}/I_{tail\_SW\_SB}$ compared with SB mixers, where $I_{tail\_SW\_Folded}$ and $I_{tail\_SW\_SB}$ are DC bias current in the switching current of the folded-cascode mixer and SB mixer, respectively.

SNR degradation caused by flicker noise can be also reduced by increasing the voltage gain in the receiver front-end. The proposed front-end can achieve $2\cdot(g_{m\_LNA}\cdot\omega_0 Q_{load} L_{load})$ times higher voltage gain than the conventional merged LNA and SB mixer under the assumption that nMOS and pMOS transconductances in the inverter circuit are the same. Therefore, the total SNR improvement of the proposed front-end over the merged LNA and SB mixer can be given by

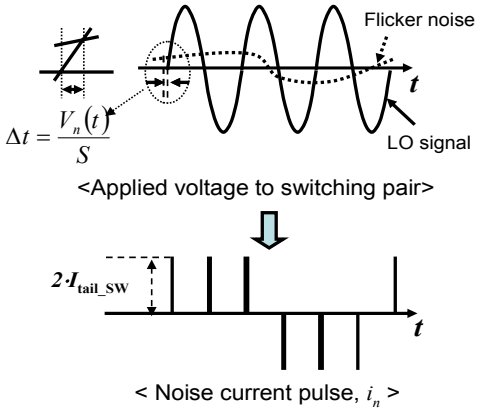

Fig. 3. Noise current generated by flicker noise at mixer output

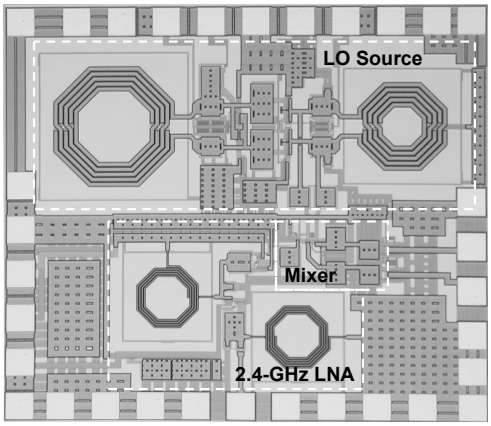

Fig. 4. Fabricated current-reused folded-cascode receiver front-end and LO source (1.6×1.45 mm^2 including pads)

$$2 \cdot \left(g_{m\_LNA} \cdot \omega_0 Q_{load} L_{load}\right) \frac{I_{tail\_SW\_SB}}{I_{tail\_SW\_Folded}} \tag{4}$$

Equation (4) ensures that the proposed front-end will be much more immune to flicker noise as well as to white noise.

IV. Measurement Results

Figure 4 shows the fabricated current-reused folded-cascode front-end including LO frequency source, which is fully integrated in 0.18 μm 1-poly 6-metal CMOS technology. This chip occupies an area of 1.6×1.45 mm^2 including pads area. We also fabricated a conventional merged LNA and SB mixer for performance comparisons. The measured conversion gain of the conventional merged LNA and SB mixer is 20.4 dB, while taking only 500 μA from a 1.0 V power supply. In the same bias condition, the proposed front-end achieves a maximum

TABLE I
PERFORMANCE COMPARISON

	[2]	[6]	This work	This work	*Improvement
Type	Merged LNA & SB mixer	Cascaded LNA & SB mixer	Merged LNA & SB mixer	Current-reused front-end	-
Process	0.13-μm CMOS	0.18-μm CMOS	0.18-μm CMOS	0.18-μm CMOS	-
Frequency (GHz)	2.35	2.44	2.4	2.4	-
V_{DD}/I_{DD} (V / mA)	1.2 / 1.4	1.8 / 3.6	1.0 / 0.5	1.0 / 0.5	-
Power (mW)	1.68	6.48	0.5	0.5	
Voltage gain (dB)	14.5	21.4	20.4	30.5	10.1
P1dB (dBm)	-	-	-	–31	
NF (dB)	**24.5	13.9 @ 2-MHz IF	19 @10-MHz IF	10.1 @10-MHz IF	8.9
			13.1 @ 50-MHz IF	9.2 @ 50-MHz IF	3.9

*Performance improvement of the proposed front-end compared with merged LNA and SB mixer in this work.
**Measured from analog test output, not front-end.

gain of 30.5 dB, which is 10 dB greater than the conventional front-end.

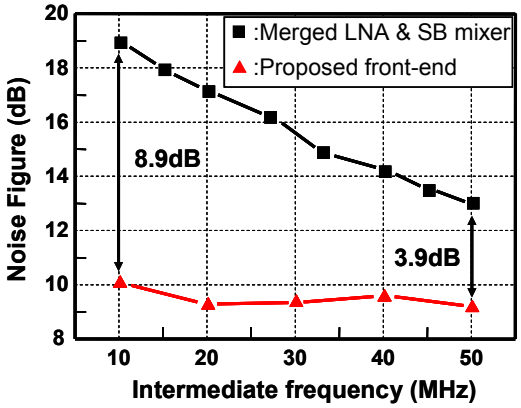

Fig. 5. Measured SSB NF of fabricated front-ends

Figure 5 shows the measured single-side band (SSB) noise figure over the output frequency range of 10 MHz to 50 MHz. As expected, the noise figure of the proposed front-end is at a more desirable level than that of the merged LNA and SB mixer. This is true over the entire measured frequency range. Especially notable is the fact that the noise figure shows a greater improvement at the lower output frequency in our graph (8.9 dB at 10 MHz and 3.9 dB at 50 MHz). This data confirms that the proposed current-reused folded-cascode front-end is much more immune to white noise as well as flicker noise due to the lower flicker noise contribution of the folded-cascode mixer and the noise screening effect of the LNA. Measured 1-dB compression point (P1dB) is –31 dBm. Table I shows the summary of the measured performances of the proposed current-reused front-end compared with a fabricated conventional merged LNA and mixer and previously reported works.

V. CONCLUSIONS

We proposed and demonstrated a 2.4-GHz fully integrated CMOS receiver front-end using current-reused folded-cascode circuit scheme. The proposed front-end improves noise figure and conversion gain by employing a vertically stacked LNA and folded-cascode mixer. The fully integrated 2.4 GHz receiver front-end achieves a voltage gain of 30.5 dB with a noise figure of 10.1 dB is achieved with 500 μW power consumption.

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