A 159.2mW SoC Implementation of T-DMB Receiver including Stacked Memories

Joohyun Lee*, Sungdo Kim*, Jinkyu Kim*, Duckhwan Kim*,
Youngsu Kwon*, Minseok Choi*, Kihyuk Park*, Bontae Koo*, Nakwoong Eum*, Hyuckjae Lee**
* Electronics and Telecommunication Research Institute (ETRI), Korea
** Information and Communication University (ICU), Korea

***Abstract* – This paper describes a system on chip (SoC) implementation of terrestrial digital multimedia broadcasting (T-DMB) receiver which integrates RF tuner, analog to digital converter (ADC), baseband processor, and multimedia processor in single silicon wafer. The pseudo-SRAM (PSRAM) and SDRAM are doubly stacked with method of silicon in package (SIP). A low-IF RF tuner and a 10bits pipelined ADC is used in this work as IP cores. Baseband processor contains Eureka-147 digital audio broadcasting (DAB) modem, MPEG1-Layer2 decoder, and outer decoder for T-DMB. Multimedia processor is consists of 32bit embedded micro processor, 24bit fixed-point DSP, and H.264/AVC hardware core. The T-DMB SoC was fabricated by using 0.13um 1poly 8metal (1P8M) CMOS process and it gives successful performance of 159.2mW total power dissipation including PSRAM and SDRAM at supply voltages of 1.2V, 2.5V for core and I/O respectively.**

I. Introduction

T-DMB system has been commercially launched in Korea. The T-DMB system is a broadcasting service which makes possible enjoying high quality audio and video at any time, at any place. Although T-DMB system is based on Eureka-147 DAB system [1], additional technology is also included to make this service possible in real world. Baseband system includes Eureka-147 receiver and outer decoder which consists of Reed-Solomon decoder and convolution de-interleaver [2]. Multimedia system is consists of bit-sliced-arithmetic-coding (BSAC) audio decoder and H.264/AVC video decoder [3][4].

Baseband processor needs large memory for time-deinterleaving and multimedia system also needs large memory for audio, video frame buffering. To complete T-DMB receiver we also need RF tuner and ADC functions.

T-DMB service mainly concerns on mobile device such as mobile-phone or hand-held equipments. In mobile application the power consumption and the area of chipset is important factor. In this work, all elements for T-DMB receiver are integrated in a single chip SoC. The implementation and its results is presented in this paper. The measured data of fabricated T-DMB SoC are also presented.

II. SoC Overview

The simplified block diagram for T-DMB SoC is shown in Fig. 1 and detailed block diagram is shown in Fig. 2. T-DMB SoC is consists of RF tuner, ADC, baseband processor, multimedia processor, and memories. There is two memories in Fig. 1. These are pseudo-SRAM(PSRAM) and SDRAM. The PSRAM is used for time de-interleaving in baseband processor, SDRAM is used for audio and video frame buffering in multimedia processor. The capacities of each are 4Mb, 64Mb respectively and these memories are stacked on T-DMB SoC. The wire bonding length was approximately 2.5um and 1.0um for PSRAM and SDRAM respectively.

T-DMB broadcasting service use Band-III (174~216Mhz) frequency band. The RF tuner selects one ensemble and output intermediate frequency (IF) signal to ADC. IF signals are sample by ADC, and sampled data are processed by baseband processor. Baseband processor demodulates the sampled data and output MPEG transport-stream (TS) to multimedia processor. Multimedia processor parses TS and de-multiplexes it to video and audio elementary-stream (ES). Audio ES is decoded by DSP and output to external digital-to-analog-converter (DAC), and video ES is decoded by H.264/AVC hardware core and output to LCD via on chip LCD controller. RF tuner, ADC, and Memories are treated as IP cores and baseband processor and multimedia processor are designed under considerations for low power dissipation. And then, all these elements are integrated in single chip T-DMB SoC.

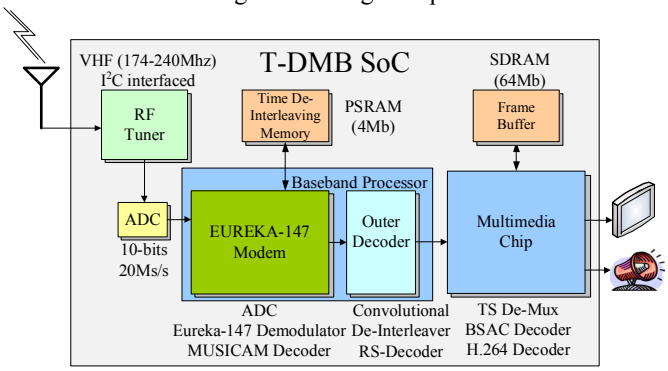

Fig. 1. Single Chip T-DMB Receiver Block Diagram

III. RF Tuner & ADC

RF tuner which used in this work is a low-IF RF tuner. A low-IF tuner does not have severe DC offset problem and there is no needs of discrete components for off-chip register and capacitor filter bank. Channel setting can be done via I^2C bus.

RF tuner selects one T-DMB ensemble [1] and output the IF signals differentially to ADC block. The output signal level is $500mV_{p\text{-}p}$ and impedance is matched with ADC input buffer.

The IF output signal is also connected to PAD. This is for the purpose of debugging (Fig. 2).

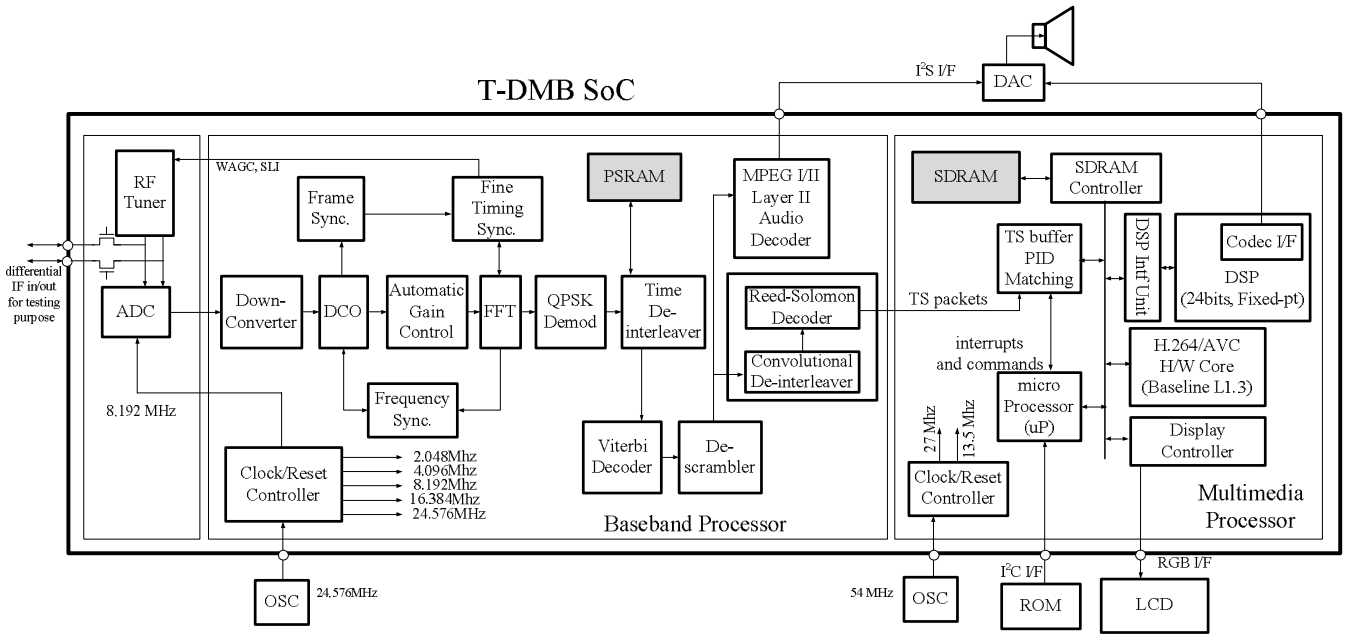

Fig. 2. Detailed T-DMB SoC Block Diagram

A 10-bits 20Msample/s pipelined ADC is used in this work, and used ADC is already silicon proven. The details of design and performances can be found in [5]. This ADC dissipates small power of 5mW and the area is only 0.26mm^2. These features and performance are very suitable for T-DMB SoC. For impedance and input signal level matching, buffer was inserted at input stage of ADC. For isolation from digital noise, a guard ring which has width of 113um was inserted around RF tuner.

IV. BASEBAND PROCESSOR

The ADC operated with sampling clock of 8.192Mhz and the sampling clock is generated from baseband processor. The down converter (Fig. 2) in baseband processor converts sampled IF signal to in-phase and quadrate-phase baseband signal. The sampling clock is 8.192Mhz and signal bandwidth is 2.048Mhz thus, the possible IF signals are given by

$$f_{if} = 2.048Mhz + n \cdot 4.096Mhz \quad (1)$$

where

$n = 0,1,2...$

f_{if} = frequency of IF signal

Most of conventional heterodyne tuners have 38.192Mhz IF output and the RF tuner in this work has 2.048Mhz IF output. Thus this sub-sampling technique is useful for both heterodyne tuner and low-IF tuner as well as attractive for several different IF frequencies.

Synchronization is performed in two steps. First one is initial acquisition (Fig. 3), and second is tracking.

During initial acquisition mode, the first thing to do is frame synchronization. Once frame timing is acquired, fine frequency synchronization is continuously performed for every symbol so, fractional portion of frequency offset is compensated. After that, coarse frequency synchronization estimates integral portion of frequency offset and compensates it. Fine timing synchronization is performed at the last of initial acquisition mode, and it estimates exact symbol timing and compensates it. This operation sequences are due to the dependencies among each synchronization algorithms.

In tracking mode, fine frequency synchronization is responsible for tracking of frequency-offset variation, and fine timing synchronization is responsible for timing drift.

The popular guard interval based (GIB) algorithm [6] is used for fine frequency synchronization algorithm and similar algorithm with [7] is used for coarse frequency synchronization.

Channel impulse response (CIR) is calculated in every frames to achieve fine timing synchronization. This can be done with received phase reference symbol (PRS) and original PRS. The timing offset can be derived as following

$$CIR = invFFT(r_k / z_k)$$
$$\delta = \underset{k}{Max}(CIR) \quad (2)$$

where

r_k = received PRS

z_k = original PRS

δ = timing offset

The frequency offset can be compensated with phase rotation operation. This is done via digital controlled oscillator (DCO) in Fig. 2. The T-DMB system use differential QPSK modulation. In this case, SNR degradations due to frequency offset is smaller than 0.1dB if frequency offset is smaller than 0.01 of subcarrier spacing. The designed DCO has resolutions

of 0.001 of subcarrier spacing. Automatic gain control (AGC) is performed before FFT to prevent overflow in FFT operations (Fig. 2).

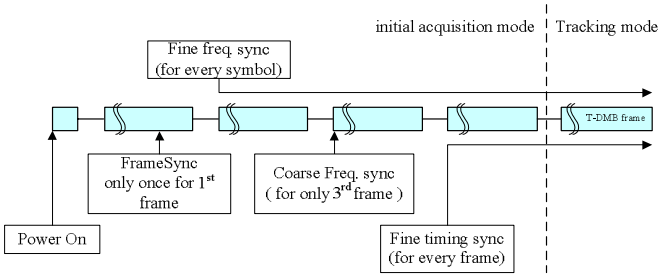

Fig. 3. Synchronization flow

After synchronization, OFDM demodulation is performed by FFT and QPSK demodulator block (Fig. 2). Time de-interleaver block performs de-interleaving of 384ms data. And then, forward error correction (FEC) is followed by de-puncturing of data. A viterbi decoder is used for FEC and it has the parameters of 4bit soft decision metric, truncation length of 128. T-DMB also includes the MPEG1-Layer2 audio service (This is also known as MUSICAM). A fully hardwired MUSICAM decoder is designed and included.

The outer decoder is adopted in T-DMB to meet the bit error rate (BER) performance for the multimedia service [2]. The outer decoder is consists of convolutional de-interleaver and Reed-Solomon decoder (RSD). RSD has parameters of (204,188,t=8) which is a shortened code from (255, 239) and generator polynomial and primitive polynomial are given by

$$g(x) = (x+\lambda^0)\cdot(x+\lambda^1)\cdot(x+\lambda^2)\cdot\ldots\cdot(x+\lambda^{15})$$
$$p(x) = x^8 + x^4 + x^3 + x^2 + 1 \quad (3)$$

where

$p(x)$ = *primitive polynomial*

$g(x)$ = *generator polynomial*

V. Multimedia Processor

The multimedia processor in this work is capable of TS demultiplexing, H.264 decoding, BSAC decoding and objects synchronization. T-DMB system use H.264/AVC and BSAC standards for video and audio application respectively.

Although T-DMB system use baseline profile level 3 of H.264/AVC, there is more restrictions to simplify hardware implementation [8]. H.264/AVC decoder in this work is conforms to T-DMB specification and designed with fully hardwired logic under low power considerations.

Baseband processor outputs TS to multimedia processor. TS buffer (Fig. 2) captures the TS packets and sends interrupts to micro processor (uP). The uP is responsible for scheduling of all video decoding procedures and parsing of incoming TS packets. After interrupt is acknowledged, uP parses the TS packets and extracts packets elementary stream (PES) packets, synchronization layer (SL) packets, and ES in consequence [8]. After parsing TS packets uP decides the T-DMB service channel and set the program identification (PID) information to PID matching unit in Fig. 2.

Once PID is set, the PID matching unit can select the correspondent packets and move the data to SDRAM independently so, the work load of uP can be reduced.

After TS packets are de-multiplexed, ES is stored in SDRAM which is the frame buffer of audio and video data. If the decoding start command is received from uP, the H.264/AVC H/W core (Fig. 2) patches the frames from SDRAM and decodes it. Once decoding procedures for a frame is completed, decoded frame is stored to decoded picture buffer (DBP) area in SDRAM.

Block diagram of H.264/AVC H/W core is shown Fig. 4. Command processor decodes the uP's commands to its internal command codes and sends to each blocks. Variable length decoder (VLD) decodes exp-golomb code and fixed length code (FLC) which is used for data other than video residual data such as syntax elements. VLD also decodes context-adaptive-variable-length-code (CAVLC) which is used for quantized transform coefficients i.e. video residual data. Transform block performs all types of H.264/AVC transforms such as 4x4 integer transform, 2x2 hadamard transforms and it is also incorporated with de-quantization.

After booting procedure, DSP continuously checks whether the audio frame data are ready in SDRAM. If audio ES is stored in SDRAM, uP sends information of audio ES to DSP interface unit (Fig. 2). After that, patching the audio ES and decoding procedures are performed by DSP. Decoded audio data are sent to external DAC via on chip I^2S interface.

uP is also parses the PCR, OCR, CTS, DTS in formations from incoming data packets to synchronize the audio, video object [3].

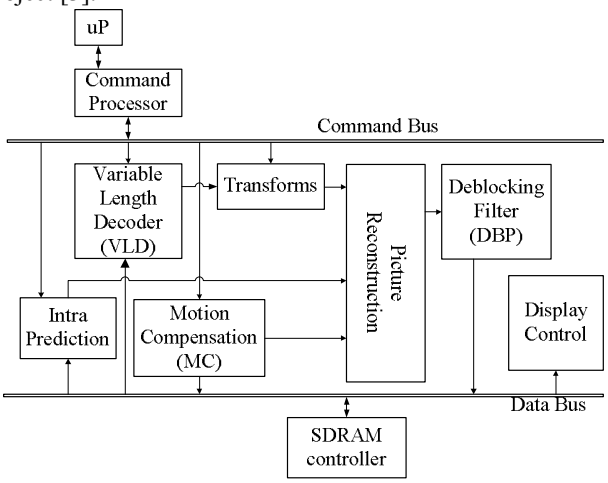

Fig. 4. H.264/AVC H/W core block diagram

VI. Implementation And Measurements

The clock domains of baseband processor and multimedia processor are carefully partitioned in 8 groups of 2.048Mhz, 4.096Mhz, 8.192Mhz, 16.384Mhz, 24.576Mhz, 13.5Mhz, 27Mhz, and 54Mhz. This optimization of clock domain is not just variations of operating frequency but the data processing algorithms for each functional block are also optimized for their clock domain. So, we can reduce the power and the size of T-DMB SoC. The detailed clock domain partitioning is

summarized in Table. 1, and T-DMB SoC implementation results are summarized in Table. 2.

The fabricated T-DMB SoC photo and its stacked photo are shown in Fig. 5-Fig. 6 and measured RF tuner performances are summarized in Table. 3. ADC and RF tuner performances are same as that of their stand-alone specifications. The power dissipation measurements are summarized in Table. 4.

VII. Conclusion

All elements for T-DMB receiver are integrated in a single chip SoC and is fabricated with 0.13um 1P8M CMOS process. Memories (PSRAM, SDRAM) are stacked on it by SIP process. The fabricated chip is verified with wireless outdoor receiving test and it shows successful performance with total power dissipation of 159.2mW including PSRAM and SDRAM at supply voltages of 1.2V, 2.5V for core and I/O respectively.

Table. 1 Clock Domain Partitions

Clock Domain	*Module Name*
24.575 Mhz	FFT, FreqSync, RF tuner
16.384 Mhz	Viterbi, RSD
8.192 Mhz	ADC, Down Converter, Time De-interleaver
4.096 Mhz	QPSKdemod, TSbuffer, MP2decoder
2.048 Mhz	AGC, DCO, FrameSync FineTimingSync, De-scrambler
54 Mhz	DSP
27 Mhz	H.264core, uP, SDRAM controller
13.5 Mhz	Display Ctrl.

Table. 2. T-DMB SoC Implementation Results

Block	*Area or Gate Counts*	*Descriptions*
RF tuner	2.2 mm x 2.5 mm	
ADC	0.59 mm x 0.44 mm	
Baseband Proc.	636,972 gates	including memory (398,816 bits)
Multimedia Proc.	441,525 gates	Including memory (291,672 bits)
DSP	895,867 gates	including memory x/y-mem:16Kx24 for each. p-mem:16Kx24
Total	6.0mm x 6.0mm (1,974,368 gates)	

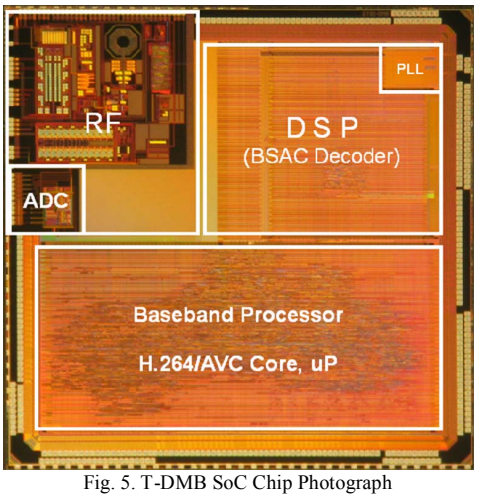

Fig. 5. T-DMB SoC Chip Photograph

Fig. 6. Memory Stacked T-DMB SoC Photograph

Table. 3. Measured RF tuner Performance

Parameters	*Value*	*Descriptions*
Sensitivity	-100 dBm	Gaussian channel
Receiver Noise Figure	3.75 dB	Cascade, max. gain
Receiver Linearity(IIP3)	+19 dBm	minimum gain condition
LO Phase noise	-88 dBc/Hz	100 KHz offset freq.
Adjacentb Ch selectivity	38 dB	1.712 Hz offset from center freq.
Far-off selectivity	48 dB	5.0 MHz offset from center freq.
Image Rejection Ratio	50 dB	Max. gain mode

Table. 4. T-DMB SoC Power Dissipation Measurements

Block	*Current (mA)*	*Supply (V)*	*Power (mW)*
RF tuner	22.0	1.2	26.4
ADC	4.0	1.2	4.8
Baseband+Multimedia	40.0	1.2	48
I/O+PSRAM+SDRAM	32.0	2.5	80
Total			*159.2*

VIII. Acknowledgment

This work is supported in part by the Ministry of Information and Communication of Korea.

Authors appreciate to Youngdeuk Jeon, who designs ADC and gives hand to make ADC as part of SoC.

IX. References

[1]. "Radio Broadcasting Systems; Digital Audio Broadcasting to mobile, portable and fixed receivers", ETSI EN 300 401, 2001

[2]. "Digital Audio Broadcasting ; Data Broadcasting – MPEG-2 TS streaming", ETSI TS 102 427, 2005

[3]. "Information technology – Coding of audio-visual objects – part 10: Advanced video coding", ISO/IEC 14496-10

[4]. "Information technology – Coding of audio-visual objects – part 3:Audio", ISO/IEC 14496-3

[5]. Young-Deuk Jeon, Seung-Chul Lee, et al, "A 5-mW 0.26mm^2 10-bit 20-MS/s Pipelined CMOS ADC with Multi-Stage Amplifier Sharing Technique", IEEE ESSCIRC, pp.544-547, 2006

[6]. Moose, Paul H. "A Technique for Orthogonal Frequency Division Multiplexing Frequency Offset Correction." IEEE Transactions on Communications, vol. 42, No. 10, Oct. 1994, pp. 2908-2914

[7]. Keukjoon Bang , Namshin Cho "A Coarse Frequency Offset Estimation in an OFDM System Using the Concept of the Coherence Phase Bandwidth", IEEE Transactions on Communications, vol.49, no.8, Aug. 2001

[8]. "Digital Audio Broadcasting DMB video service; UserApplication Specification", ETSI TS 102 428, 2005