Low-Crosstalk 10-Gb/s Flip-Chip Array Module for Parallel Optical Interconnects

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***Abstract*—A 10-Gb/s optical receiver array with low interchannel crosstalk is realized by exploiting an InGaP–GaAs heterojunction bipolar transistor technology in a three-dimensional multilayer low-temperature cofiring ceramics (LTCC) module. Neutralization feedback circuit with LTCC embedded bus structure is proposed to suppress significant high-frequency crosstalk from on-chip bus and intermetallic capacitance. This module demonstrates 5 dB better suppressed-coupling than a conventional on-chip bus module with 0.8-dB power penalty.**

***Index Terms*—Channel crosstalk, flip-chip, low-temperature cofiring ceramic (LTCC) substrate, parallel optical interconnects, transimpedance amplifier.**

I. Introduction

PARALLEL optical interconnects emerge as the most effective solutions for very short reach interfaces which cover terabit-per-second (Tb/s) class switching systems and enterprise class server clusters [1]. However, when compared to long-haul optical point-to-point systems, its design faces a very challenging specification, i.e., crosstalk. Since parallel optical interconnects are typically based on multimode fiber ribbon cable technology, there exist inherently the physical limitation of channel pitch (250 μm) in a single chip array.

In order to facilitate the severe crosstalk problem from narrow channel pitch, balanced parasitic capacitances, and separate interstage biasing were introduced in [2] and channel pitch conversion technique was proposed in [3]. Yet, previous research had barely suppressed the crosstalk at higher frequencies than 10 GHz, and thus, led to large power penalty in the multichannel operations. Hence, an efficient high-speed crosstalk suppression technique is proposed in this letter, including the judicious designs of chip layout and low-temperature cofiring ceramic (LTCC) module structure simultaneously.

II. Circuit Descriptions: Transimpedance Amplifier Array

Fig. 1(a) shows the block diagram of a single-channel receiver, consisting of transimpedance amplifier stage (TG), neutralization gain (NG) stage, and output buffer (LT). All blocks are designed to be fully differential in order to minimize TIA common mode noises. The TIA stage incorporates only the resistive negative feedback through R_F, whereas, the following NG stages employ neutralization feedback including a feedback resistor R_N and a small neutralization capacitance C_N. This frequency-dependent path creates a positive feedback loop on the input transistors Q_1 and Q_2, which helps to achieve wide-band flat gain in the frequency response.

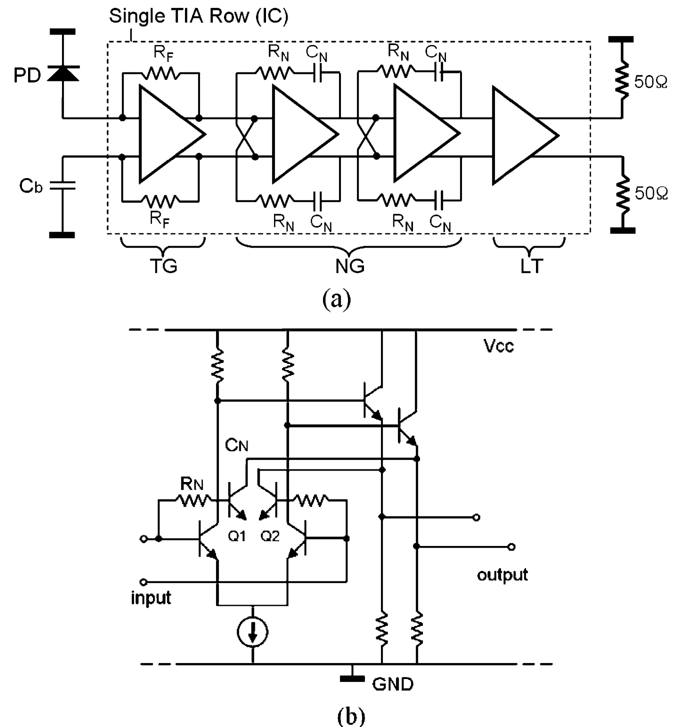

Fig. 1. (a) Block diagram of a single channel receiver, where C_b is the off-chip balancing capacitor and (b) schematic diagram of the NG stage using $C_{\rm bc}$ of Q_1 as C_N.

For efficient suppression of interchannel crosstalk, the receiver chip is implemented with an InGaP–GaAs heterojunction bipolar transistor (HBT) technology providing high substrate resistance. However, the GaAs technology has an inherent drawback, i.e., high turn-on voltage (around 1.4 V) and, thus, requires high supply voltage. This drawback is avoided in this work by employing the positive neutralization feedback circuit, leading to only 5-V supply. Fig. 1(b) illustrates the schematic diagram of the NG stage, where the value of C_N is nearly 300 fF. It is implemented with the base-collector capacitance $C_{\rm bc}$ because on-chip metal–insulator–metal capacitors cannot achieve such a small capacitance on the GaAs substrate.

The well-known crosstalk paths in a multichannel single-chip are summarized as 1) the capacitive coupling between closely

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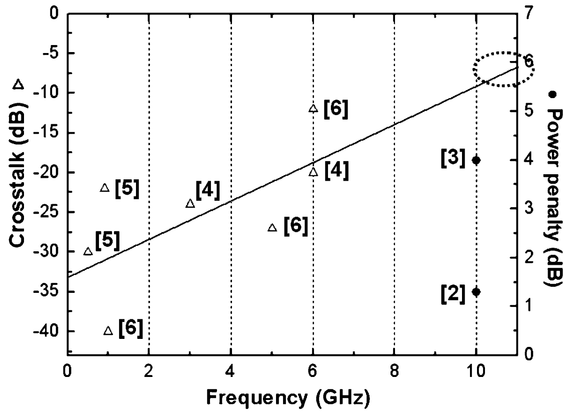

Fig. 2. Previously reported power penalties at 10 Gb/s, and crosstalk of the array receiver ICs at various data rates [2]–[6].

adjacent signal lines, 2) the parasitic inductances of on-chip supply and ground buses, and 3) the parasitic intermetallic capacitances. The first path is mainly due to the fixed narrow pitch (250 μm) of the multimode fiber, which cannot be improved at integrated circuit (IC) design level. The second path is typically due to the long stretched shape of buses and gives the most significant impact on the high-frequency crosstalk, because the parasitic inductances facilely transfer the noise voltage from an operating channel to adjacent channels. Particularly, the bond wires at the end of the buses render this effect even worse due to their large intrinsic inductance, and result in quite severe noisy buses on the operating channels. The third path of intermetallic capacitance is relatively small, yet providing considerable coupling at high frequencies.

Fig. 2 shows the previously reported power penalties and crosstalk measurements with fully differential IC topologies [2]–[6], where it is clearly seen that no less than 1.3 dB of power penalty was achieved at 10 Gb/s at best. Also, a linear extrapolation was conducted in Fig. 2 in order to obtain the quantitative amount of crosstalk at 10 GHz, indicating that a 10-Gb/s multichannel array chip realized in a conventional on-chip bus module may suffer from less than -10-dB crosstalk at 10 GHz.

This work presents two different three-channel arrays implemented with the same TIA circuit layout for each channel in order to compare the interchannel crosstalk quantitatively up to 10 GHz. In Fig. 3(a), it is clearly seen that the supply and ground buses take relatively large crossing area with lower metallization with conventional on-chip bus module structure. However, the width of these buses cannot be simply reduced because it will directly increase the parasitic inductance of bus lines and, thus, the line crosstalk, indicating that the conventional on-chip line bus structure cannot relax this inevitable tradeoff. Therefore, we propose a novel LTCC embedded bus structure with flip-chip bonding to remove these noisy on-chip buses which will leads to effective crosstalk suppression. The metallization crossing area decreases as well from 12 600 to 2050 μm^2 per each channel, as shown in Fig. 3(b).

III. Three-Dimensional LTCC Module

The array IC with flip-chip pads needs an embedded line multilayer structure in order to connect each pad separately.

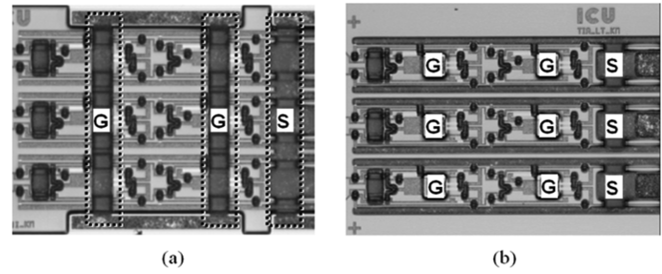

Fig. 3. Chip microphotographs of both 10-Gb/s array IC (a) with on-chip buses and (b) with LTCC embedded buses using flip-chip bonding pads, where G is ground pad and bus and S is supply voltage pad and bus.

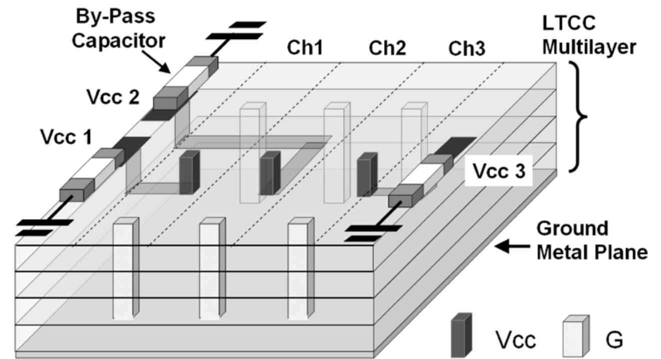

Fig. 4. Simplified schematic of LTCC multilayer module, where V_{cc} is the supply voltage and G is ground.

Therefore, LTCC is a very attractive technology due to its fine embedded line patterning and excellent transmission characteristics from dc to 10 GHz. Fig. 4 illustrates the simplified schematic of the LTCC multilayer module, where each supply voltage uses a separate embedded line that is connected to a bypass capacitor. Ground connections are realized through via holes directly to the bottom ground plane to minimize the parasitic inductance. Photodiodes are mounted using active align technique with bond-wires for both modules.

IV. Experimental Verification

The frequency responses of both modules were measured by using HP 8703B lightwave component analyzer. A 1510-nm light source is loaded on the InGaAs PD at Channel 2 with the input power level of -11.4 dBm. Also, the adjacent channel crosstalk is measured simultaneously with no light signal loading. Fig. 5(a) demonstrates the measured results of the conventional on-chip bus module, yielding -16 dB of crosstalk at 5 GHz and -10 dB at 10 GHz. It confirms the estimated value shown in Fig. 2. This module shows much worse coupling at higher frequencies. Meanwhile, the LTCC multilayer bus module with flip-chip bonding achieves -27-dB crosstalk at 5 GHz and -15 dB at 10 GHz, as shown in Fig. 5(b). This level of signal-to-crosstalk ratio maintains up to 13 GHz.

Fig. 6 depicts the measured eye diagrams of the midchannels of both modules for 5- and 10-Gb/s nonreturn-to-zero $2^{31}-1$ pseudorandom binary sequence, respectively, when all adjacent channels are simultaneously turned ON. Fig. 7 shows the measured bit-error rate (BER) of the LTCC embedded bus modules. In the conventional on-chip bus module, eye diagrams and BER test results could not be properly measured at 10 Gb/s because of

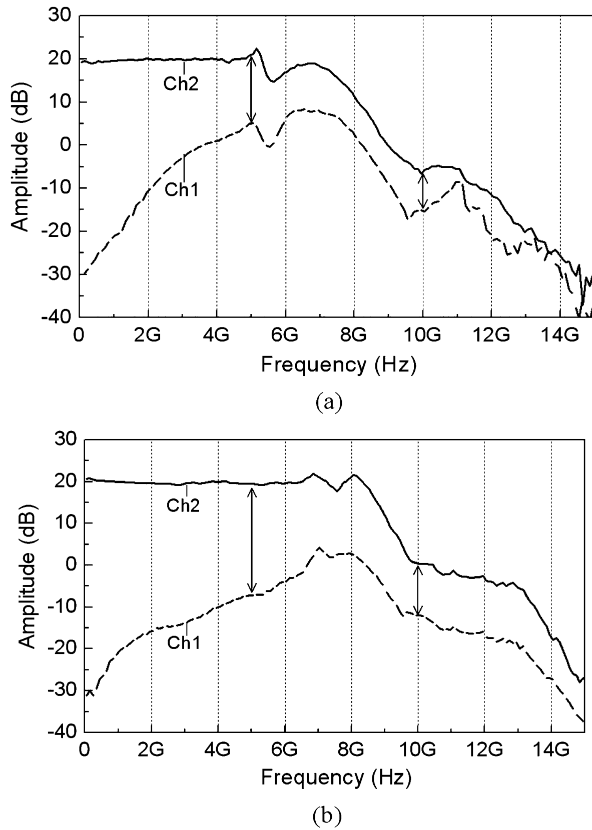

Fig. 5. Measured frequency responses of both 10-Gb/s receiver array modules: (a) conventional on-chip bus module and (b) LTCC embedded bus module.

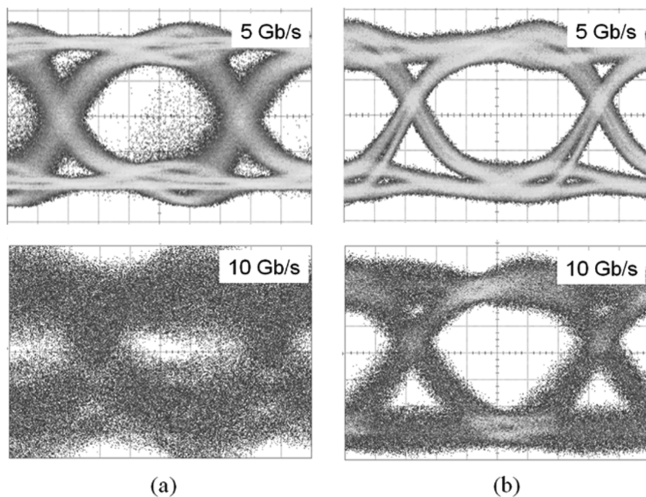

Fig. 6. Measured eye diagrams of the midchannel with adjacent channels turned ON simultaneously: (a) in a conventional on-chip bus module and (b) in the LTCC embedded bus module with flip-chip bonding.

the severe crosstalk noise. Meanwhile, the proposed LTCC embedded bus module achieves the wide-open eye diagrams and also demonstrates only 0.8-dB power penalty. Hence, it clearly reveals that the proposed module suppresses the high-frequency crosstalk effectively and, hence, provides a reliable solution for 10-Gb/s multichannel optical receiver arrays.

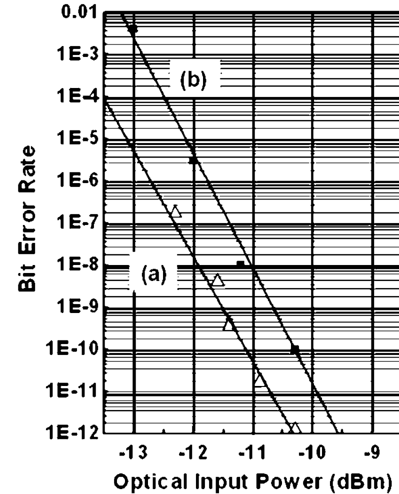

Fig. 7. Measured BER of the LTCC embedded bus module: (a) with a single channel operation, and (b) with three channels turned ON.

V. Conclusion

A 10-Gb/s multichannel receiver array has been realized in a multilayer LTCC bus module by exploiting an InGaP–GaAs HBT technology for the applications of parallel optical interconnects. It incorporates the neutralization feedback circuit technique that achieves wide-band flat gain characteristic with low power supply of 5 V. Due to the significant reduction of the bus line parasitic inductances and intermetallic parasitic capacitances, the LTCC embedded bus module achieves 5 dB better crosstalk at 10 GHz than a conventional on-chip bus module, with only 0.8-dB power penalty. For future high-end systems, this novel LTCC module structure can be one of the main solutions because above two parasitic crosstalk paths inevitably increases with channel number growth to 12 or even higher with on-chip bus module structure.

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