Duo-Binary Circular Turbo Decoder Based on Border Metric Encoding for WiMAX

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Abstract - This paper presents a duo-binary circular turbo decoder based on border metric encoding. With the proposed method, the memory size for branch memory is reduced by half and the dummy calculation is removed at the cost of the small-sized memory which holds the encoded border metrics. Based on the proposed SISO decoder and the dedicated hardware interleaver, a duo-binary circular turbo decoder is designed for the WiMAX standard using a 0.13 µm CMOS process, which can support 24.26 Mbps at 200MHz.

I. Introduction

The turbo code introduced in 1993 is one of the most powerful forward error correction channel codes. Recently, non-binary tail-biting turbo codes have received a great attention and adopted in several mobile radio systems such as DVB-RCS and IEEE 802.16 standard (WiMAX) [1], as they can offer many advantages over the classical single-binary turbo codes [2]. To avoid spectrum waste caused by the tail bits, the circular coding technique is also employed in the turbo codes. How to SISO decode the duo-binary turbo codes and its complexity compared to the classical single-binary turbo codes are well described in [3].

This paper presents an energy-efficient SISO decoder suitable for the non-binary circular turbo decoding. Based on the proposed architecture, a double-binary circular turbo decoder is implemented for the WiMAX with a dedicated hardware interleaver.

II. Border Metric Encoding

The sliding window technique is effective in reducing the memory size required to store metric values. Compared to the sliding window which requires the dummy calculation to obtain the reliable initial values of each window at the borders, as shown in Fig. 1, the sliding window with border memory which use the values of the previous iteration for the reliable border metric values are preferred since it can avoid the dummy backward metric calculation and suitable for circular turbo decoding [3].

Although the sliding window with the border memory can eliminate the need of the dummy calculation, the border memory size is considerable. By allowing a few values to represent the border metrics, the reduction of the border memory can be realized. A simple encoding with low hardware complexity is to floor the original metric value to the closest power-of-two number as shown in Fig. 2. In Fig. 3, the BER performance of the proposed encoding is compared with those of various methods. The size of the border memory can be reduced significantly by using the proposed encoding with which leads to overall memory size reduction of a SISO decoder [3].

III. Duo-Binary Circular Turbo Decoder Implementation

A. Hardware Interleaver Design for the WiMAX

For 3G wireless systems, a dedicated hardware interleaver that generates interleaved addresses on-the-fly has been proposed to achieve small area [4]. Such a dedicated interleaver is also effective in reducing power consumption as

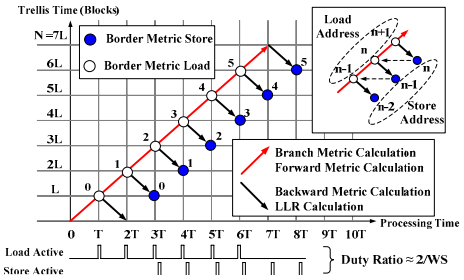

Fig. 1. Sliding window diagram with border memory

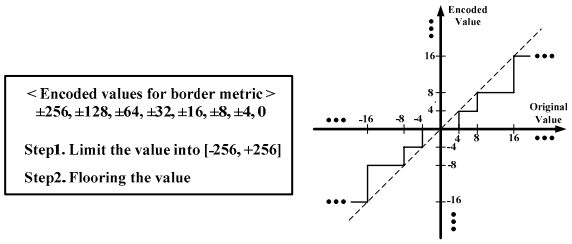

Fig. 2. Proposed 4-bit border metric encoding

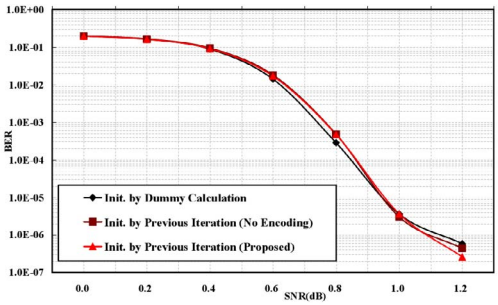

Fig. 3. BER performance with 8 iterations for 4800-bit frame

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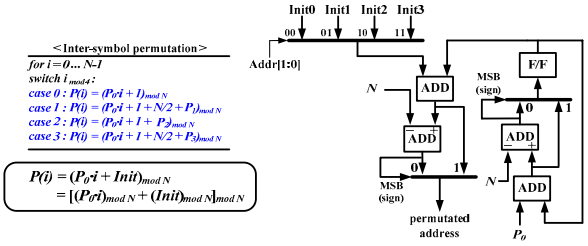

Fig. 4. Interleaver structure for the WiMAX

there is no need to include a large-sized memory. Fig. 4 describes how to calculate the interleaved addresses on-the-fly for the WiMAX, where P_0, P_1, P_2 and P_3 are determined according to the frame length, N [1]. Since the input address increases sequentially, accumulating P_0 and adding it to an initial value selected by the two LSBs can generate the permutated address. To replace the complicated modulo operation, subtractions are performed in Fig. 4 when the intermediate values are not less than N. The initial values are pre-calculated and maintained in a small table.

B. Turbo Decoder for the WiMAX

With the quantization indicated in Table I, a Max-log-MAP decoder based on the proposed border metric encoding was synthesized with a 0.13 μm 6-Metal CMOS standard-cell library. Design Compiler and Power Compiler of Synopsys were used for the synthesis and power estimation, respectively.

The proposed duo-binary circular turbo decoder is based on the time-multiplex architecture consisting of one SISO decoder, an extrinsic information memory and a dedicated interleaver. The proposed turbo decoder occupies 2.24mm^2 and the die photo of the proposed turbo decoder is shown in Fig. 5. The total gate count of the proposed turbo decoder is 65,724 excluding memories and the critical path delay is 4.2ns. The buffers are implemented using single-port SRAMs, and small-sized RAM and ROM memories are replaced with registers and logic circuitry, respectively. To process a 2400-pair (4800-bit) frame, the proposed turbo decoder takes 39,585 cycles for eight iterations. As a result, the data rate that the proposed turbo decoder operating at 200MHz can process is 24.26Mbps.

In Table II, the energy consumption of the proposed SISO decoder is compared with that of the conventional decoder. As shown in Table II, the energy consumption of the SISO logic is reduced by eliminating the dummy calculation. Also, the energy consumption of the border memory is very low because the memory is small and infrequently accessed as

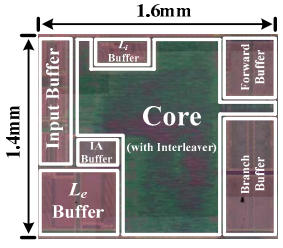

Fig. 5. Die photo of the proposed turbo decoder chip.

TABLE I
Implementation Environment

Window Size	32
Quantization	Received input : (6,2) Branch Metrics & State Metric : (10, 2) Extrinsic Information : (8, 2) LLR value : (11, 2)

TABLE II
Energy Consumption of SISO Decoders for 8 iterations

	With Dummy Calculation	Proposed
SISO Logic	1056.6 pJ/bit/iter	844.6 pJ/bit/iter
Interleaver	24.8 pJ/bit/iter	1.6 pJ/bit/iter
Branch Memory	579.8 pJ/bit/iter	292.5 pJ/bit/iter
Forward Memory	251.6 pJ/bit/iter	251.6 pJ/bit/iter
Border Memory	N.A.	22.2 pJ/bit/iter
Total	1912.8 pJ/bit/iter (100%)	1412.5 pJ/bit/iter (73.8%)

shown in Fig. 1. Employing the dedicated hardware interleaver, the area and power consumption are significantly reduced compared to the table-based interleaver. Therefore, the proposed SISO decoder can reduce the energy consumption by 26.2% compared to the SISO decoder based on the dummy calculation and table-based interleaver.

V. Conclusions

We have proposed an energy-efficient SISO decoder based on the border metric encoding, which is especially suitable for the non-binary circular turbo codes. In addition, a dedicated hardware interleaver compatible with the WiMAX is employed to reduce power and area further. The duo-binary circular turbo decoder implemented for the WiMAX supports 24.26Mbps at 200MHz.

Acknowledgements

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